Wio-LR2021 Module

LoRa® Wireless Module LR2021

Datasheet

v1.0

Content

1. Introduction

Wio-LR2021 is a next-generation, multi-band wireless transceiver module powered by Semtech's fourth-generation LR2021 chipset. Engineered as a unified RF platform, it integrates Sub-GHz (863–928 MHz), 2.4 GHz ISM, and licensed S-band (1.6–2.4 GHz) operation into a single compact subsystem, eliminating the need for multiple radio designs across regional and application boundaries.

1.1. Feature

Unified Multi-Band RF Platform

- Sub-GHz: 863~928 MHz (868/915 MHz ISM bands)[1], receive sensitivity down to –141.1 dBm (SF12/125 kHz), transmit power up to +22 dBm
- 2.4 GHz ISM: 2400–2500 MHz global operation, sensitivity down to –133 dBm, supporting data rates up to 2.6 Mbps (FLRC modulation)
- S-Band: 1.6–2.4 GHz licensed spectrum for satellite IoT (NTN), sensitivity down to –131 dBm

Ultra-Low Power Consumption

- Transmit: 116 mA (Sub-GHz @ +22 dBm), 28.4 mA (2.4 GHz @ +12 dBm)
- Receive: 8.19 mA (Sub-GHz), 8.59 mA (2.4 GHz)
- Deep sleep: 583 nA
- Idle: 960 uA

Advanced Modulation & Protocol Support

- Modulation: LoRa, (G)FSK, (G)MSK, FLRC, 4-FSK, O-QPSK, and LR-FHSS (transmit-only) for enhanced anti-interference
- Protocol stack[2]: LoRaWAN (Sub-GHz and 2.4 GHz), Bluetooth® LE 5.0, IEEE® 802.15.4 (Thread®/Zigbee™), Wi-SUN, Wireless M-BUS

- Concurrent multi-Spreading Factor (SF) reception and enhanced Channel Activity Detection (CAD) for high-density deployments

NOTE:

1. While the Semtech LR2021 transceiver covers the 150–960 MHz range, the Wio-LR2021 module's RF front-end including the matching network and harmonic filtering is factory-optimized for the 868 MHz and 915 MHz ISM bands to ensure certified RF performance and regulatory compliance.

For deployments requiring the 433–490 MHz band, a dedicated low-frequency variant, designated Wio-LR2021-LF, is currently under development for native operation in the low-frequency band. Contact sensecap@seeed.cc for feasibility and lead-time assessment.

2. Protocols such as BLE, Thread, Zigbee, Wi-SUN, and Z-Wave require the main MCU to run the corresponding MAC/network protocol stack, whereas the Wio-LR2021 only provides support for physical-layer modulation/demodulation and packet processing.

1.2. Diagram

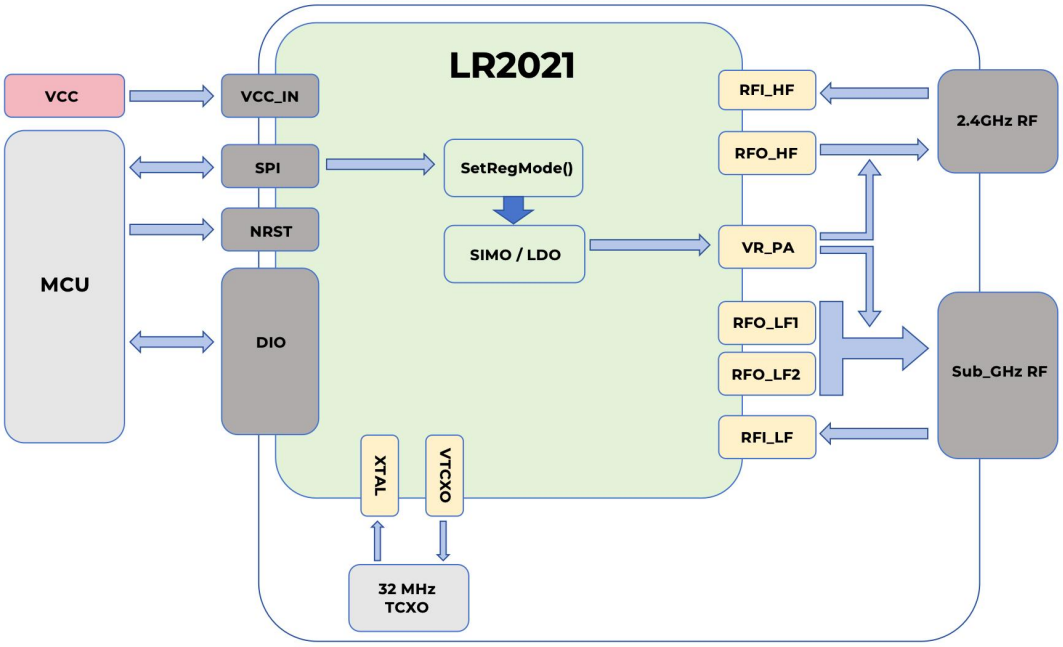

Figure 1 Wio-LR2021 Schematic Diagram

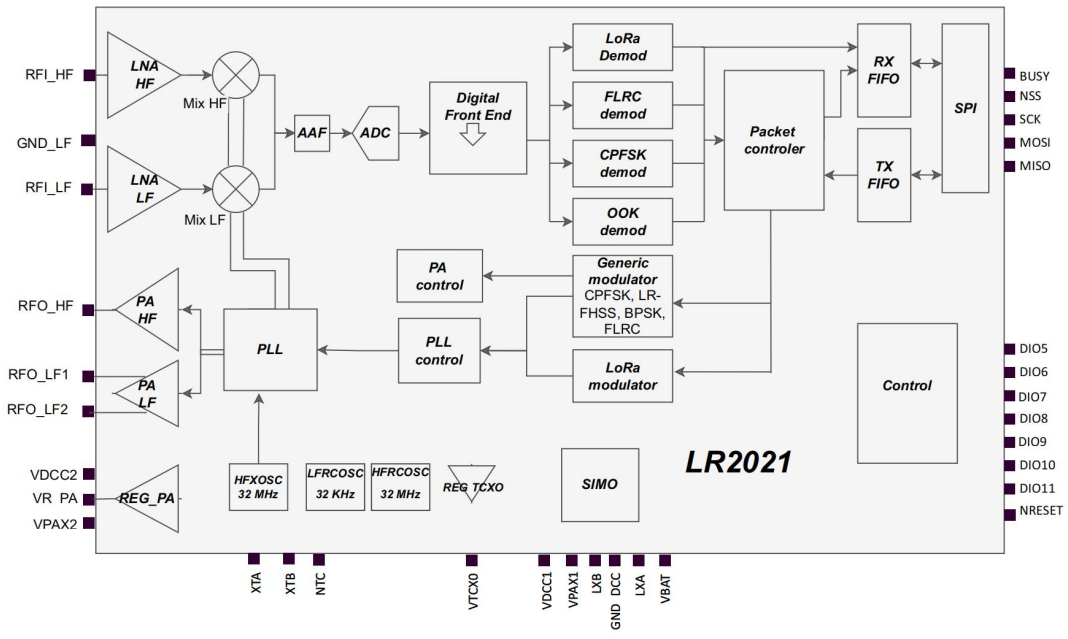

Figure 2 LR2021 Block Diagram

2. Description

2.1. Pin Definition

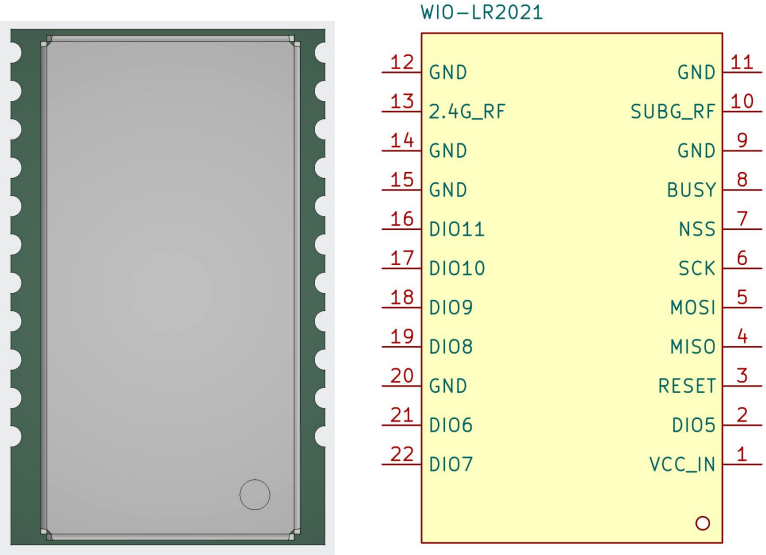

Figure 3 Wio-LR2021 Pinout

Number	Name	Type	Description
1	VCC_IN	Power	Power supply
2	DIO5	I/O	Multi-purpose digital I/O
3	RESET	I	Reset signal, active LOW
4	SPI_MISO	O	SPI MISO
5	SPI_MOSI	I	SPI MOSI
6	SPI_SCK	I	SPI clock
7	SPI_NSS	I	SPI chip select
8	BUSY	O	Busy indicator signal
9	GND	-	Ground
10	SubG_RF	RF	Sub-GHz channel
11	GND	-	Ground
12	GND	-	Ground
13	2.4G_RF	RF	2.4GHz channel
14	GND	-	Ground
15	GND	-	Ground
16	DIO11	I/O	Multi-purpose digital I/O
17	DIO10	I/O	Multi-purpose digital I/O

18	DIO9	I/O	Multi-purpose digital I/O
19	DIO8	I/O	Multi-purpose digital I/O
20	GND	-	Ground
21	DIO6	I/O	Multi-purpose digital I/O
22	DIO7	I/O	Multi-purpose digital I/O
Note: 1. The LR2021 only features 7 multi-purpose I/O channels (DIO5~DIO11); it does not have DIO0~DIO4 pins. Wio-LR2021 module has exposed all 7 DIO channels.			

2.2. DIO Specification

All DIO functions (IRQ, RF switch control, clock output, Tx/Rx trigger) must be configured via SPI command *SetDioFunction* while the module is in STDBY_RC mode. Configuration is retained across Sleep (warm start) but lost after a cold start or power cycle.

Upon module power-up or reset release, the LR2021 transceiver enters STDBY_RC mode with the following default pin states:

- DIO5, DIO6: Internal weak pull-up to VCC_IN. These two pins will read logic-high if left unconnected.
- DIO7~DIO11: High-impedance (Hi-Z). External pull-up or pull-down resistors are recommended if these pins are routed to the host PCB and not immediately configured by firmware.

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Please note that exceeding these values will result in permanent damage and functional degradation.

Item	Value
Supply Voltage (Vcc)	3.9 V
IO Voltage	3.9 V
Operating Temperature	-40 ~ 85 ℃
Storage Temperature	23 ± 5 ℃
Maximum RF Input Power	+10 dBm[1]
CAUTION: This module employs a switchless Direct-Tie matching network where the PA output (RFO) and LNA input (RFI) share the same RF node. Consequently, any external power applied to the antenna port is presented simultaneously to both the RFI and RFO pins of the LR2021. [1] The +10 dBm absolute maximum is a stress rating only. Functional operation at or above **+6 dBm** is not recommended and may degrade device reliability. External power above +6 dBm requires additional front-end protection.	

3.2. Normal Working Conditions

	Min	Typical	Max	Units	Remark
Supply Voltage (Vcc)	1.8	3.3	3.7	V	Ripple: 11.2mV, BW: 20MHz
VTCXO (Internal)	-	3.0	-	V	Ripple: 8.129 mV, BW: 20MHz
Transmit Current	-	-	-	mA	490MHz @ 17dBm
	-	38.5	-	mA	868MHz @ 14dBm
	-	119.4	-	mA	915MHz @ 22dBm
	-	28.4	-	mA	2.4GHz @ 12dBm
Receive Current	-	8.19	-	mA	Sub-GHz LoRa @ SF12, 125kHz
	-	8.59	-	mA	2.4GHz LoRa @ SF12, 125kHz

	-	7.99	-	mA	915MHz FLRC @ 260kbps
	-	11.92	-	mA	915MHz FLRC @ 2600kbps
	-	8.52	-	mA	2.4GHz FLRC @ 260kbps
	-	12.60	-	mA	2.4GHz FLRC @ 2600kbps
Sleep Current	-	583	-	nA	
Idle Current	-	960	-	uA	

3.3. Digital I/O Characteristics

	Min	Typical	Max	Units	Remark
Output Logic 1 (VOH)	0.9×VCC	-	VCC	V	I_{max}=2.5mA
Output Logic 0 (VOL)	0	-	0.1×VCC	V	I_{max}=-2.5mA
Input Logic 1 (VIH)	0.7×VCC	-	VCC+0.3	V	
Input Logic 0 (VIL)	-0.3	-	0.3×VCC	V	
Internal pull-up/ pull-down resistors	-	40	-	kΩ	

4. RF Performance

4.1. General RF Parameters

Parameter	Sub-GHz	2.4 GHz	Remark
Frequency Range	863 ~ 928 MHz	2402 ~ 2480 MHz	
Tx Power Range	-10 ~ +22 dBm	-17 ~ +12 dBm	Software configurable
Frequency Drift	< 1.5 ppm	< 1.5 ppm	

Parameter	Value	Remark
LoRa Receiving Sensitivity[1]	-127.5 dBm	Sub-GHz @ SF7, 125kHz
	-141.1 dBm	Sub-GHz @ SF12, 125kHz
	-118.4 dBm	2.4GHz @ SF7, 400kHz
	-133 dBm	2.4GHz @ SF12, 400kHz
FLRC Receiving Sensitivity[1]	-110 dBm	915MHz @ BRF = 260kbps, CR = 3/4, BWF = 300kHz
	-100.5 dBm	915MHz @ BRF = 2600 kbps, CR = 3/4, BWF = 2666 kHz
	-108.5 dBm	2.4GHz @ BRF = 260kbps, CR = 3/4, BWF = 300kHz
	-99 dBm	2.4GHz @ BRF = 2600kbps, CR = 3/4, BWF = 2666kHz
Harmonic Noise	-	490MHz @ 120kHz
		868MHz @ 120kHz
		915MHz @ 100kHz
NOTE: [1] The sensitivity values are referenced to the signal generator output; cable loss is not compensated in the raw data. The approximate cable loss is 0.7 dB. Condition: PER ≤ 10 %, RxBoosted ON.		

4.2. Power Consumption

4.2.1. LoRa Power Specifications

- Sub-GHz Transmission Power Consumption

868 MHz		915 MHz		490 MHz	
Tx Power (dBm)	Current (mA)	Tx Power (dBm)	Current (mA)	Tx Power (dBm)	Current (mA)
-10	7.8	-10	7.8	-	-
0	9.9	0	10.1	-	-
+10	19.4	+10	19.7	-	-
+15	38.5	+15	38.5	-	-
+17	52.3	+17	53.9	-	-
+18	61.8	+18	63.4	-	-
+19	76.0	+19	77.8	-	-
+20	92.5	+20	93.4	-	-
+21	109.8	+21	111.2	-	-
+22	116.0	+22	119.4	-	-
NOTE: Tested at 25 ℃ ambient.					

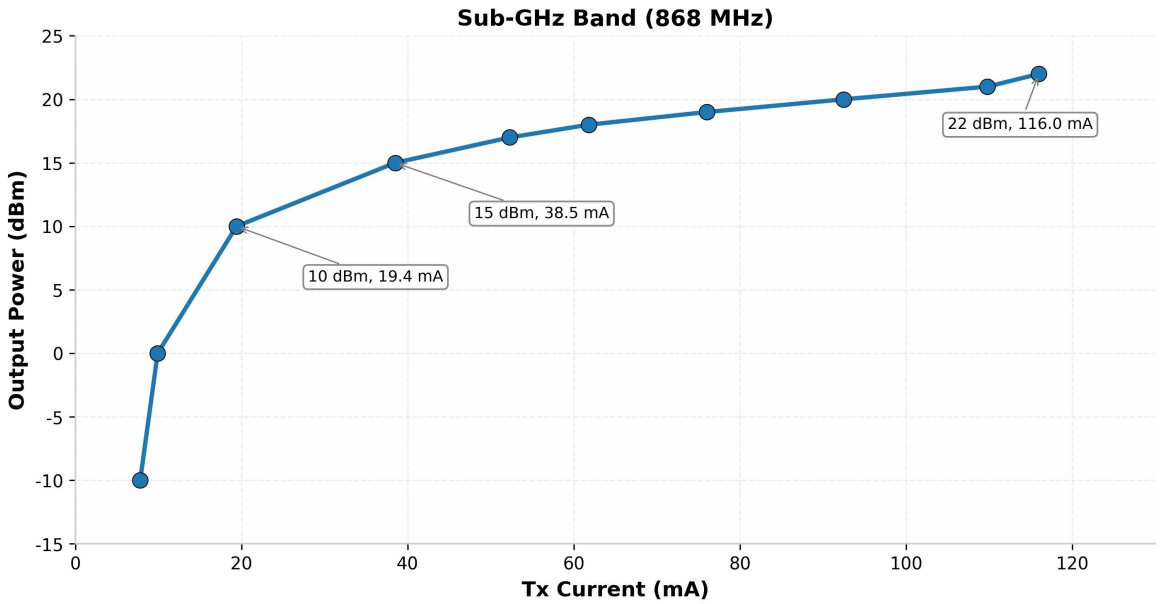

Figure 4 Output Power VS Transmission Current (868MHz)

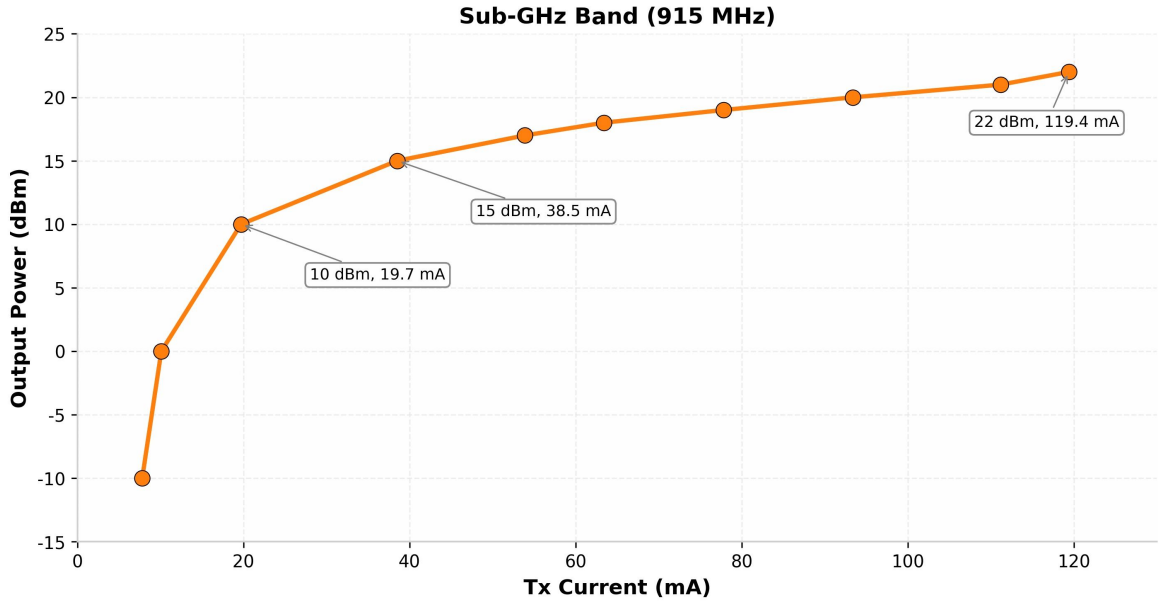

Figure 5 Output Power VS Transmission Current (915MHz)

- 2.4GHz Transmission Power Consumption

Tx Power (dBm)	Current (mA)
-17	9.7
-13	10.2
-10	10.8
-5	12.0
-3	12.6
0	13.6
+3	15.3
+5	17.0
+10	22.9
+12	28.4
NOTE: Tested at 25 ℃ ambient.	

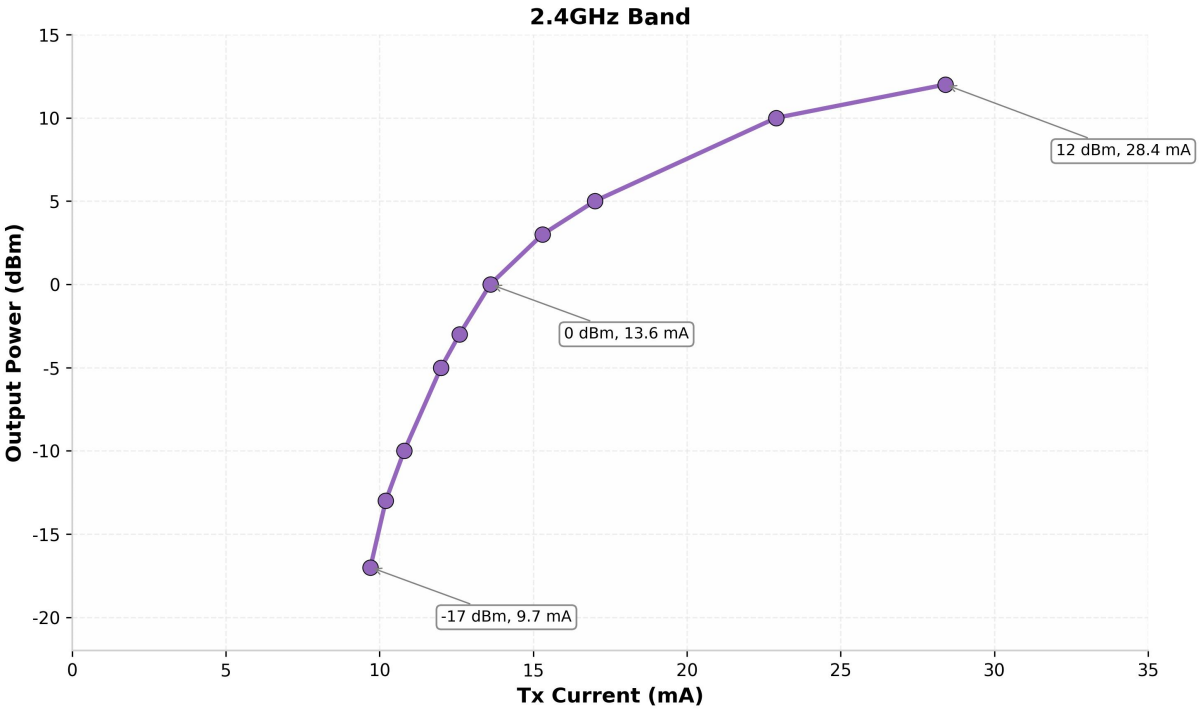

Figure 6 Output Power VS Transmission Current (2.4GHz)

4.2.2. FLRC Power Specifications

- 260kbps Bit Rate Transmission Power Consumption

915MHz		2.4GHz	
Tx Power (dBm)	Current (mA)	Tx Power (dBm)	Current (mA)
-10	8.93	-17	10.13
-5	9.69	-14	11.07
-3	9.82	-11	11.53
+2	10.87	-7	11.54
+4	12.30	-4	12.77
+8	17.04	-2	13.57
+12	25.26	0	14.38
+16	46.82	+5	17.30
+19	75.91	+8	19.51
+22	117.53	+12	27.58

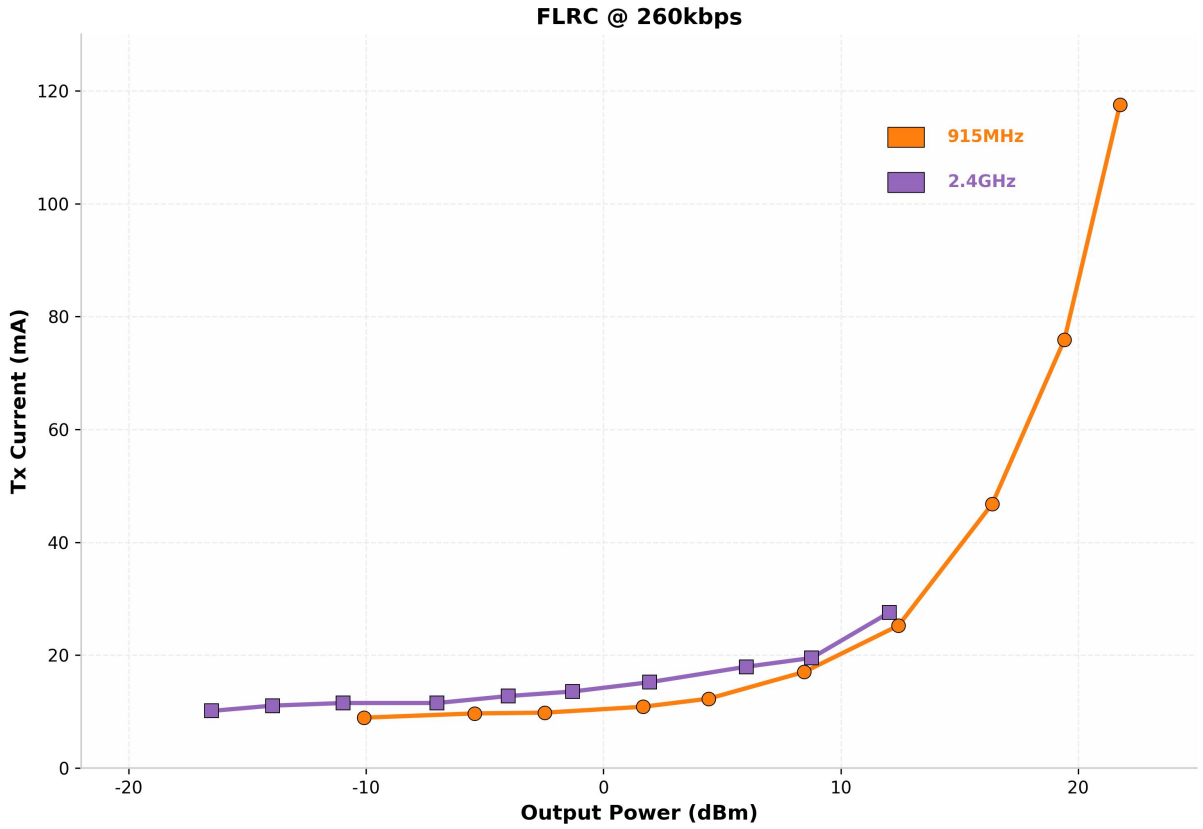

Figure 7 Output Power VS Transmission Current (FLRC @ 260kbps)

- 2600kbps Bit Rate Transmission Power Consumption

915MHz		2.4GHz	
Tx Power (dBm)	Current (mA)	Tx Power (dBm)	Current (mA)
-10	2.60	-17	2.77
-5	2.72	-14	2.81
-3	2.73	-11	2.84
+2	2.91	-9	2.93
+4	3.05	-5	3.02
+7	3.26	-2	3.13
+10	3.76	0	3.17
+15	5.50	+5	3.45
+18	7.62	+8	3.64
+22	12.07	+12	4.40

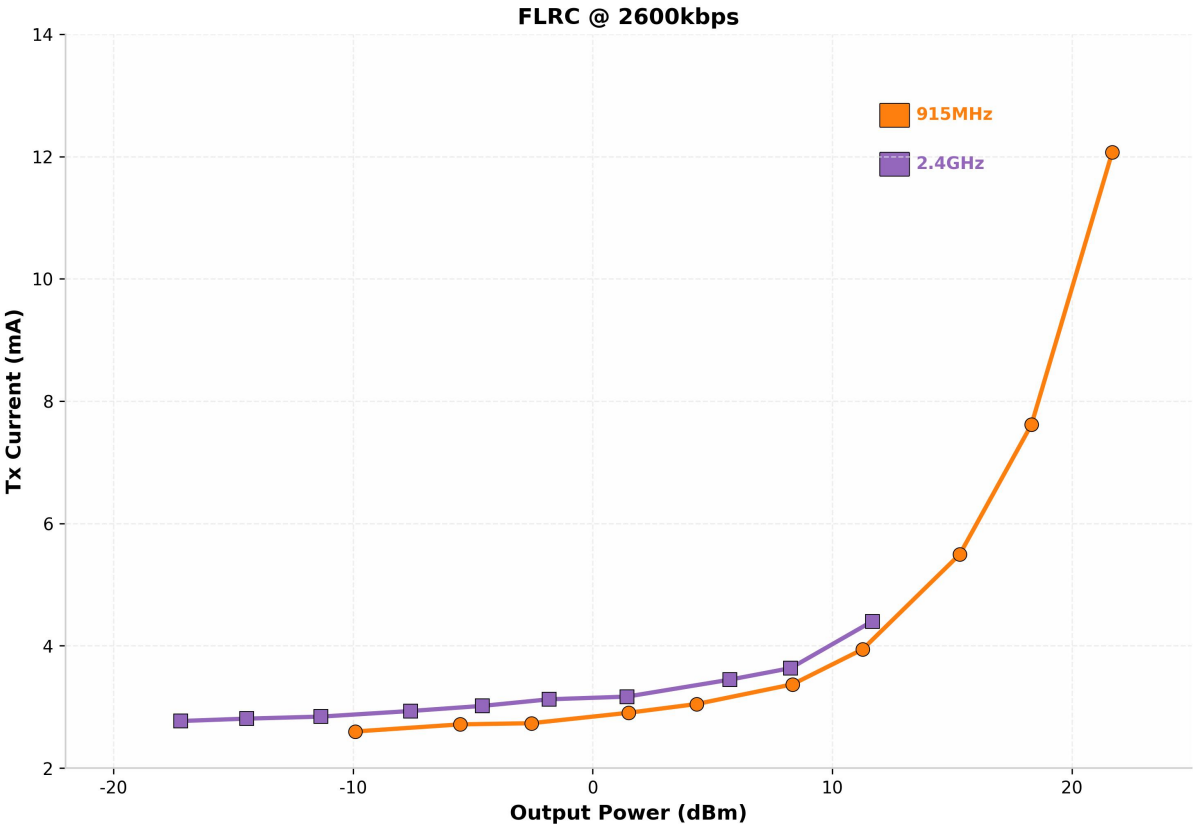

Figure 8 Output Power VS Transmission Current (FLRC @ 2600kbps)

5. Application Information

5.1. Mechanism Dimension (Unit: mm)

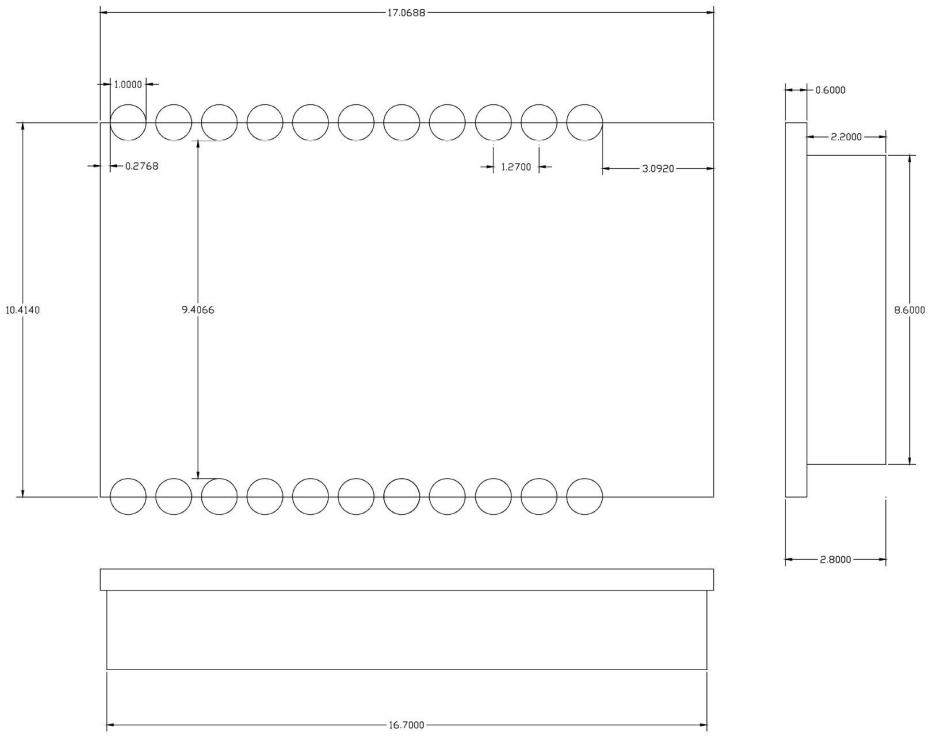

Figure 9 Mechanical Drawing

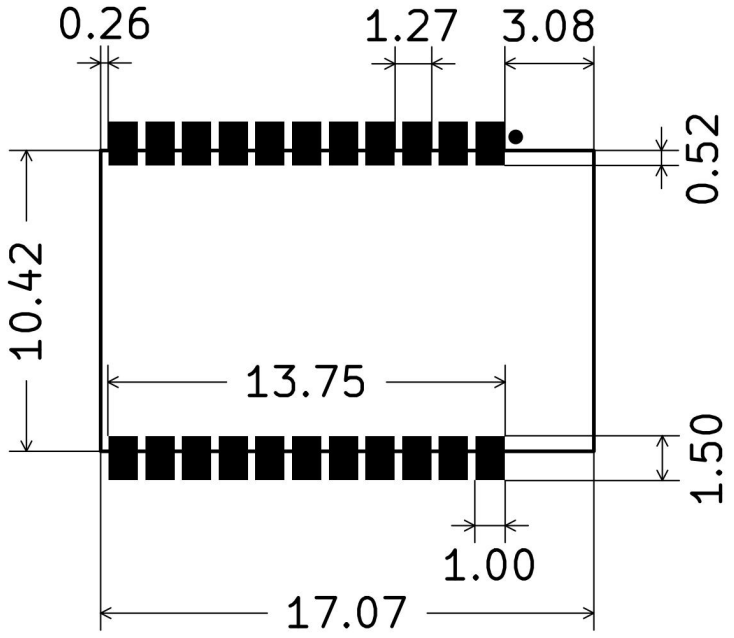

Figure 10 Footprint Drawing

5.2. Reference Design

The following is a typical reference design using the Wio-LR2021 module:

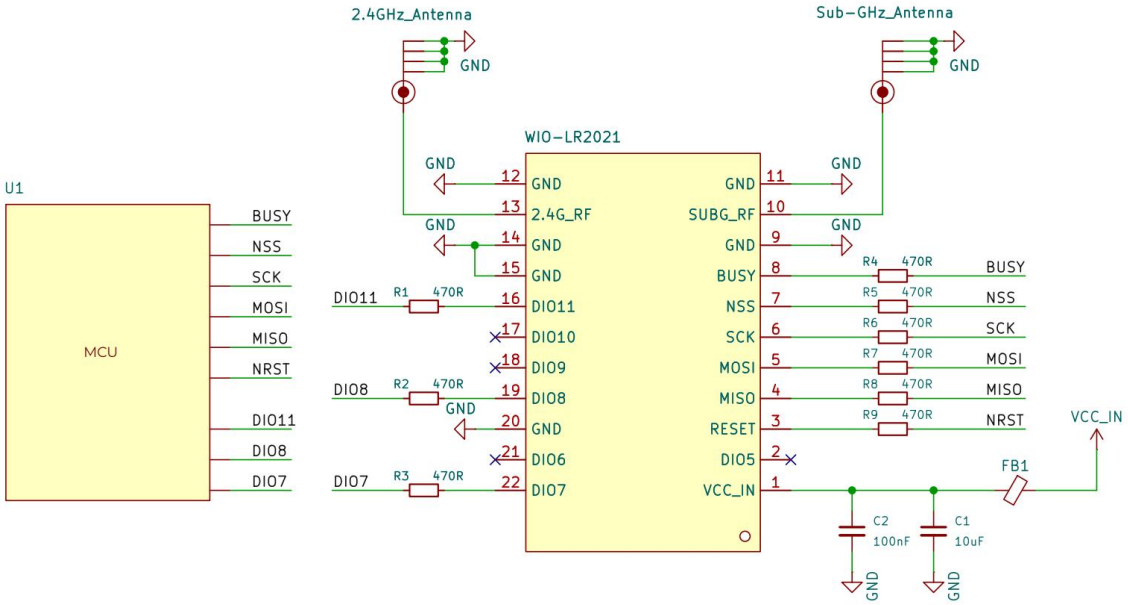

Figure 11 Reference Design Based on Wio-LR2021

PCB Layout Notice:

1. SPI interface and DIOs between host MCU and Wio-LR2021 must be connected via a 470 Ω resistor to suppress high-frequency harmonics on signal lines. All 470 Ω resistors should be placed as close as possible to the Wio-LR2021 module.

RF Trace Design Guidelines:

1. The output impedance of the RF channels are both 50 Ω and compatible with IPEX and SMT connectors.

1. The RF trace impedance specifications are based on a standard 4-layer FR-4 PCB construction with 1 oz (35 µm) outer-layer copper and Prepreg 2116 (~0.10 mm / 4 mil).

2. To maintain a 50 Ω characteristic impedance (±10%) for the microstrip traces routing from the module's RF pinout to the IPEX/SMA connectors, a trace width of (0.152 mm / 6 mil) is recommended.

3. Place stitching vias at ≤1 mm intervals along both sides of the RF trace to suppress parasitic coupling and ensure return path integrity.

5.3. Host Interface Timing

5.3.1. SPI Timing Specification

The Wio-LR2021 module operates as an SPI subordinate device. The module SPI port conforms to **Mode 0 (CPOL = 0, CPHA = 0)**. The host must configure its SPI controller accordingly. MISO is high-impedance when NSS is de-asserted (HIGH). The SPI runs on the external SCK clock with a maximum frequency of **16MHz**.

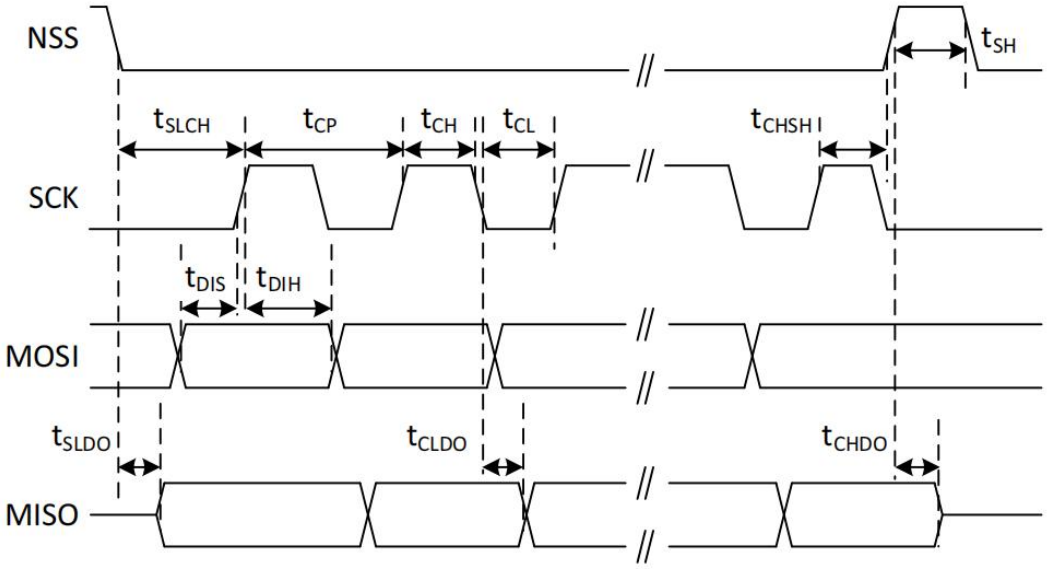

Figure 12 SPI Timing Diagram

- SPI Timing Requirements

Symbol	Description	Min	Max	Unit
t_{SH}	NSS high time (bus release)	125	-	ns
t_{SLCH}	NSS falling edge to first SCK rising edge (setup)	31.25	-	ns
t_{CP}	SCK clock period	61.5	-	ns
t_{CH}	SCK high time	31.25	-	ns
t_{CL}	SCK low time	31.25	-	ns
t_{CHSH}	Last SCK falling edge to NSS rising edge (hold)	65	-	ns
t_{SLDO}	MISO valid delay from NSS falling edge	1	10	ns
t_{DIS}	MOSI data setup time	15	-	ns
t_{DIH}	MOSI data hold time	15	-	ns
t_{CLDO}	MISO valid delay from SCK falling edge	-	18	ns

t_{CHDO}	SCK rising edge to MISO data output time	-	10	ns

NOTE:

1. The module SPI interface does not support continuous frame mode (NSS kept low across multiple opcodes). NSS must be released (HIGH) for t_{SH} minimum between each command frame.

5.3.2. BUSY Signal Specification

The BUSY signal (module pin 8) provides hardware flow control between the host and the module radio controller:

- When the BUSY line is held LOW, it indicates that the radio is ready to accept a command from the host controller.
- The BUSY pin will be automatically pulled HIGH on the falling edge of NSS.
- Once the chip has finished processing the command, the BUSY line will be released(LOW), indicating that the chip has entered a stable mode and is ready to accept another command.
- In FS mode, BUSY goes LOW when the PLL is locked.
- In Rx mode, BUSY goes LOW as soon as the chip is ready to receive data.
- In Tx mode, BUSY goes LOW when the PA has ramped-up and transmission of preamble starts.
- When triggered by a DIO pin, the BUSY signal will not be raised.

NOTE:

For exhaustive SPI timing parameters, command opcodes, and host interface protocol details, please refer to the **Semtech LR2021 Datasheet**.

Documentation: Semtech LoRa Plus LR2021 Datasheet

6. Production

6.1 Reflow Soldering Parameters

The Wio-LR2021 module is designed for easy integration into production processes, including soldering onto a PCB using reflow soldering techniques. A critical factor is that users must select the appropriate solder paste and ensure it meets the temperature requirements during the reflow process.

Note: During reflow soldering, the module temperature must not exceed 260°C, and the duration in the reflow zone should not exceed 30 seconds.

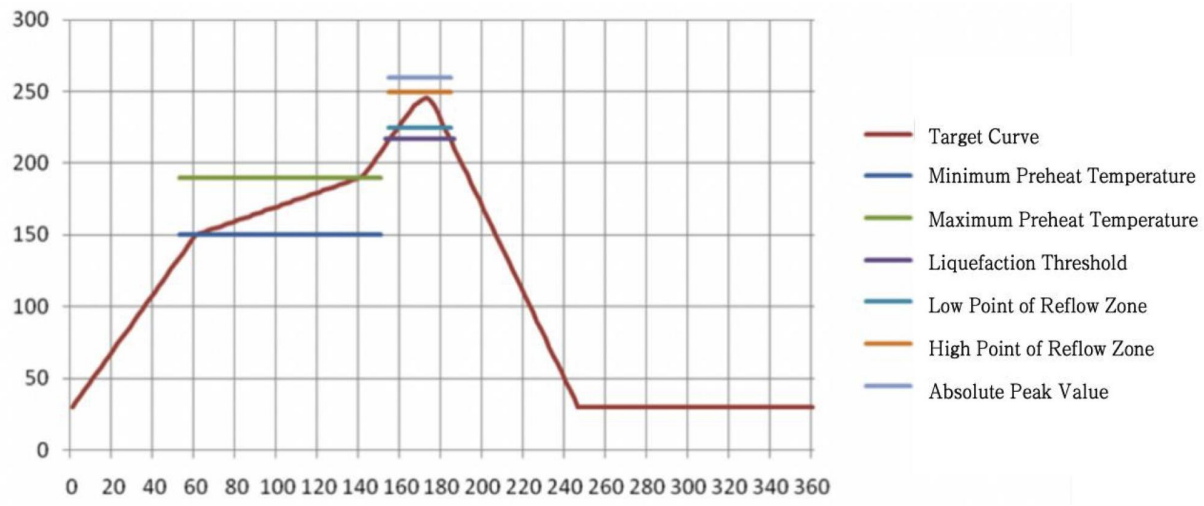

Figure 13 Soldering Profile

Item	Value	Unit
Heating Rate	1~3	℃/s
Cooling Rate	2~4	℃/s
Heating Rate of Preheating Zone	0.5~1	℃/s
Minimum Time of Preheating Zone	70	s
Maximum Time of Preheating Zone	120	s
Minimum Temperature of Preheating Zone	150	℃
Maximum Temperature of Preheating Zone	190	℃
Minimum Residence Time of Solder Paste (above liquefaction temperature)	50	s
Maximum Residence Time of Solder Paste (above liquefaction temperature)	70	s

Residence Time in Reflux Zone	30	s
Maximum Residence Time at Peak Temperature	5	s
Recommand Liquefaction Zone Threshold	218	℃
Low Point Temperature of Reflux Zone	240	℃
High Point Temperature of Reflux Zone	250	℃
Peak Temperature	260	℃

6.2 Tape & Reel

The Wio-LR2021 module can be supplied taped and reeled in quantities of 1236 per reel. The tape and reel packaging follows industry standards with the following dimensions and specifications:

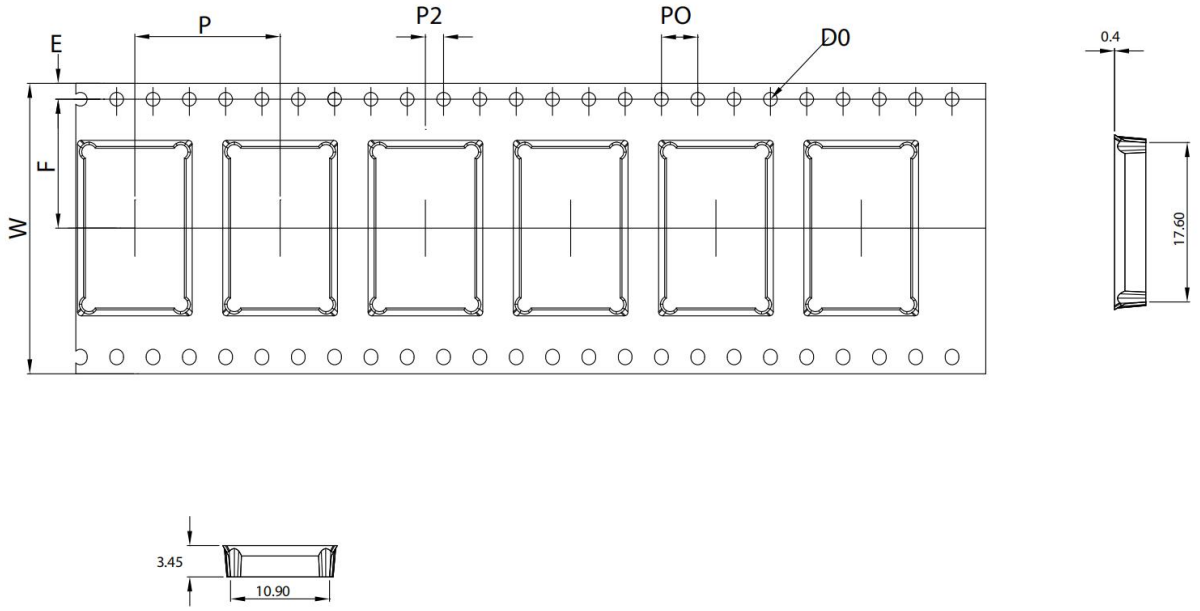

Figure 14 Tape and Reel Dimension

Tape & Reel Dimensions							
W	32.0±0.30	P	16.0±0.10	A	10.9±0.10	B0	17.6±0.10
S0	/	P0	4.0±0.10	A1		B1	
E	1.75±0.10	P2	2.0±0.10	A2		B2	
F	14.2±0.10	D0	Ø1.5	K0	3.45±0.10		
T	0.4±0.05	D1		K1			
NOTE: 1. Dimensions comply with the EIA-481-D standard.							

2. All dimensions in millimeters. Cumulative tolerance for 10 sprocket hole pitches: ±0.20 mm.
3. Material: Conductive polystyrene.

7. Version

V1.0	2026-05-14	First Release	David Du

