FGH100M Hardware Design

Short-Range Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-03-22	Paul YU/James XIONG/ Adam ZENG	Creation of the document
1.0	2024-04-29	Paul YU/James XIONG/ Mark HUANG	First official release

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1 Introduction

This document defines the FGH100M and describes its air interfaces and hardware interfaces which are connected with your applications. With this document, you can quickly understand module interface specifications, RF performance, electrical and mechanical details, as well as other related information of the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

FGH100M is a long-range and low-power Wi-Fi HaLow module compliant with IEEE 802.11ah Wi-Fi standard. It operates in Sub-1 GHz frequency band, features 32.5 Mbps maximum transmission rate [1] and provides an SDIO 2.0 interface for Wi-Fi application.

It is an SMD module with compact packaging. Related information is listed in the table below:

Table 2: Basic Information

FGH100M	
Packaging type	LGA
Pin counts	40
Dimensions	(13.0 ±0.2) mm × (13.0 ±0.2) mm × (2.2 ±0.2) mm
Weight	Approx. 0.72 g

[1] Optional. Different models of the module correspond to different physical layer maximum transmission rates. For details, please consult Quectel Technical Support.

2.1. Key Features

Table 3: Key Features

Basic Information	
Protocol and Standards	● Wi-Fi Protocol: IEEE 802.11ah ● All hardware components are fully compliant with EU RoHS directive
Power Supplies	**VBAT Power Supply:** ● 3.0–3.6 V ● Typ.: 3.3 V **VDD_FEM Power Supply:** ● 3.0–3.6 V ● Typ.: 3.3 V **VDD_IO Power Supply [2]:** ● 1.8–3.6 V ● Typ.: 3.3 V
Temperature Ranges	● Operating temperature: -30 to +85 °C [3] ● Extended temperature: -40 to +85 °C ● Storage temperature: -40 to +95 °C
EVB Kit	FGH100M-M.2, RK3568-WF EVB [4]
RF Antenna Interface	
Antenna Interface	● ANT_WIFI ● 50 Ω characteristic impedance
Application Interface	
Application Interfaces	SDIO 2.0, JTAG

[2] The VDD_IO power supply should not exceed VBAT.
[3] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module's indicators comply with IEEE requirements.
[4] For more details about the EVB, see ***document [1]***.

2.2. Functional Diagram

The functional diagram illustrates the following major functional parts:

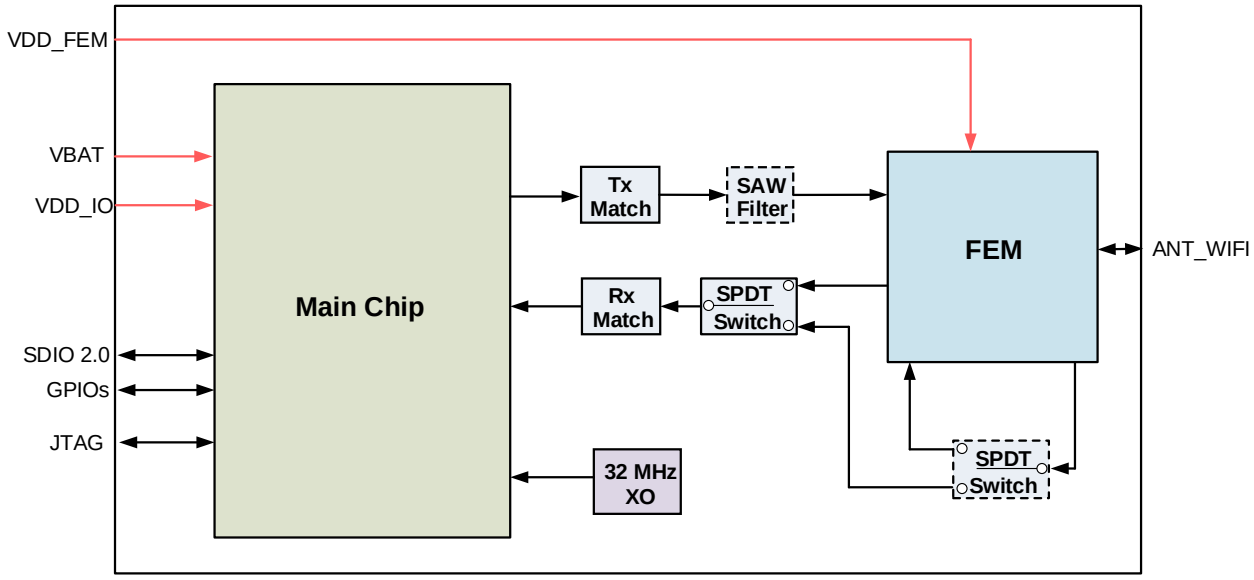


Figure 1: Functional Diagram

3 RF Performances

3.1. Wi-Fi Performances

Table 4: Wi-Fi Performances

Operating Frequency				
Sub-1 GHz: 850–950 MHz				
Modulation				
OFDM, BPSK, QPSK, 16QAM, 64QAM				
Operating Mode				
● AP ● STA				
Encryption Mode				
AES, SHA-256, SHA-384, SHA-512, WPA3, OWE				
Transmission Data Rate				
● 1 MHz: MCS 0–MCS 7, MCS 10 ● 2 MHz: MCS 0–MCS 7 ● 4 MHz: MCS 0–MCS 7 ● 8 MHz: MCS 0–MCS 7				
Condition (VBAT = 3.3 V, VDD_FEM = 3.3 V, VDD_IO = 1.8 V; Temp. = 25 °C)		**EVM**	**Typ.; Unit: dBm; Tolerance: ±2 dB**	
			Transmitting Power	**Receiver Sensitivity**
Sub-1 GHz	802.11ah, 1 MHz @ MCS 0	≤ -5 dB	21	-108
	802.11ah, 2 MHz @ MCS 0		20	-104
	802.11ah, 4 MHz @ MCS 0	≤ -5 dB	20	-102
	802.11ah, 8 MHz @ MCS 0	≤ -5 dB	20	-98

	802.11ah, 1 MHz @ MCS 7	≤ -27 dB	17	-88
	802.11ah, 2 MHz @ MCS 7	≤ -27 dB	17	-84
	802.11ah, 4 MHz @ MCS 7	≤ -27 dB	17	-82
	802.11ah, 8 MHz @ MCS 7	≤ -27 dB	17	-77
	802.11ah, 1 MHz @ MCS 10	≤ -5 dB	21	-109

NOTE

There are differences in the RF circuit design between different models of the module. ***Table 4*** only shows the RF data of one model. For the complete RF data of the module, see the module specification. For more details, please contact Quectel Technical Support.

4 Application Interfaces

4.1. Pin Assignment

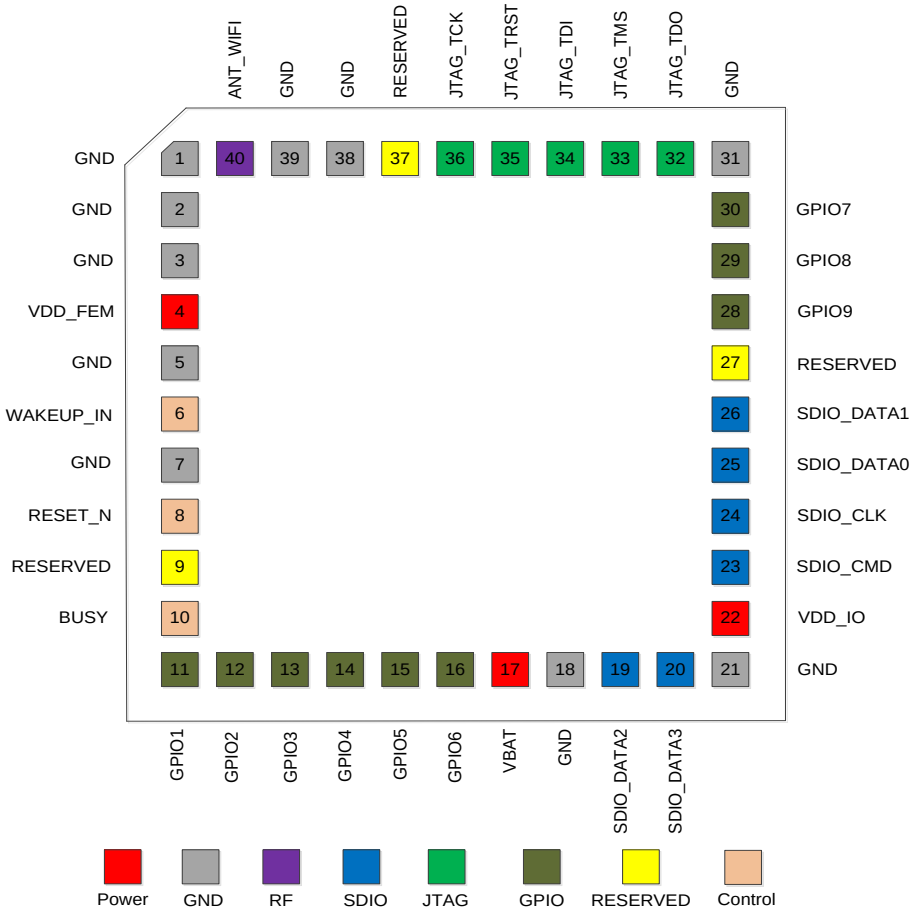


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins unconnected.
2. All GND pins should be connected to ground.
3. Keep all unused GPIO pins (GPIO1–GPIO9) pulled down to GND via 10 kΩ resistors.
4. All unused digital I/O pins must be pulled up or down to ensure they are connected, otherwise more leakage current in VDD_IO power supply will be generated.

4.2. Pin Description

Table 5: Parameter Definition

Parameter	Description
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply and GND Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	17	PI	Power supply for the module	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	It must be provided with sufficient current of at least 0.5 A.
VDD_FEM	4	PI	Power supply for the FEM	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	
VDD_IO	22	PI	Power supply for the I/O pins	Vmax = 3.6 V Vmin = 1.8 V	

				Vnom = 3.3 V	
GND	1–3, 5, 7, 18, 21, 31, 38, 39				
Wi-Fi Application Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_CLK	24	DI	SDIO clock	VDD_IO	SDIO 2.0 compliant. **SDIO mode**: Require differential impedance of 50 Ω. Reserve 10–100 kΩ resistors to pull each of them up to VDD_IO. **SPI mode (Slave mode only):** Switch to SPI mode by controlling SDIO_DATA3 and SDIO_CMD. For details, please consult Quectel Technical Support.
			SPI clock		
SDIO_CMD	23	DIO	SDIO command		
		DI	SPI master-out slave-in		
SDIO_DATA0	25	DIO	SDIO data bit 0		
		DO	SPI master-in slave-out		
SDIO_DATA1	26	DIO	SDIO data bit 1		
		DI	SPI interrupt		
SDIO_DATA3	20	DIO	SDIO data bit 3		
		DI	SPI chip select		
SDIO_DATA2	19	DIO	SDIO data bit 2		
			-		Pulled up to VDD_IO via a 47 kΩ resistor in SPI mode.
JTAG Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
JTAG_TDO	32	DO	JTAG test data out	VDD_IO	Externally pulled down to GND with 10 kΩ resistors.
JTAG_TMS	33	DI	JTAG test mode select		
JTAG_TDI	34	DI	JTAG test data in		
JTAG_TCK	36	DI	JTAG test clock		
JTAG_TRST	35	DI	JTAG test reset		Pulled down to GND with a 10 kΩ resistor inside the module.

GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	11	DIO	General-purpose input/output	VDD_IO	If unused, pull them down to GND with 10 kΩ resistors.
GPIO2	12	DIO	General-purpose input/output		
GPIO3	13	DIO	General-purpose input/output		
GPIO4	14	DIO	General-purpose input/output		
GPIO5	15	DIO	General-purpose input/output		
GPIO6	16	DIO	General-purpose input/output		
GPIO7	30	DIO	General-purpose input/output		
GPIO8	29	DIO	General-purpose input/output		
GPIO9	28	DIO	General-purpose input/output		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_WIFI	40	AIO	Wi-Fi antenna interface		50 Ω characteristic impedance.
Control Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BUSY	10	DO	Power saving	VDD_IO	Externally pulled down to GND with 10 kΩ resistors. If power-saving mode is not used, the pin can not be connected to the host.
WAKEUP_IN	6	DI	Wake up the module	VBAT	If power-saving mode is not used, pull it up to VBAT through a 10 kΩ resistor.
RESET_N	8	DI	Reset the module		Active low.
RESERVED Pins					

Pin Name	Pin No.	Comment
RESERVED	9, 27, 37	Keep them open.

4.3. Power Supply

The module is powered by VBAT, and the power supply chip for VBAT should provide sufficient current of 0.5 A at least. For better power supply performance, it is recommended to parallel a 10 μF decoupling capacitor and 100 nF filter capacitors near the module's VBAT pin. C3 is reserved for debugging and not mounted by default. In addition, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VDD_FEM supplies power for the FEM, and VDD_IO supplies power for the I/O pins of the module. Both power supply designs can be consistent with VBAT's. The circuit reference design is shown below:

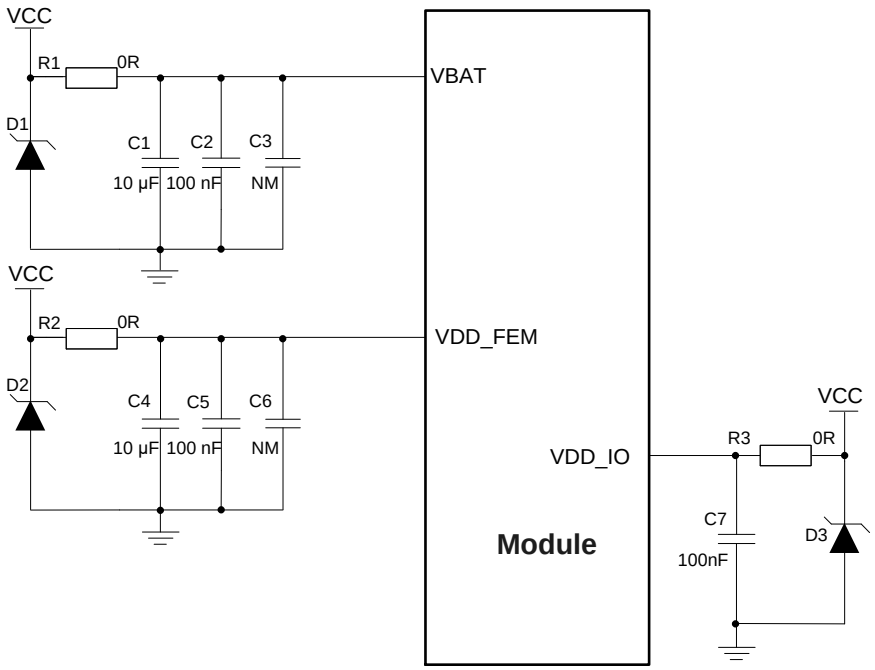


Figure 3: Reference Circuit of Power Supply

VBAT, VDD_FEM and VDD_IO do not have strict power-on sequence requirements, but the voltage of VDD_IO should not exceed VBAT. In addition, it is necessary to confirm that the level of module power supply interfaces corresponds to the host level.

4.4. Wi-Fi Application Interface

The module provides one SDIO 2.0 interface for Wi-Fi applications. At the same time, the power saving mode can be enabled or disabled by controlling the WAKEUP_IN and BUSY pins.

- If power saving mode is used, a GPIO of the host is needed to be set as a CMOS input pin to receive the BUSY signal from the pin 10 (BUSY) of the module.
- If power-saving mode is not used, WAKEUP_IN of the module should be pulled up to VBAT through a 10 kΩ resistor. For more details, please contact Quectel Technical Support.

The Wi-Fi application interface connection between the module and the host in different modes is shown below:

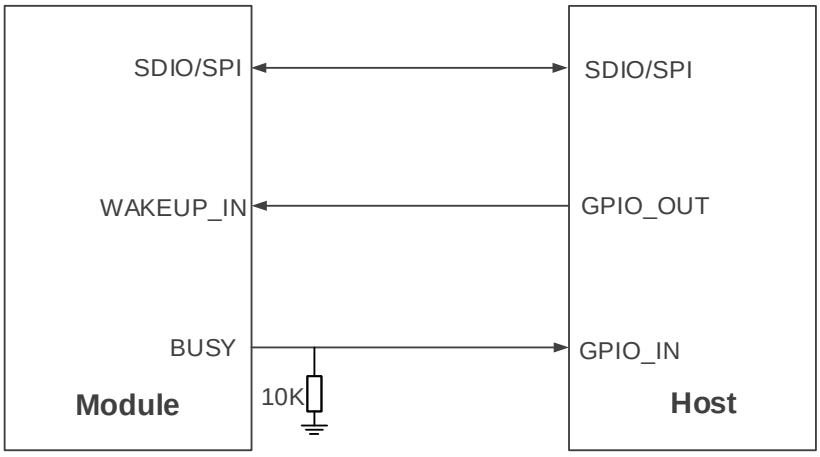


Figure 4: Wi-Fi Application Interface Connection (Power-Saving Mode)

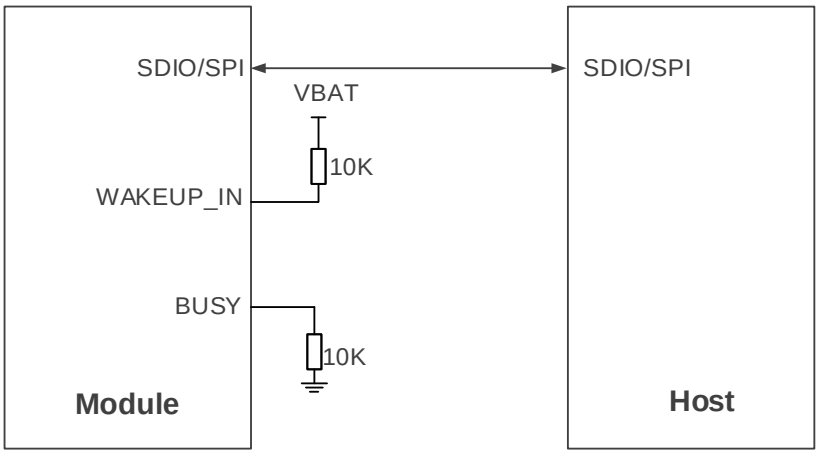


Figure 5: Wi-Fi Application Interface Connection (Non-Power-Saving Mode)

4.4.1. SDIO Interface

In SDIO mode, SDIO interface connection between the module and the host is illustrated in the following figure.

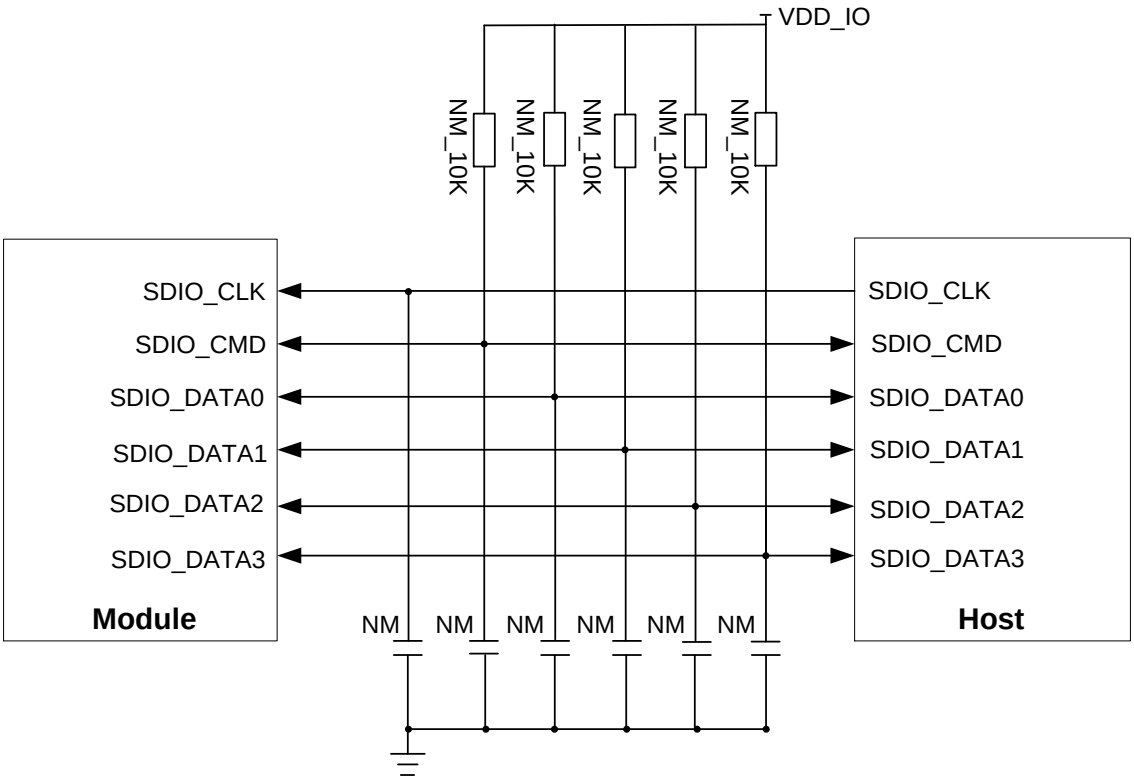


Figure 6: SDIO Interface Connection

To ensure compliance of interface design with the SDIO 2.0 specification, it is recommended to adopt the following principles:

- To avoid jitter of bus, reserve pull-up resistors with value of 10–100 kΩ (recommended value is 10 kΩ) on the SDIO_CMD, SDIO_DATA[0:3] and SDIO_CLK signal traces, and pull them up to VDD_IO of the module.
- The impedance of SDIO signal traces is 50 Ω ±10 %. Route the SDIO traces in inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock signals and DC-DC signals.
- The distance between SDIO signals and other signals must be greater than twice the trace width, and the bus load capacitance must be less than 15 pF.

The SDIO interface can be switched to SPI mode by controlling SDIO_DATA3 and SDIO_CMD. Only SPI slave mode is supported. For details, please consult Quectel Technical Support. Pull up the unused SDIO_DATA2 to VDD_IO through a 47 kΩ resistor.

Table 7: Pin Description of SDIO Interface in SPI Mode

Pin Name	Pin No.	I/O	Description
SDIO_CLK	24	DI	SPI clock
SDIO_CMD	23	DI	SPI master-out slave-in
SDIO_DATA0	25	DO	SPI master-in slave-out
SDIO_DATA1	26	DI	SPI interrupt
SDIO_DATA3	20	DI	SPI chip select

In SPI mode, SDIO interface connection between the module and the host is illustrated in the following figure.

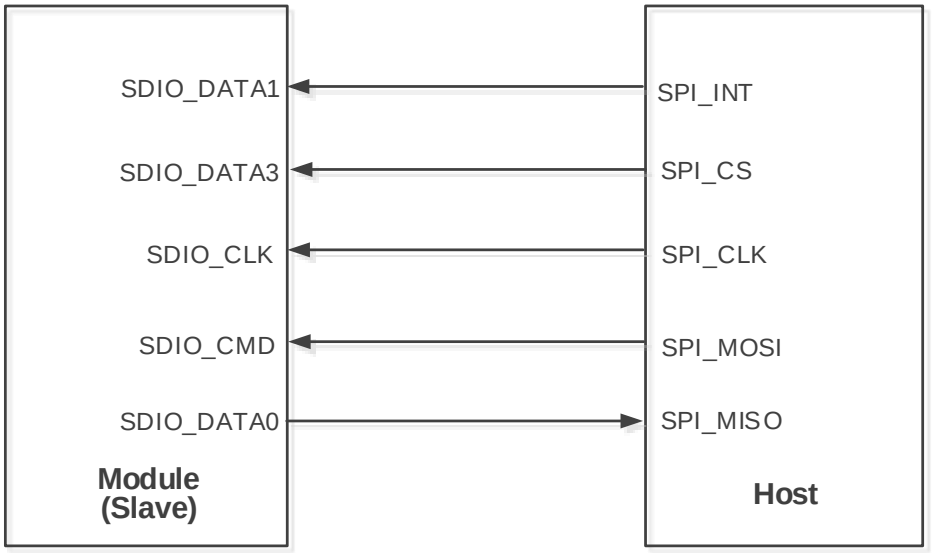


Figure 7: SDIO Interface Connection in SPI Mode

Consider the following recommendations to achieve the best throughput:

- The host must support level-triggered interrupts.
- The host must support full-duplex mode.
- If the SPI bus requires higher throughput, the host must support DMA transactions. The standard SPI interface has a transmission rate of up to 25 Mbps when the clock frequency is 50 MHz. But if the host does not support DMA transactions, the transfer rate will be significantly reduced. For example, for an SPI interface with an 8-byte DMA transaction buffer, the transfer rate may only reach 2 Mbps.

4.5. JTAG Interface

The module provides a JTAG interface for module testing. JTAG interface is only reset by JTAG_TRST. JTAG_TRST is pulled down to GND with a 10 kΩ resistor inside the module.

4.6. RF Antenna Interface

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module supports one antenna interface (ANT_WIFI). The impedance of antenna port is 50 Ω.

4.6.1. Reference Design

A reference circuit for the RF antenna interface is shown below. It is recommended to reserve a π-type matching circuit and add an ESD protection component for better RF performance. Reserved matching components (R1, C1, C2, and D1) shall be placed as close to the antenna as possible. C1, C2 and D1 are not mounted by default. The parasitic capacitance of TVS should be less than 0.05 pF and R1 is recommended to be 0 Ω.

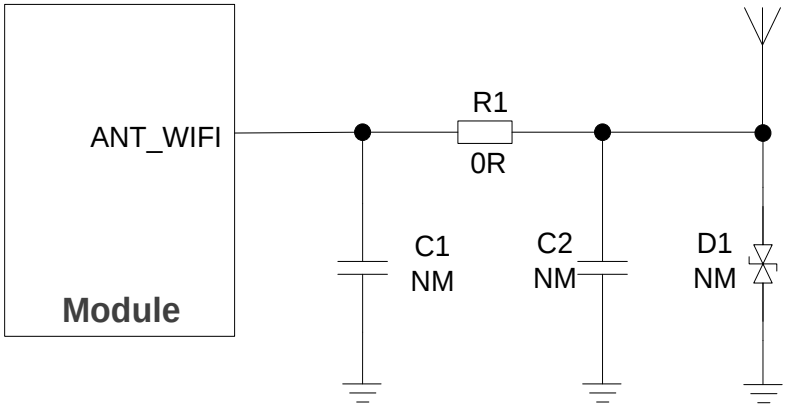


Figure 8: Reference Circuit for RF Antenna Interface

4.6.2. Requirements for Antenna Design

Table 8: Requirements for Antenna Design

Parameter	Requirement [5]
Frequency Range (MHz)	850–950
Cable Insertion Loss (dB)	< 1
VSWR	≤ 2 (Typ.)
Gain (dBi)	1 (Typ.)
Max. Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

4.6.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

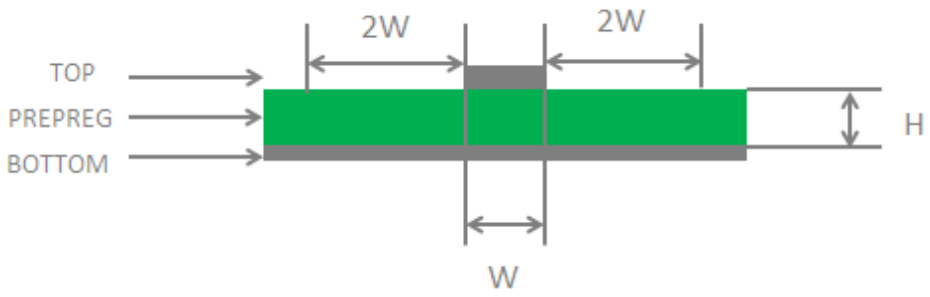


Figure 9: Microstrip Design on a 2-layer PCB

[5] For more details about the RF performances, see ***Chapter 3***.

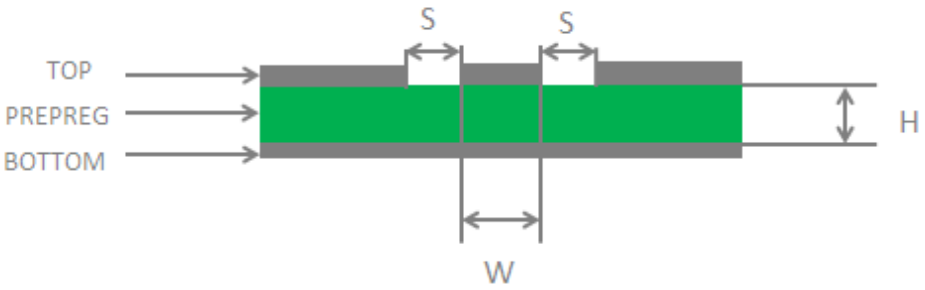


Figure 10: Coplanar Waveguide Design on a 2-layer PCB

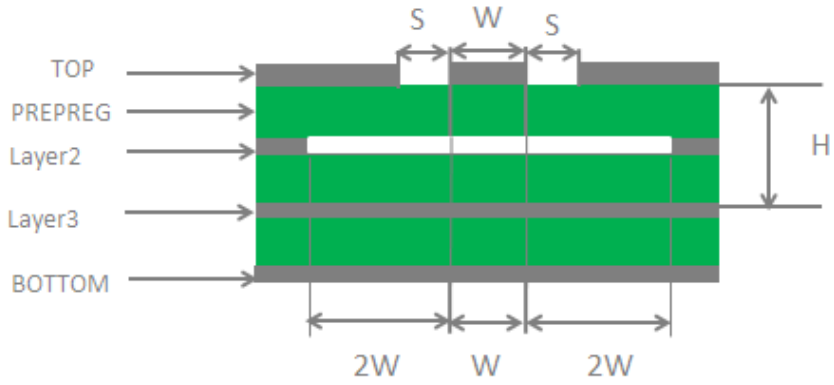


Figure 11: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

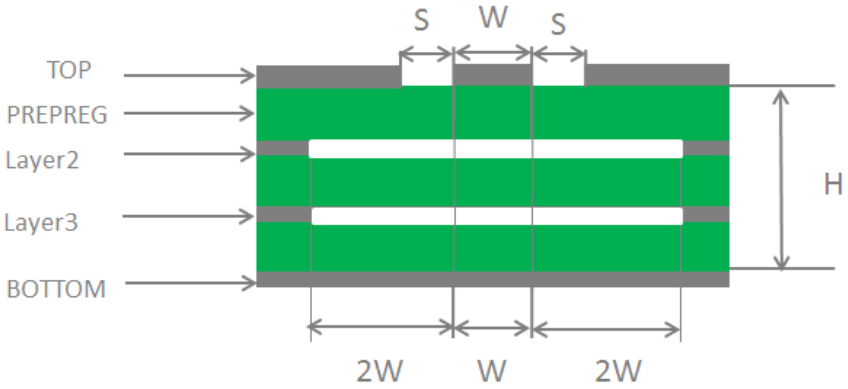


Figure 12: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The traces of RF pin should be typically routed with ground clearance and have a 50 Ω characteristic impedance.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

4.6.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

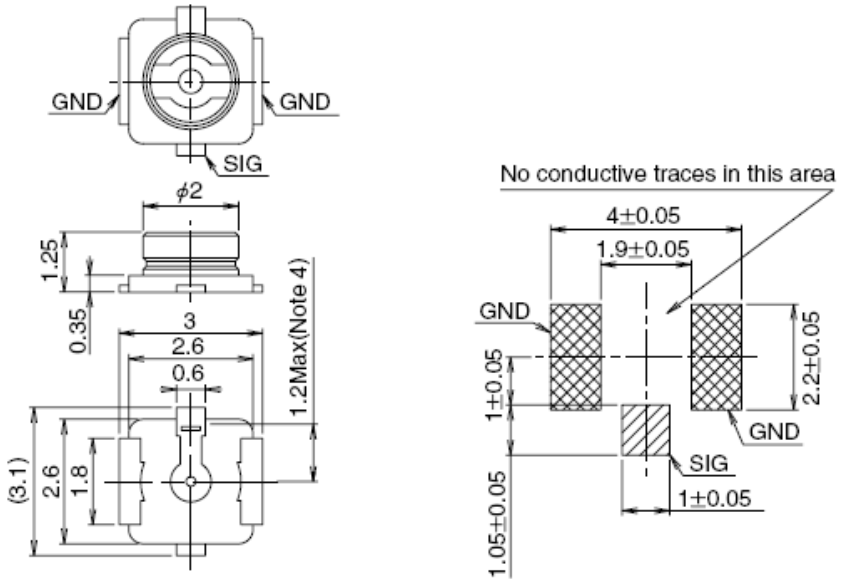


Figure 13: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

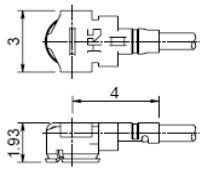
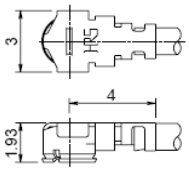
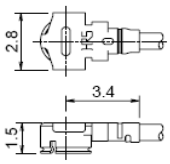
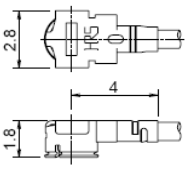
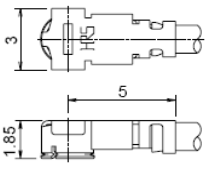
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 14: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

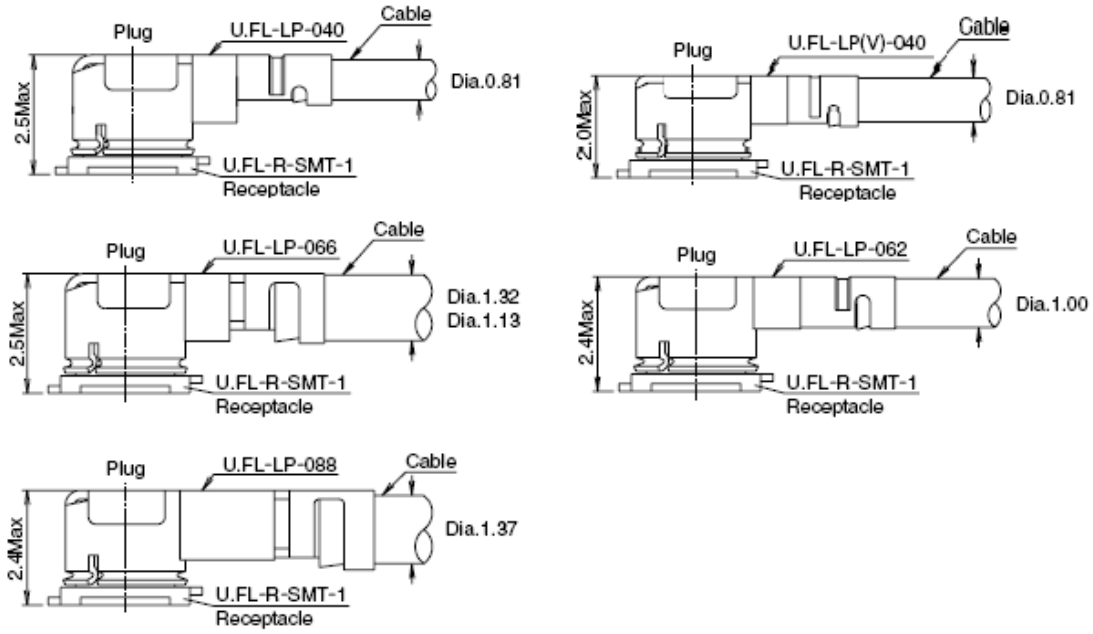


Figure 15: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	4.3
VDD_FEM	-0.3	5.5
VDD_IO	-0.3	4.3

5.2. Power Supply Ratings

Table 10: Module's Power Supply Ratings (Unit: V)

Parameter	Description	Condition	Min.	Typ.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.0	3.3	3.6
VDD_FEM	Power supply for the FEM	-	3.0	3.3	3.6
VDD_IO	Power supply for I/O pins	-	1.8	3.3	3.6

5.3. Power Consumption

Table 11: Wi-Fi Power Consumption (Typ.; Unit: mA)

Condition		I_{VDD_FEM}	I_{VBAT}
802.11ah, Tx @ 915 MHz	1 MHz @ MCS 0	120	58
	2 MHz @ MCS 0	114	60
	4 MHz @ MCS 0	104	64
	8 MHz @ MCS 0	93	72
	1 MHz @ MCS 7	72	49
	2 MHz @ MCS 7	58	48
	4 MHz @ MCS 7	45	49
	8 MHz @ MCS 7	35	54
	1 MHz @ MCS 10	119	58
802.11ah, Rx @ 915 MHz	1 MHz @ MCS 0	5	27
	2 MHz @ MCS 0	5	29
	4 MHz @ MCS 0	5	36
	8 MHz @ MCS 0	5	42
	1 MHz @ MCS 7	5	29
	2 MHz @ MCS 7	5	31
	4 MHz @ MCS 7	5	36
	8 MHz @ MCS 7	5	43
	1 MHz @ MCS 10	5	28

5.4. Digital I/O Characteristics

Table 12: VDD_IO I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VDD_IO	VDD_IO + 0.2
V_{IL}	Low-level input voltage	-0.3	0.3 × VDD_IO
V_{OH}	High-level output voltage	0.9 × VDD_IO	-
V_{OL}	Low-level output voltage	-	0.1 × VDD_IO

5.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

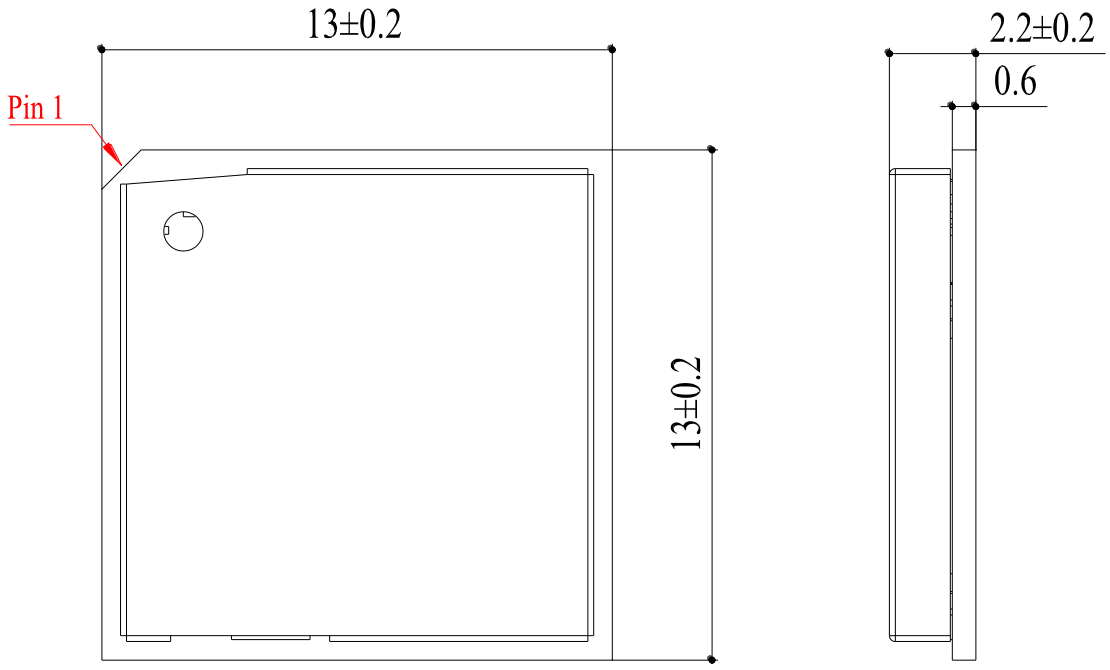


Figure 16: Top and Side Dimensions

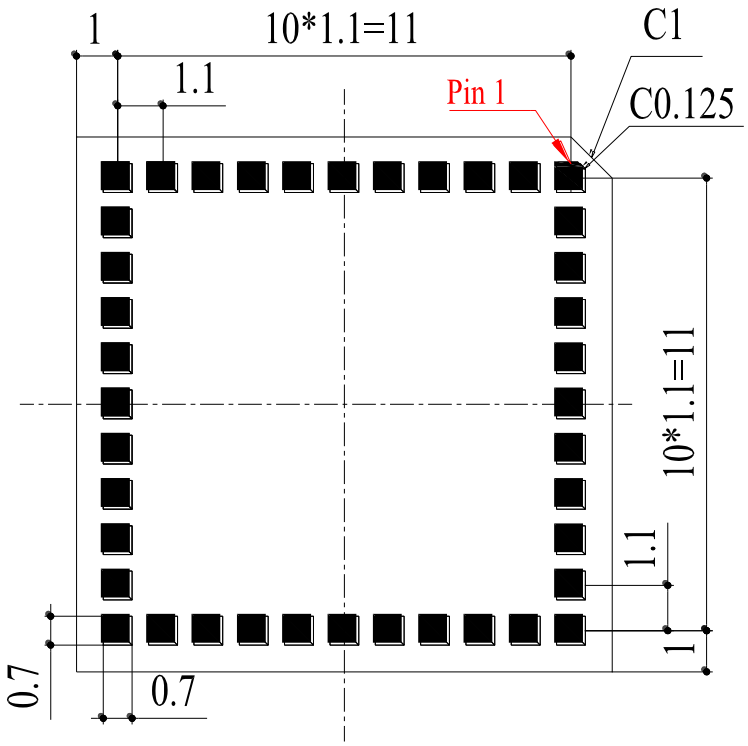


Figure 17: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to *JEITA ED-7306* standard.

6.2. Recommended Footprint

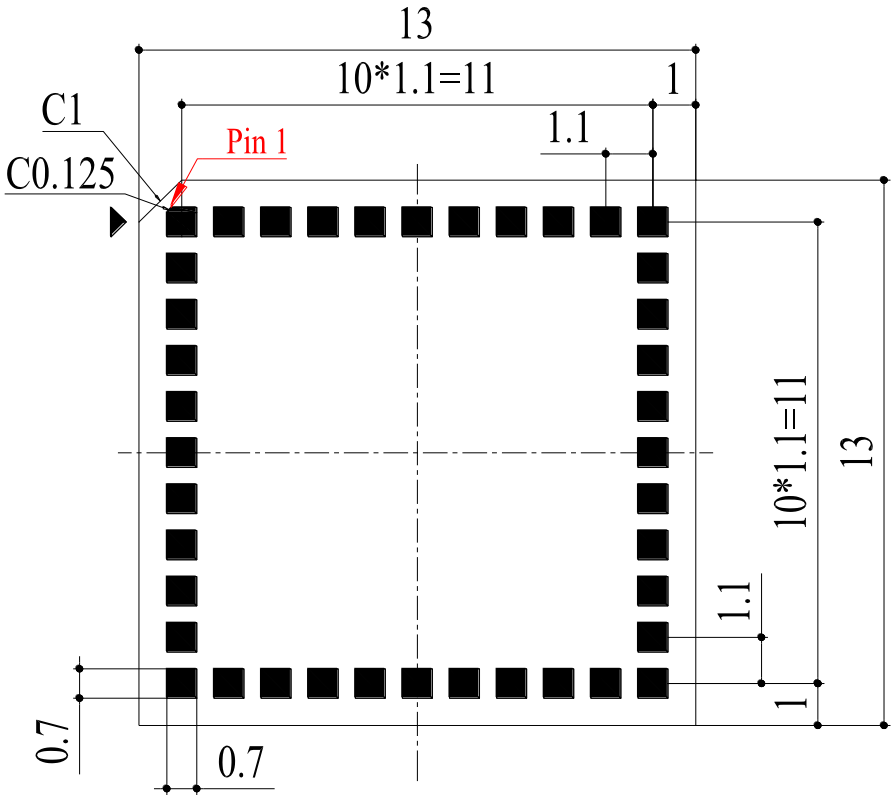


Figure 18: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

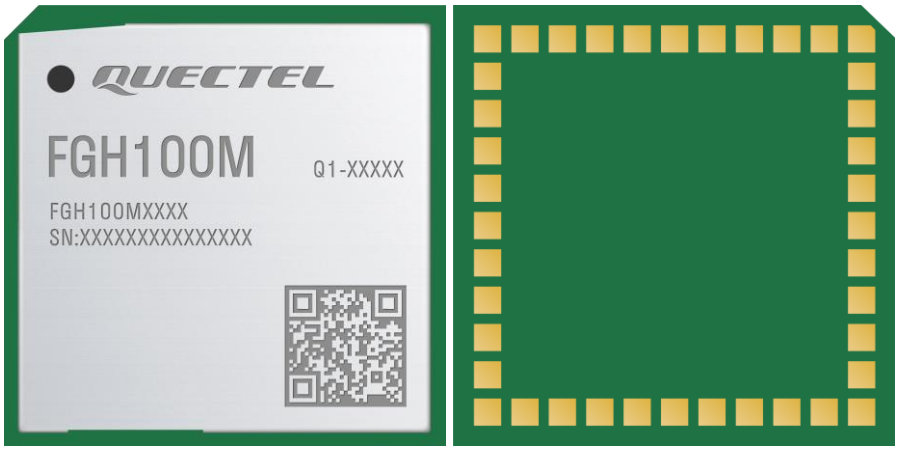


Figure 19: Top and Bottom Views

NOTE

Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[6] This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

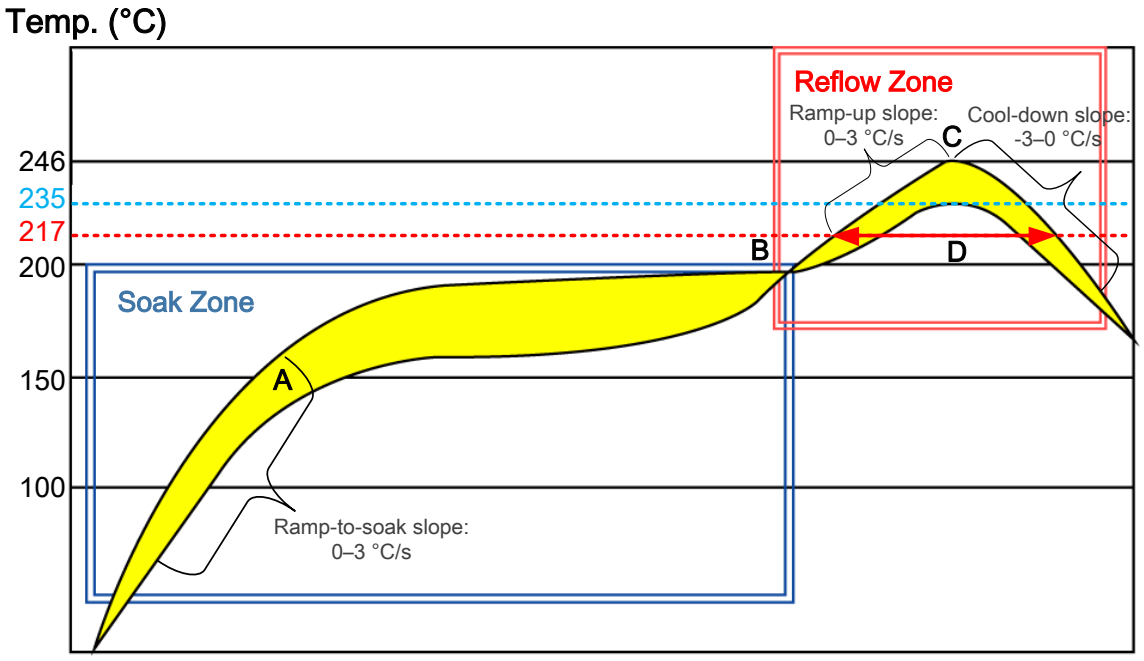


Figure 20: Recommended Reflow Soldering Thermal Profile

Table 13: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

7.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

7.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

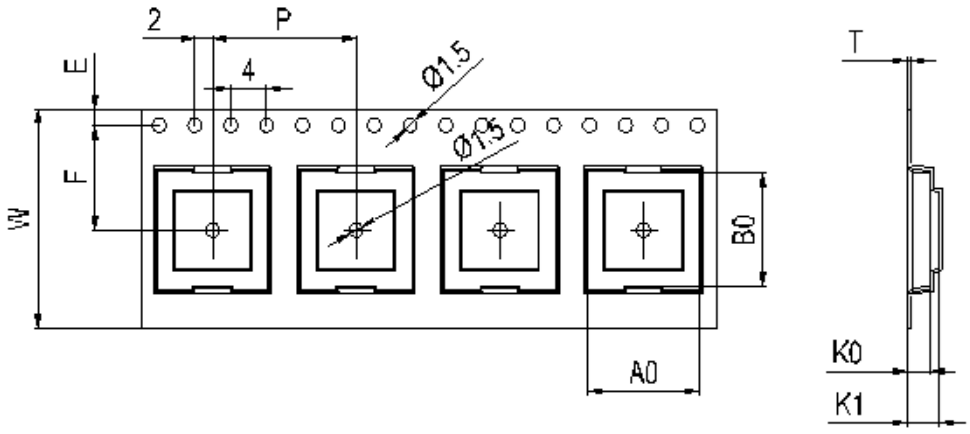


Figure 21: Carrier Tape Dimension Drawing (Unit: mm)

Table 14: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
24	20	0.4	13.4	13.4	2.95	5.6	11.5	1.75

7.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

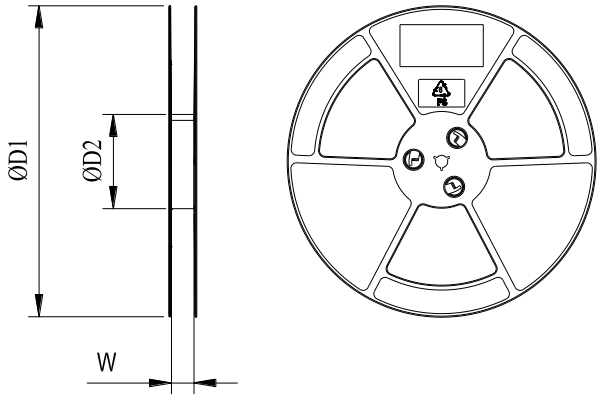


Figure 22: Plastic Reel Dimension Drawing

Table 15: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	24.5

7.3.3. Mounting Direction

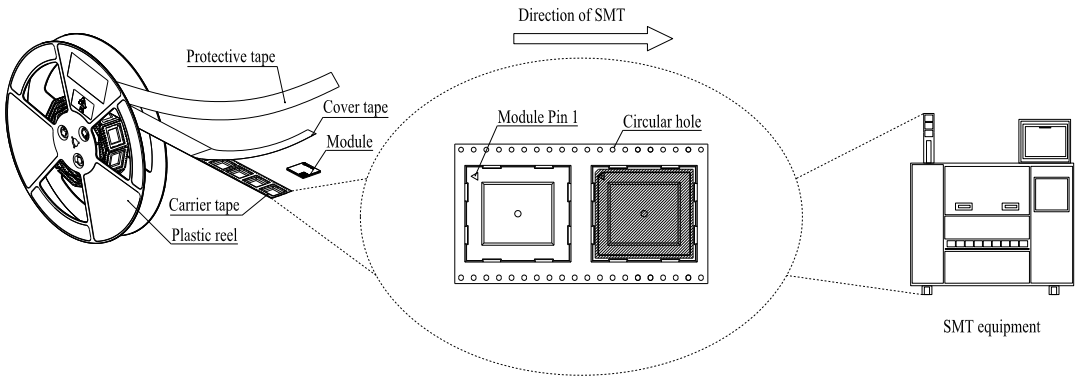
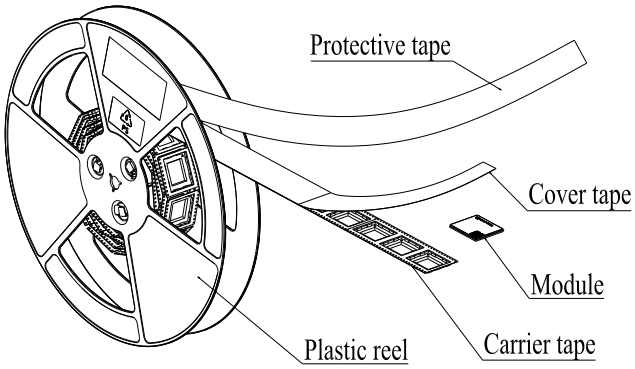


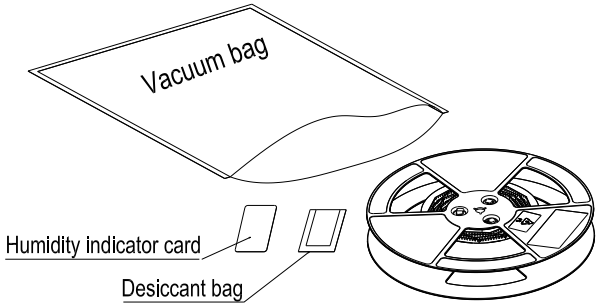
Figure 23: Mounting Direction

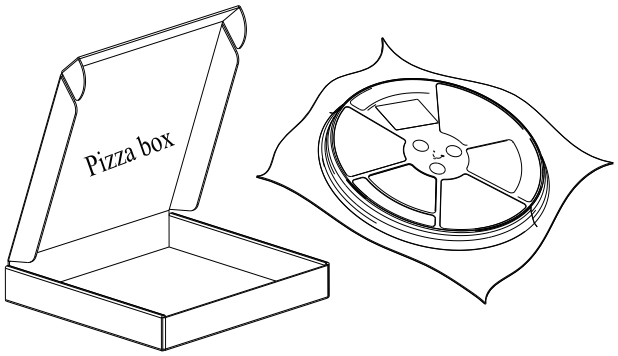
7.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

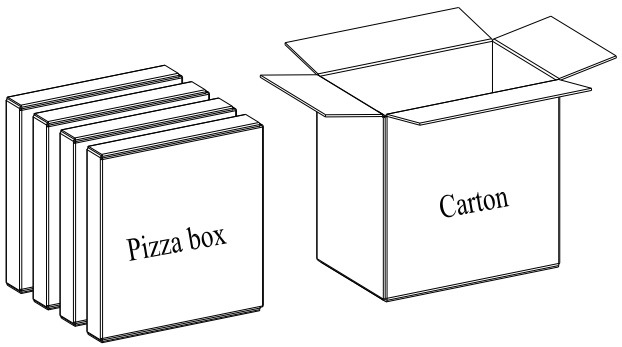


Figure 24: Packaging Process

8 Appendix References

Table 16: Related Documents

Document Name
[1] Quectel_RK3568-WF_EVB_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_Stencil_Design_Requirements
[4] Quectel_Module_SMT_Application_Note

Table 17: Terms and Abbreviations

Abbreviation	Description
AES	Advanced Encryption Standard
AP	Access Point
BPSK	Binary Phase Shift Keying
CCK	Complementary Code Keying
CDM	Charge Device Model
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DMA	Direct Memory Access
ESD	Electrostatic Discharge
EVB	Evaluation Board
EVM	Error Vector Magnitude

FEM	Front-End Module
GND	Ground
GPIO	General-Purpose Input/Output
HBM	Human Body Model
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
JTAG	Joint Test Action Group
LGA	Land Grid Array
MBIST	Memory Build-In-Self Test
Mbps	Million Bits Per Second
MCS	Modulation and Coding Scheme
MSL	Moisture Sensitivity Levels
OFDM	Orthogonal Frequency-Division Multiplexing
OWE	Opportunistic Wireless Encryption
PCB	Printed Circuit Board
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RISC-V	Reduced Instruction Set Computer Five
RoHS	Restriction of Hazardous Substances
Rx	Receive
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input/Output
SHA	Secure Hash Algorithm
SMT	Surface Mount Technology

SPDT	Single-Pole Double-Throw
SPI	Serial Peripheral Interface
STA	Station
TVS	Transient Voltage Suppressor
Tx	Transmit
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WPA	Wi-Fi Protected Access