

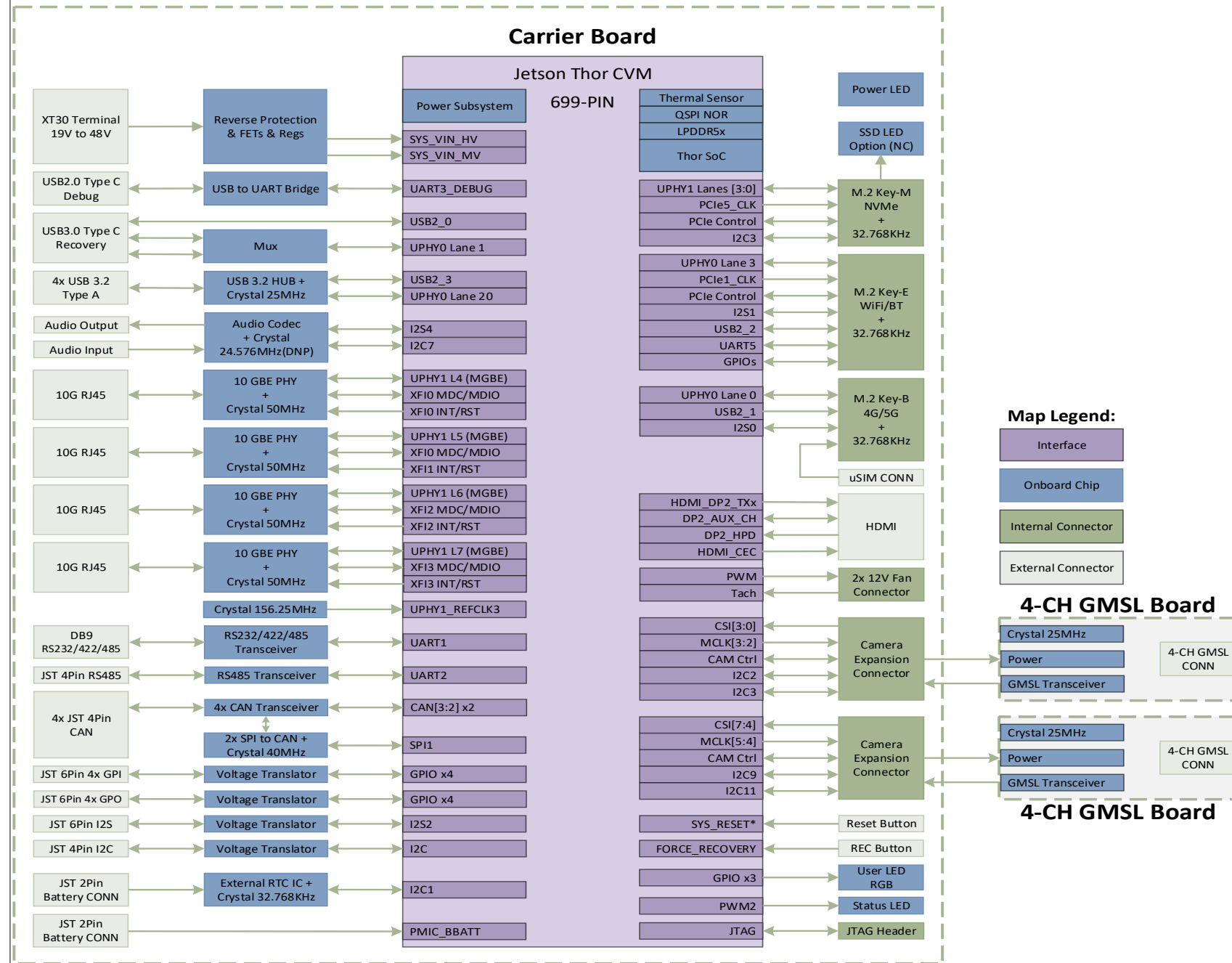
reComputer J601 Carrier Board

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Revision History

| VER  | DATE       | REVISION                                      | DESCRIPTION      |
|------|------------|-----------------------------------------------|------------------|
| V1.0 | 06/12/2026 | reComputer J601 Carrier Board_V1.0_SCH_260612 | Initial Version. |

# reComputer J601 Carrier Board Block Diagram



seeed studio

<https://www.seeedstudio.com>

Title: reComputer J601 Carrier Board

Size: A3

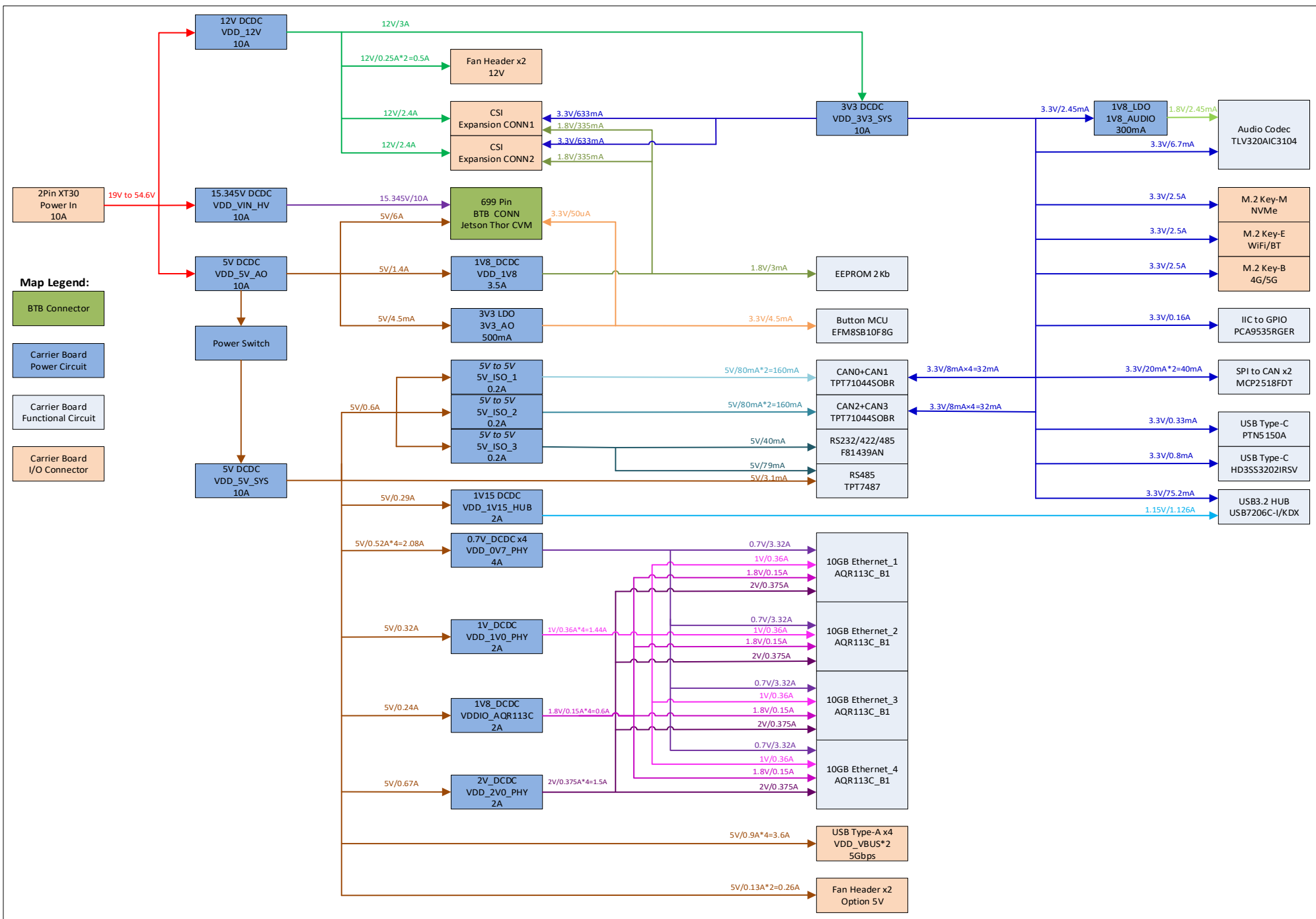
Document Number: 02 Block Diagram

Rev: V1.0

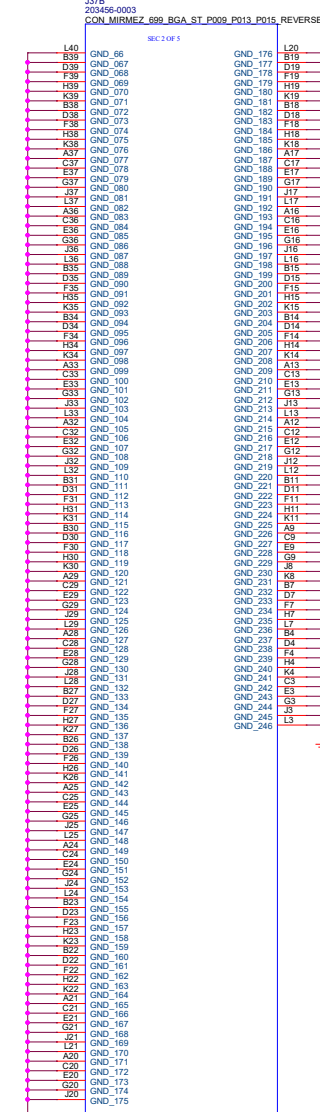
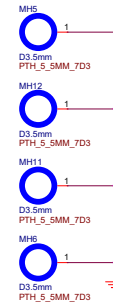
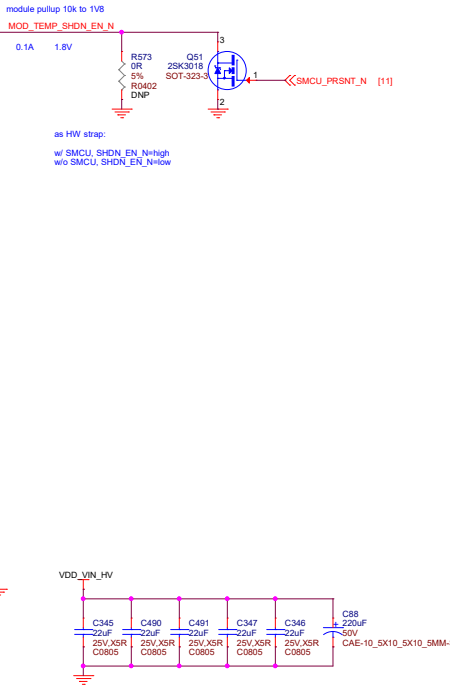
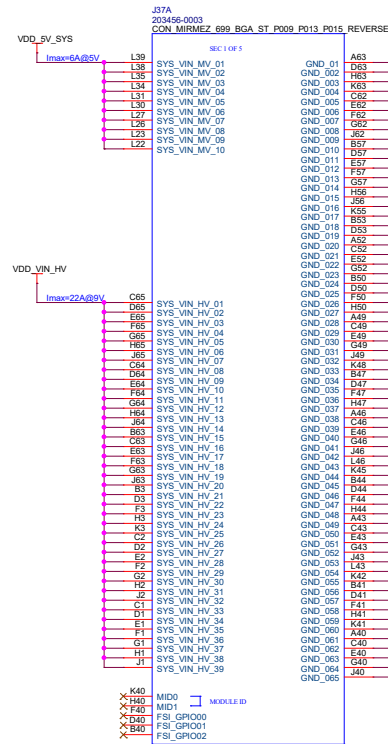
Draw By: Seeed

Date: Wednesday, May 27, 2026

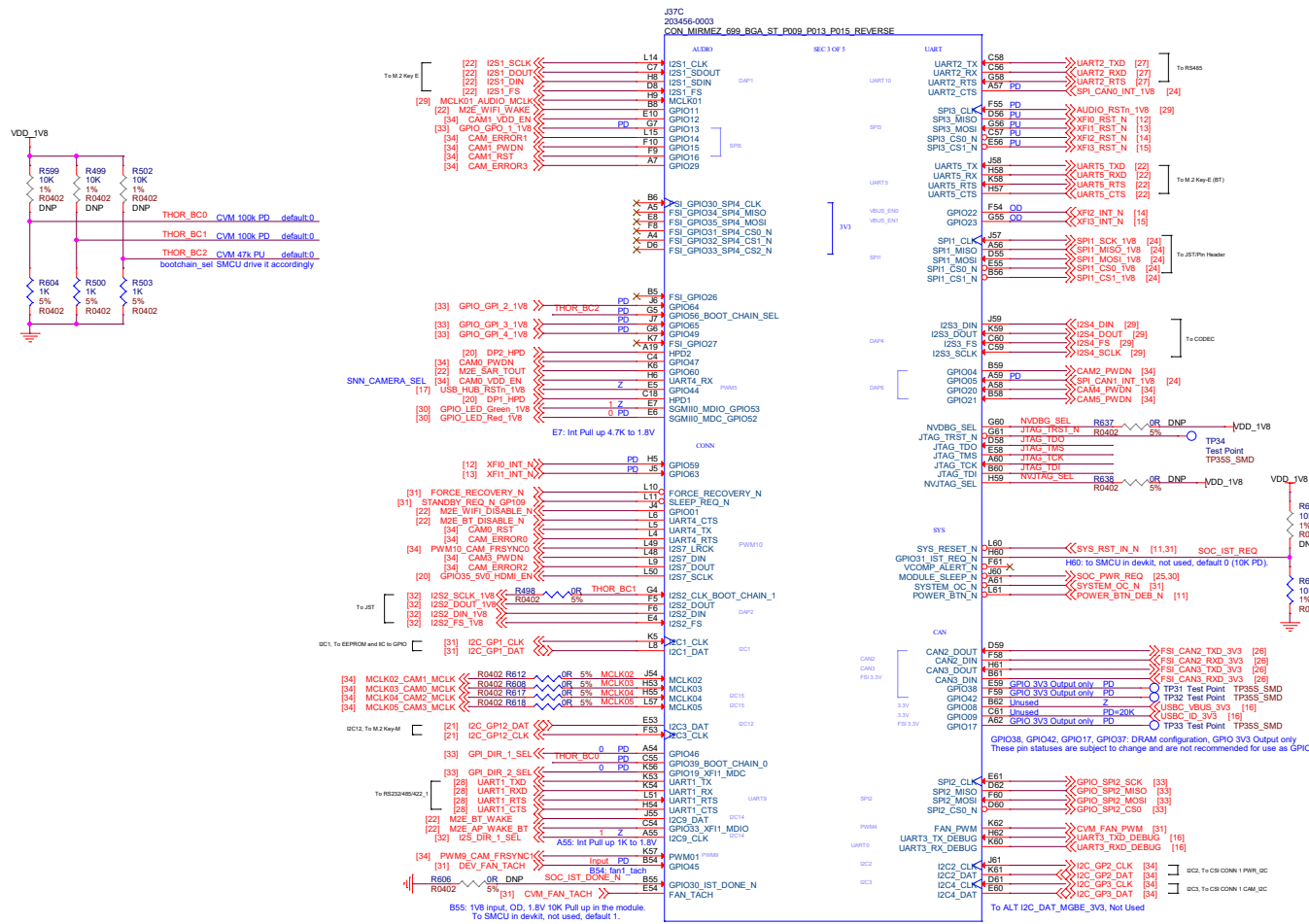
Sheet: 2 of 34



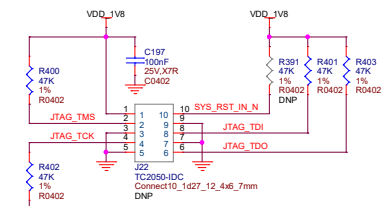
# CVM Connector 1/3



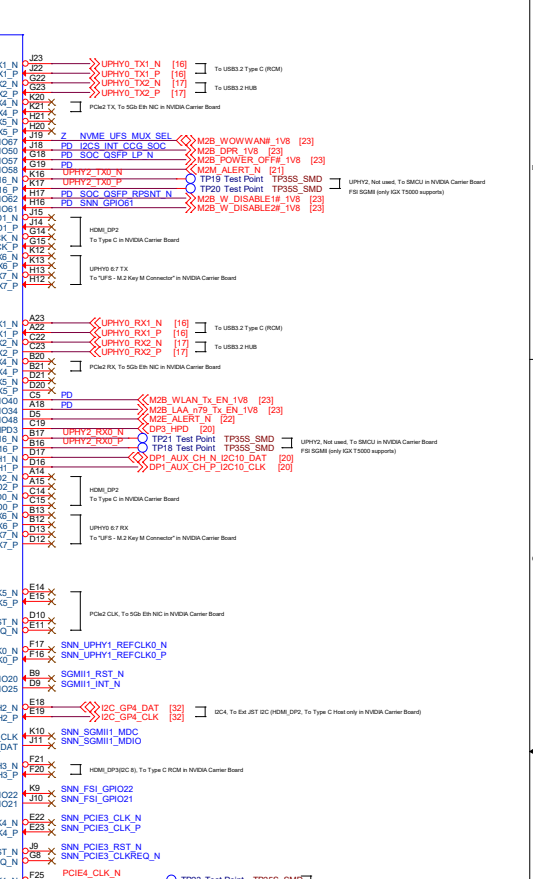
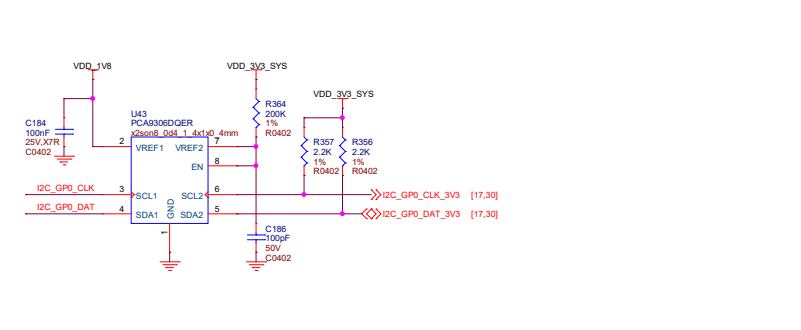
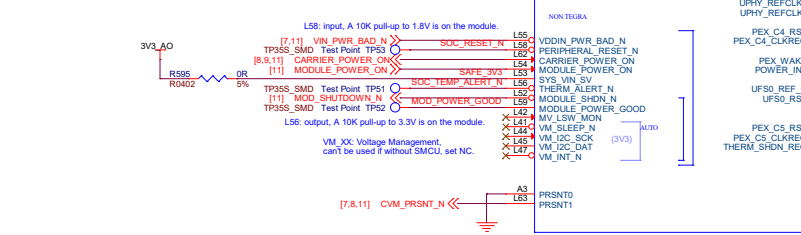
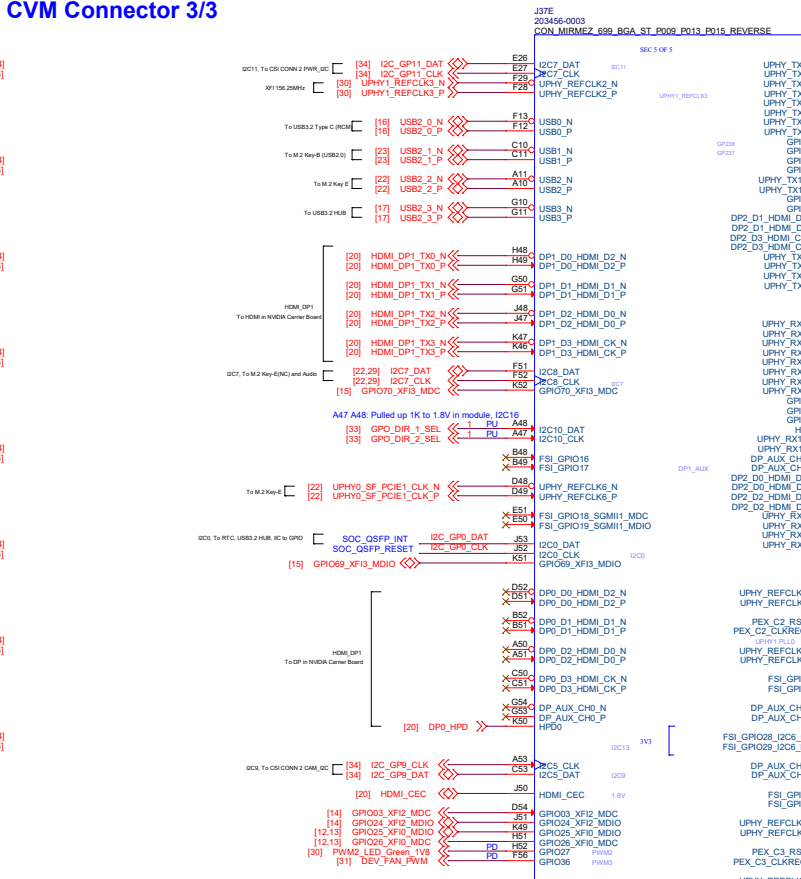
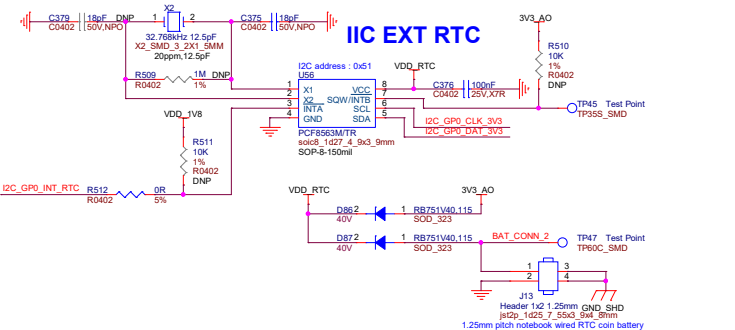
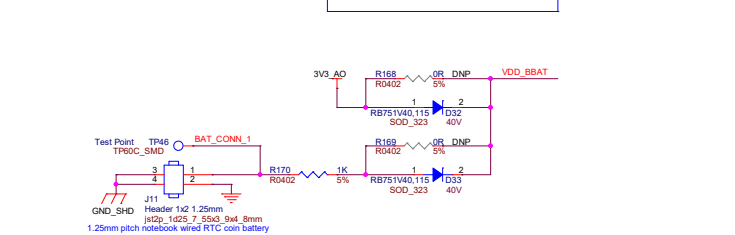
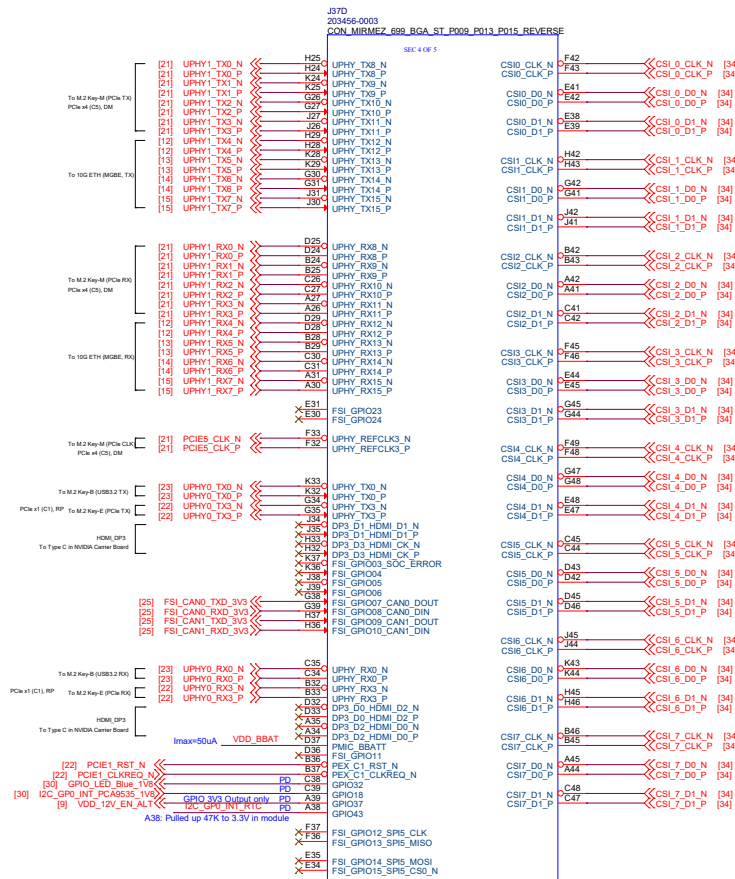
## CVM Connector 2/3



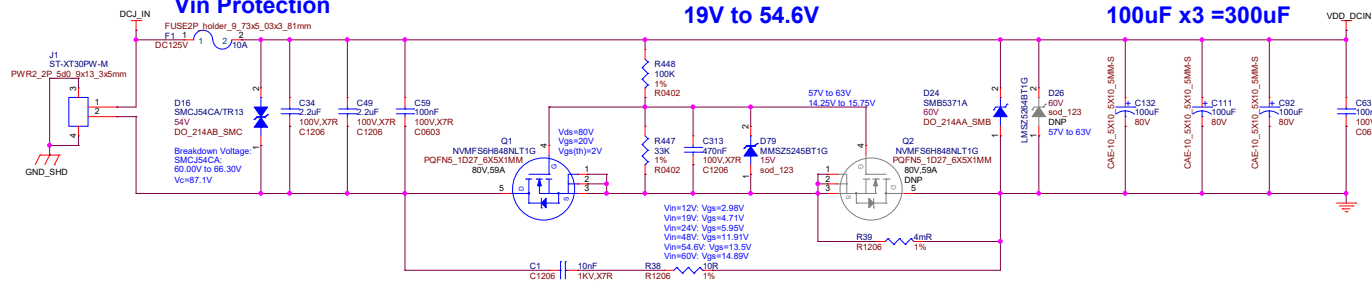
## Tag-Connect



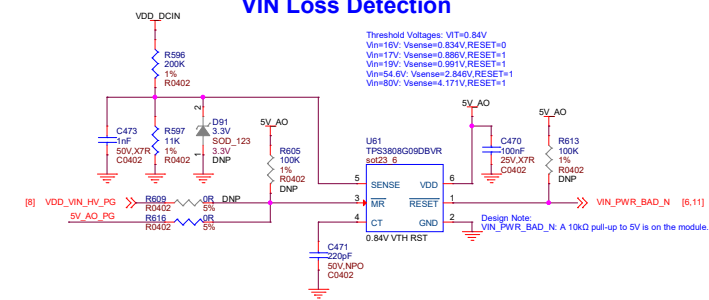
### CVM Connector 3/3



## Vin Protection



## VIN Loss Detection



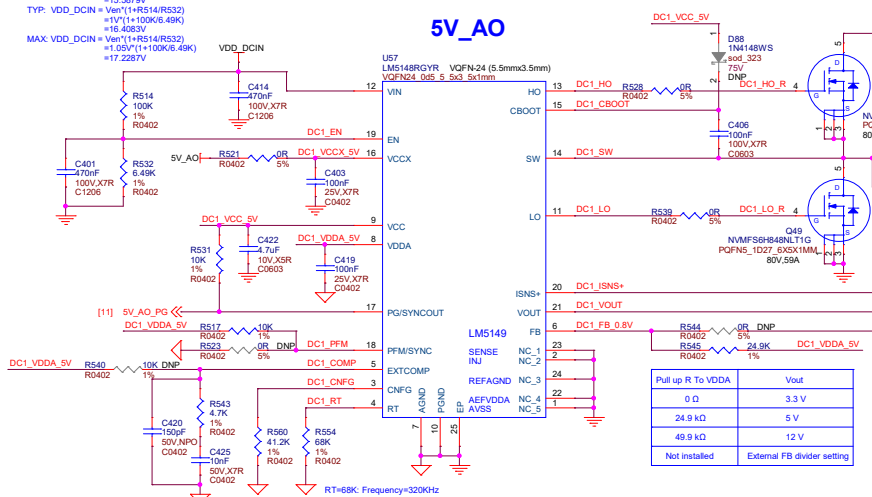
Pin20 Enable Control Pin:  
VIN\_UVLO: VDD\_DCIN=Ven\*(1+R514/R532)

MIN: VDD\_DCIN = Ven\*(1+R514/R532)  
= 0.95V\*(1+100K/6.49K)  
= 15.5879V

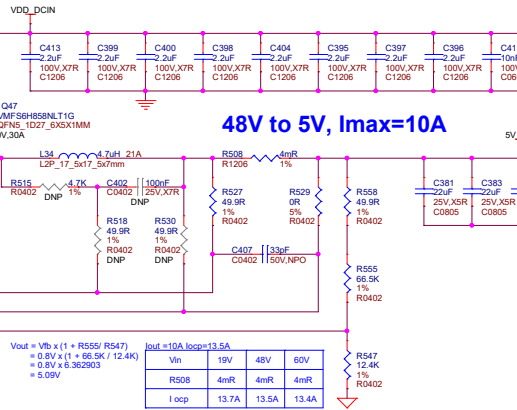
TYP: VDD\_DCIN = Ven\*(1+R514/R532)  
= 1V\*(1+100K/6.49K)  
= 16.4083V

MAX: VDD\_DCIN = Ven\*(1+R514/R532)  
= 1.05V\*(1+100K/6.49K)

**5V\_AO**



48V to 5V, I<sub>max</sub>=10A



|                   |                             |
|-------------------|-----------------------------|
| Pull up R To VDDA | Vout                        |
| 0 $\Omega$        | 3.3 V                       |
| 24.9 k $\Omega$   | 5 V                         |
| 49.9 k $\Omega$   | 12 V                        |
| Not installed     | External FB divider setting |

$$\begin{aligned} V_{out} &= V_{fb} \times (1 + R_{555} / R_{f1}) \\ &= 0.8V \times (1 + 66.5K) \\ &= 0.8V \times 6.362903 \end{aligned}$$

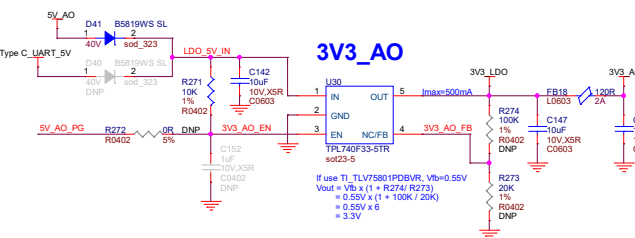
$I_{out} = 10A$   $I_{ocp} = 13.5A$

| $V_{in}$ | 19V | 48V | 60V |
|----------|-----|-----|-----|
|----------|-----|-----|-----|

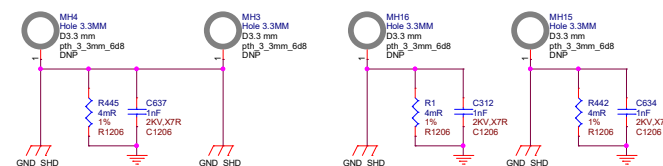
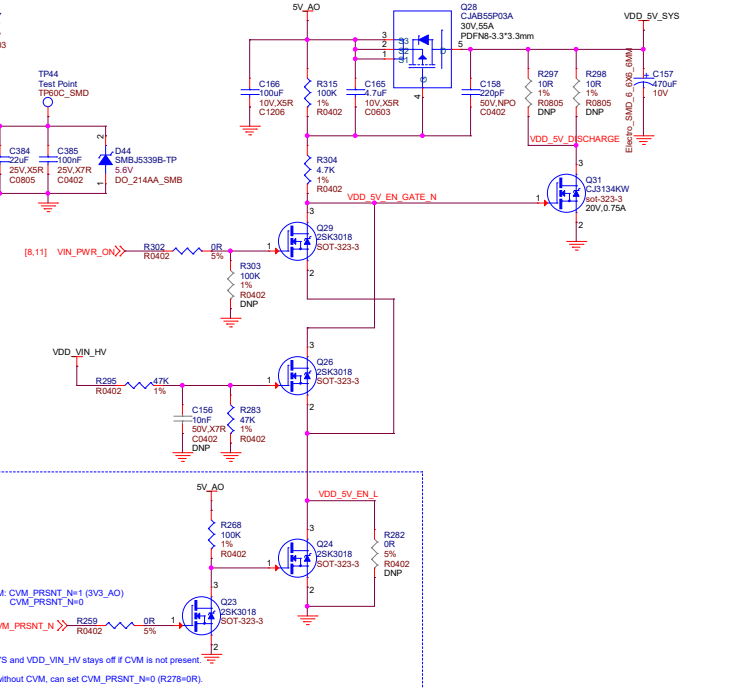
|      |       |       |       |
|------|-------|-------|-------|
| R508 | 4mR   | 4mR   | 4mR   |
| Loss | 10.34 | 10.54 | 10.44 |

|           |       |       |       |
|-----------|-------|-------|-------|
| $I_{ocp}$ | 13.7A | 13.5A | 13.4A |
|-----------|-------|-------|-------|

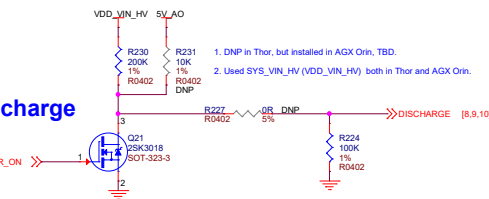
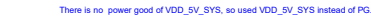
### 3V3 AO



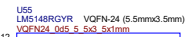
**VDD\_5V**



Power On : MV -> HV  
Power Off: HV -> MV



[6,8,9,11] CARRIER\_POWER\_ON >> 1



|       |       |
|-------|-------|
| Vin   | 19V   |
| R452  | 4mR   |
| I ocp | 14.7A |

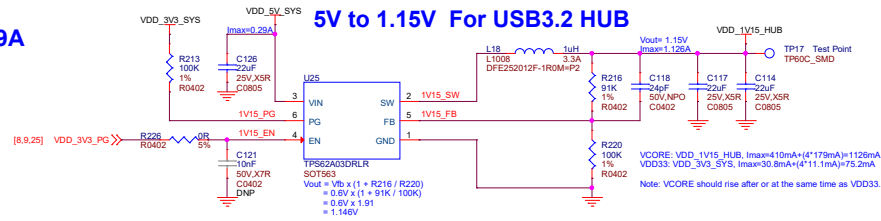




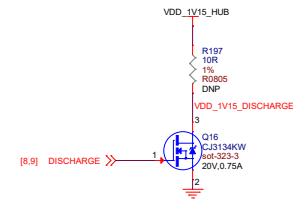


## USB3.2 HUB Power

**USB Total: 5V 5.09A**



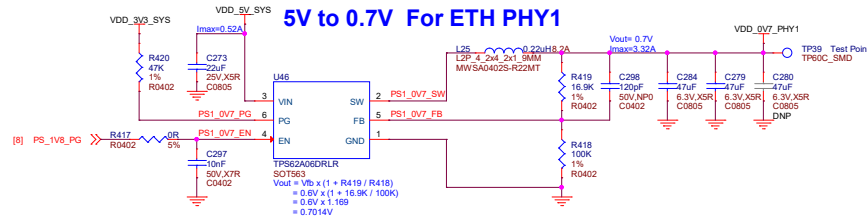
### VDD\_1V15\_HUB Discharge



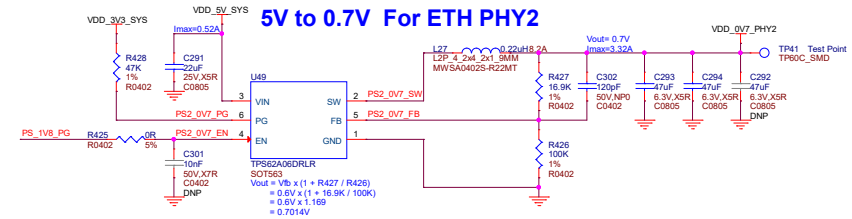
**Ethernet Total: 5V 3.31A**

## 10G Ethernet PHY Power

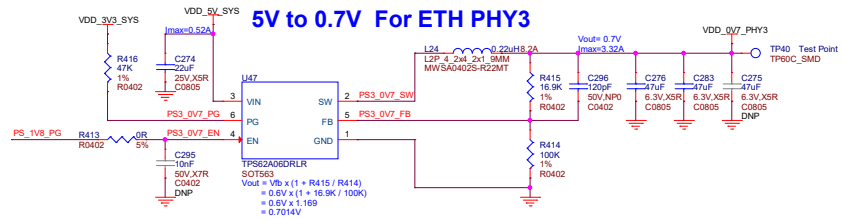
**5V to 0.7V For ETH PHY1**



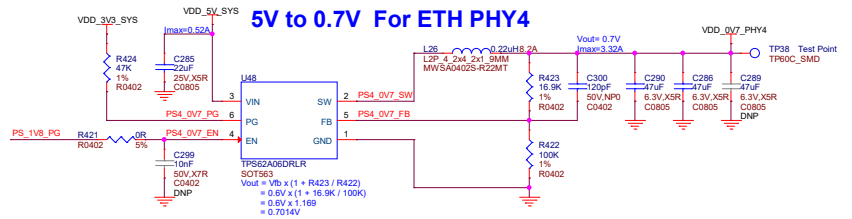
**5V to 0.7V For ETH PHY2**



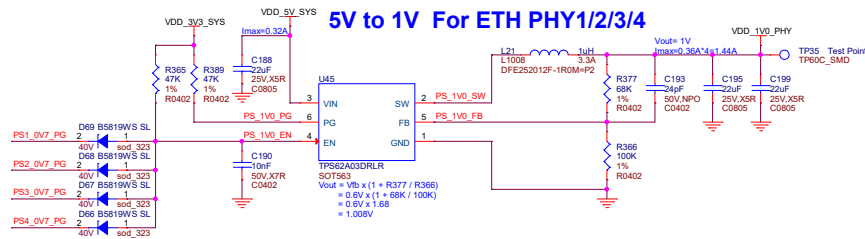
**5V to 0.7V For ETH PHY3**



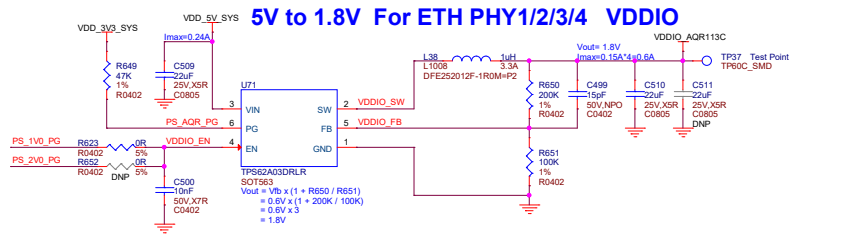
**5V to 0.7V For ETH PHY4**



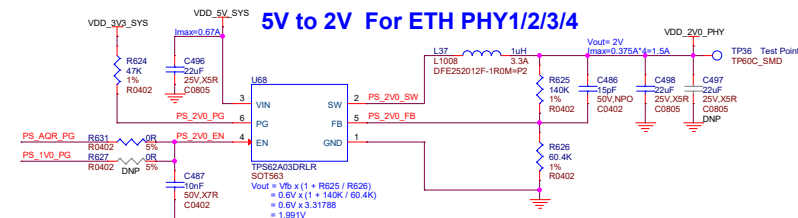
**5V to 1V For ETH PHY1/2/3/4**



YS **5V to 1.8V For ETH PHY1/2/3/4 VDDIO**



**5V to 2V For ETH PHY1/2/3/4**

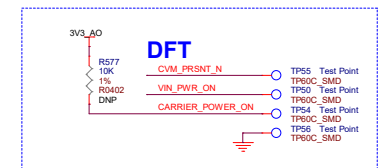
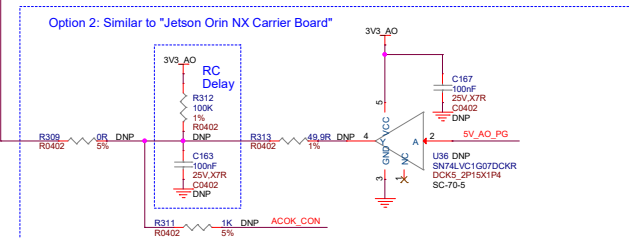
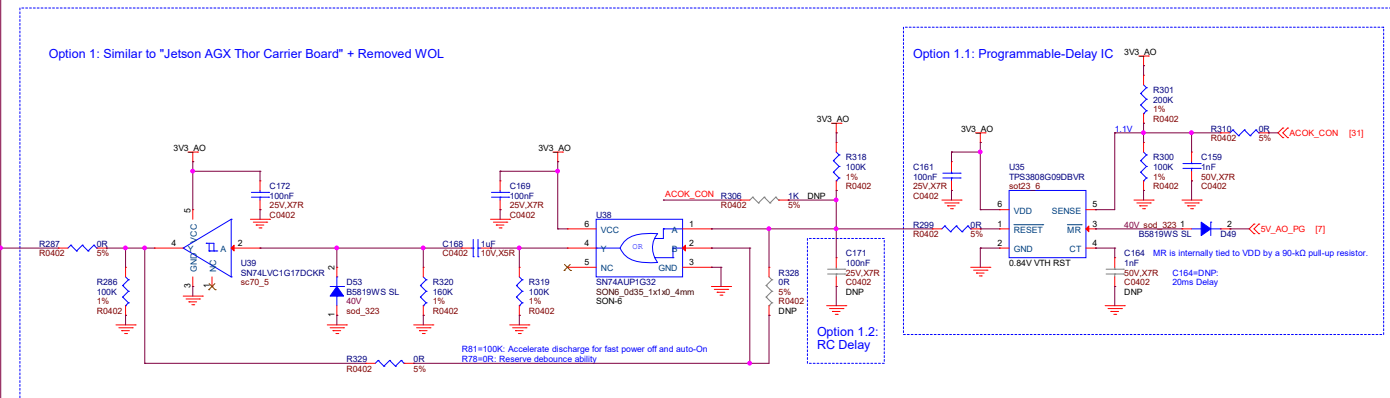
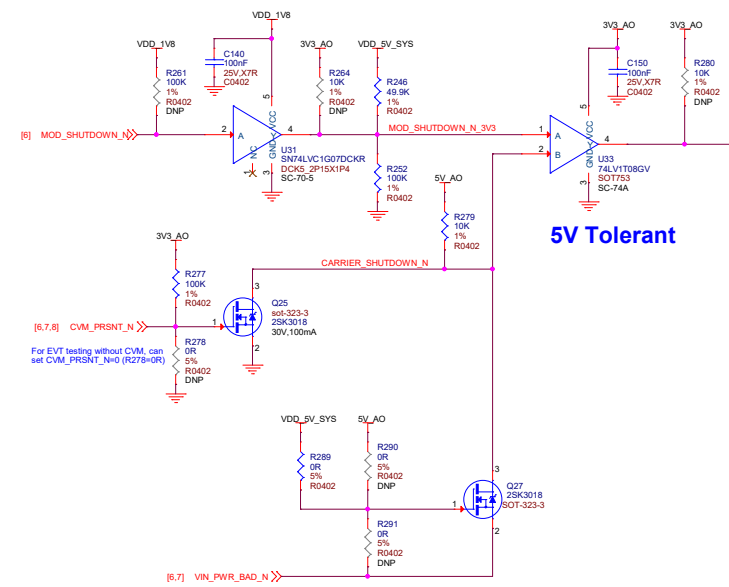
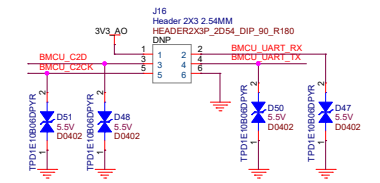
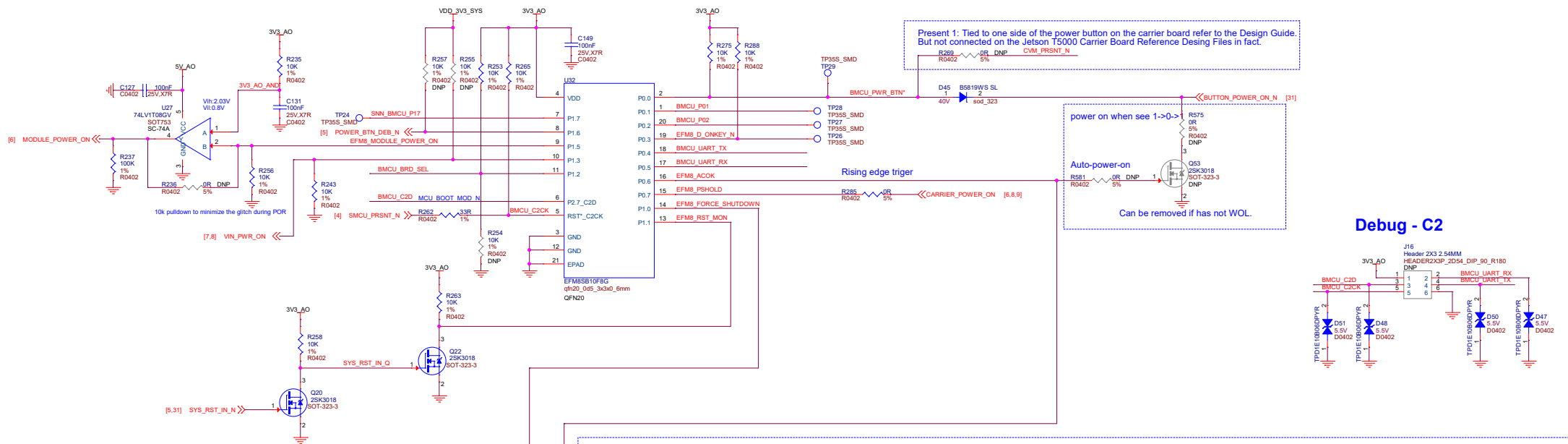


### PHY AQR113C Power-Up Sequence Requires:

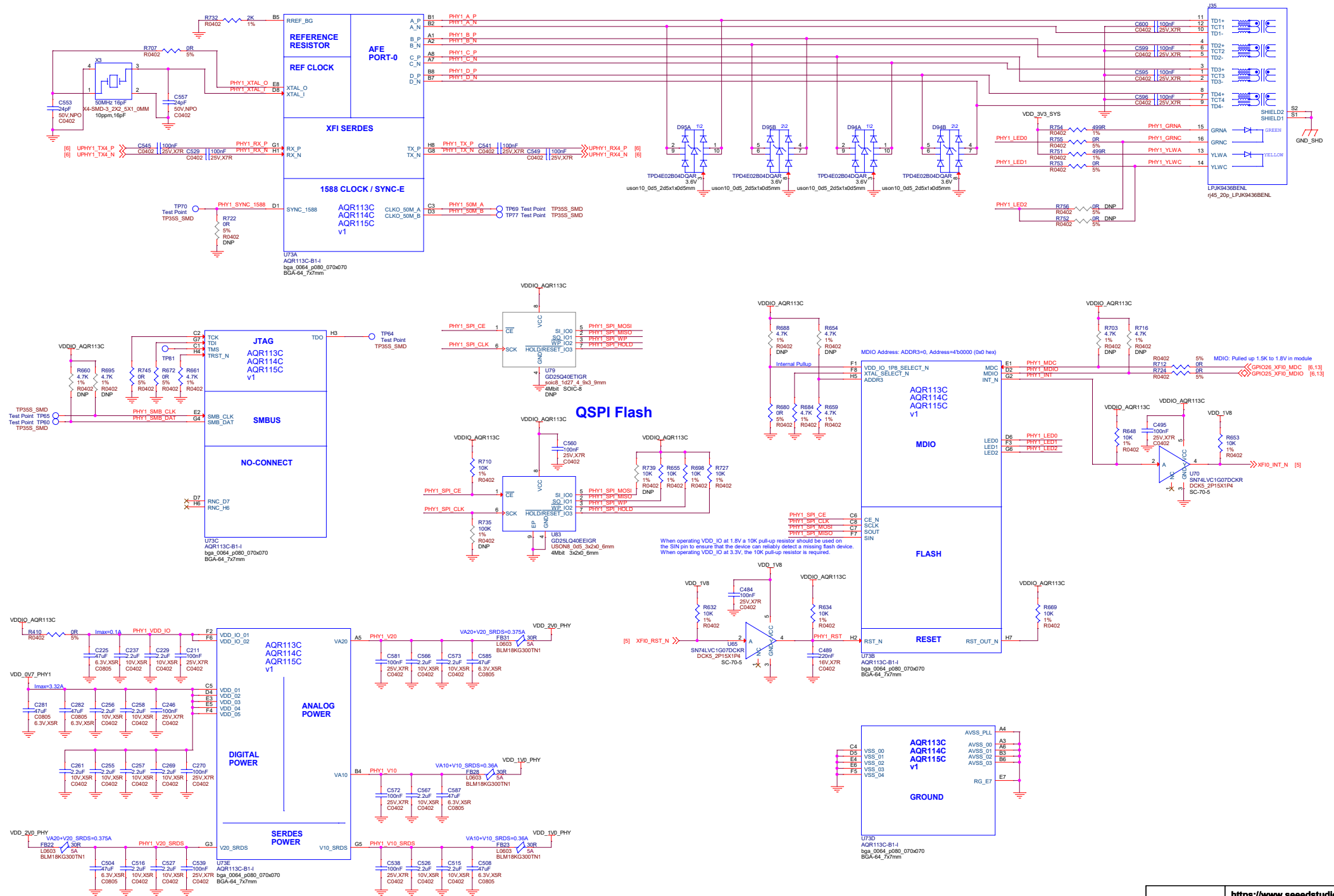
If VDD IO is 1.8V: VDD -> 1.0V -> VDD IO -> 2.0V, Default.

If VDD\_IO is 3.3V: VDD -> 1.0V -> 2.0V -> VDD\_IO.

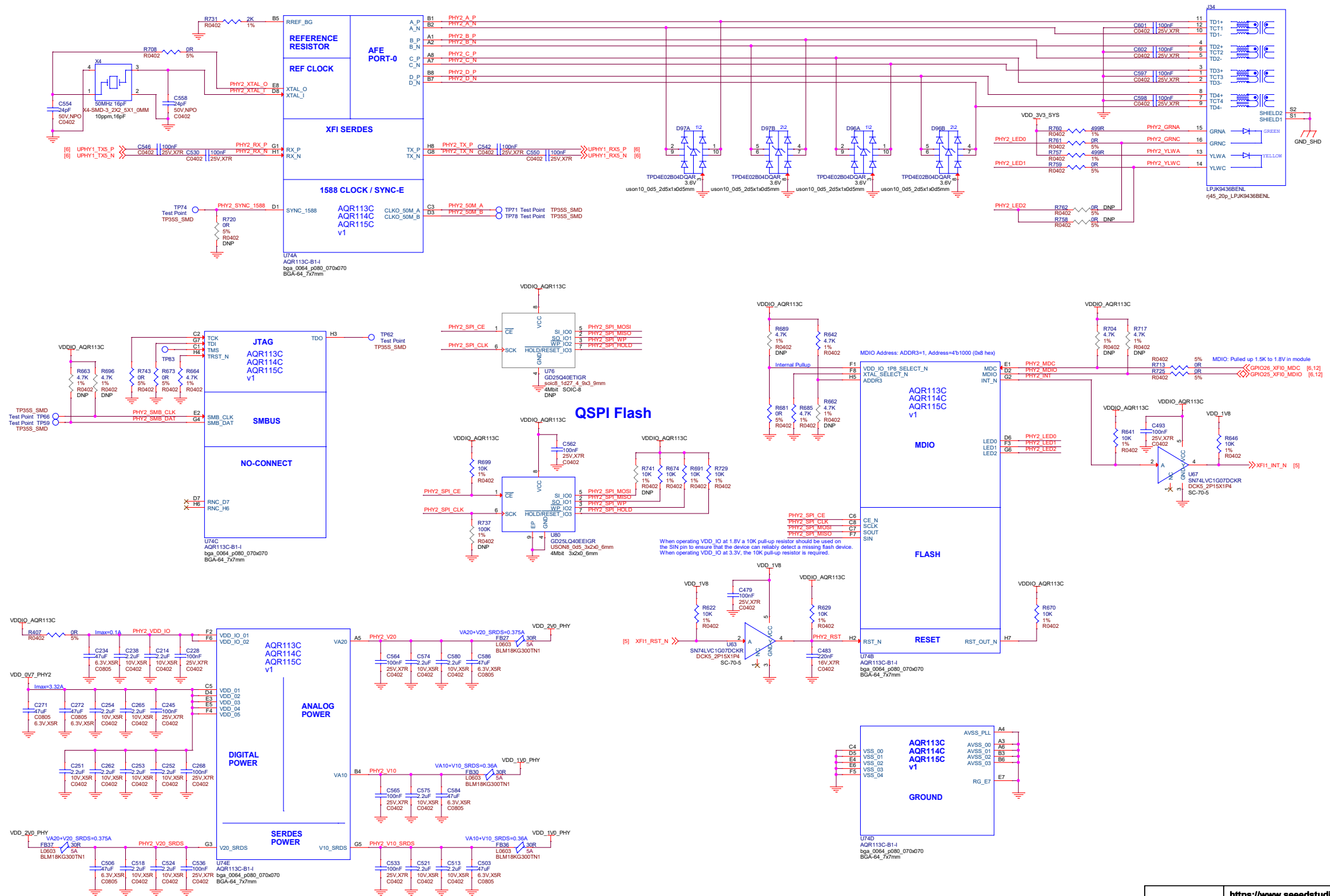
## Button MCU For Power Up



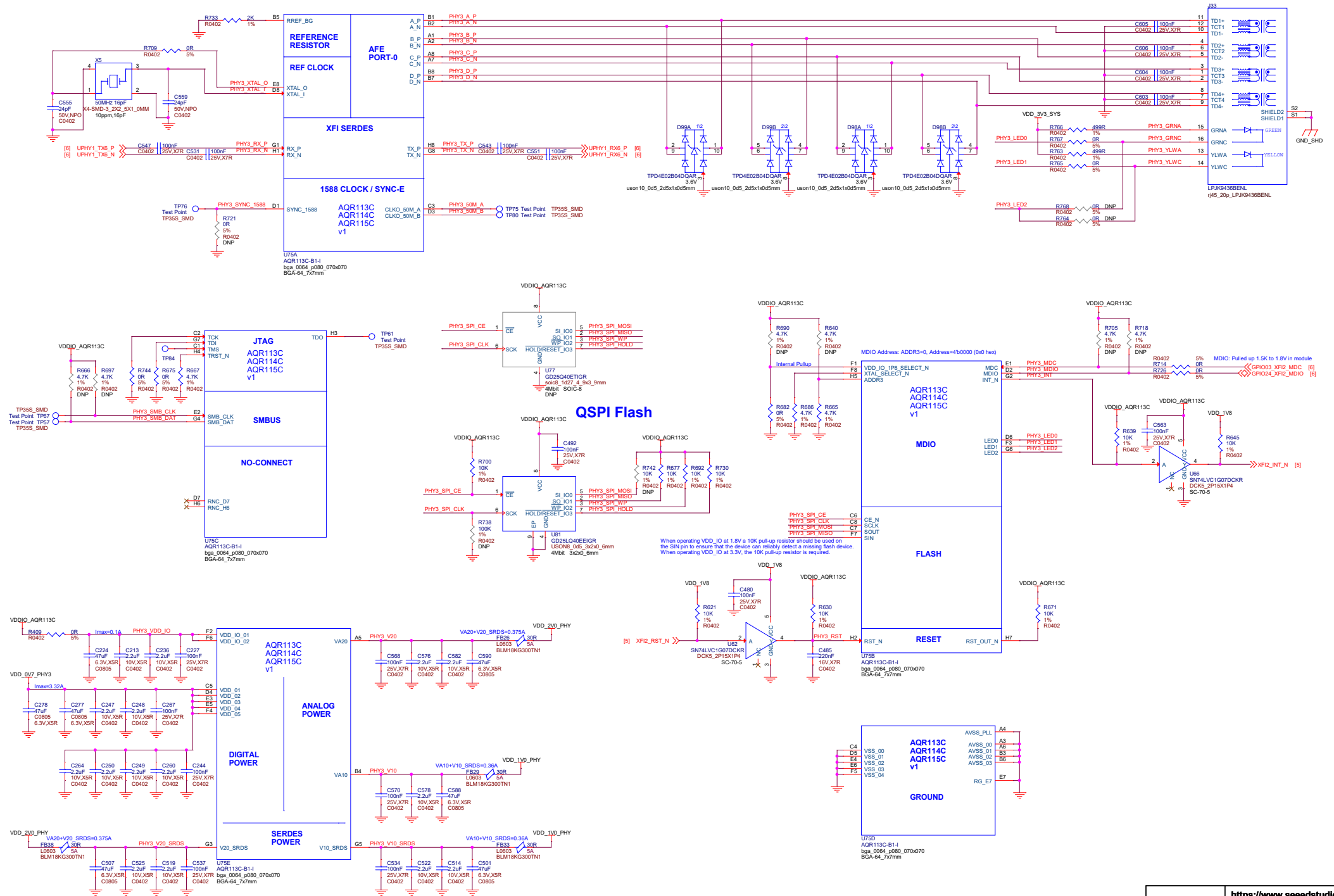
# 10GB Ethernet 1/4



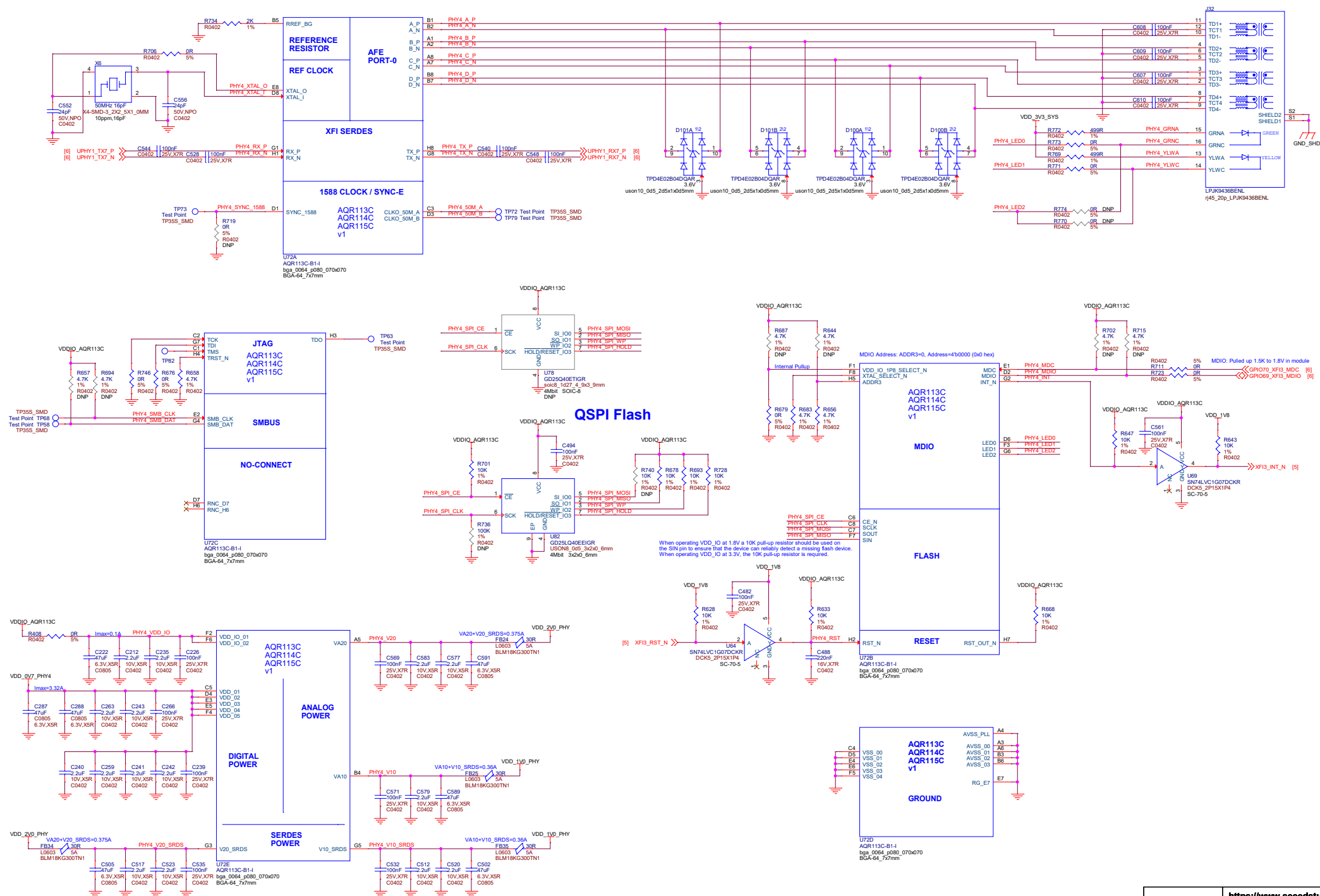
## 10GB Ethernet 2/4



# 10GB Ethernet 3/4

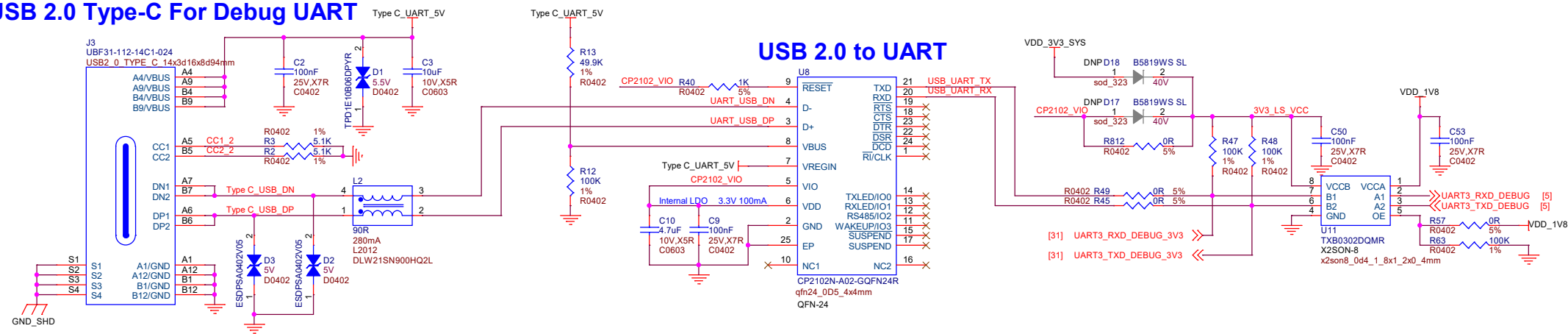


## 10GB Ethernet 4/4

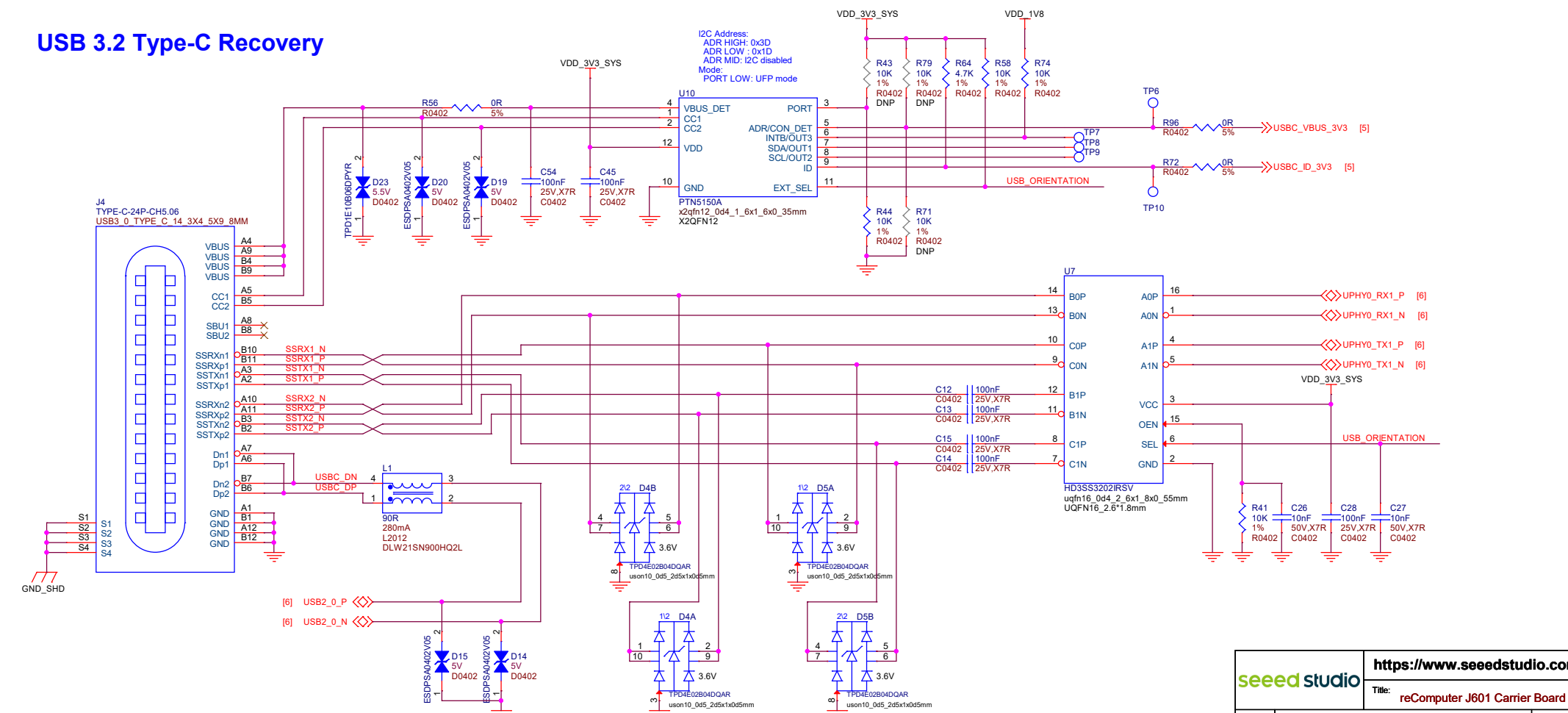




# USB 2.0 Type-C For Debug UART



# USB 3.2 Type-C Recovery





[illegible]

**USB 3.2 GEN2 10Gbps HUB x6 Ports**

**Design Note:**  
 USB\_HUB\_Reset\_1V8: From Thor GPIO, 1.8V.  
 USB\_HUB\_Reset\_3V3: From IC to GPIO, 3.3V.

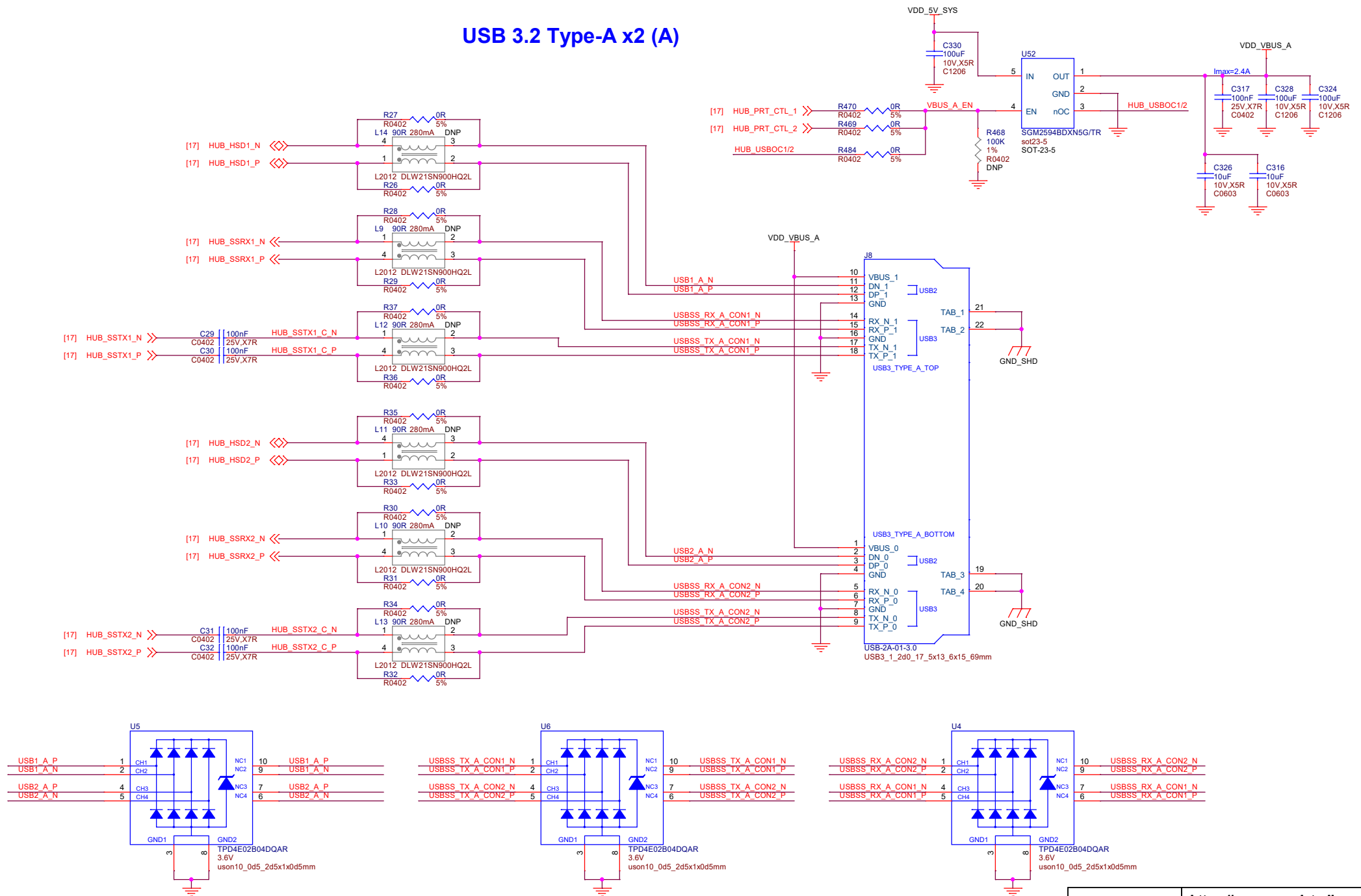
**QSPI Flash**

**Design Note:**  
 CFG\_BC\_EN: 200K Pull-Down. No battery charging  
 CFG\_NON\_REM: 200K Pull-Down. All ports removable

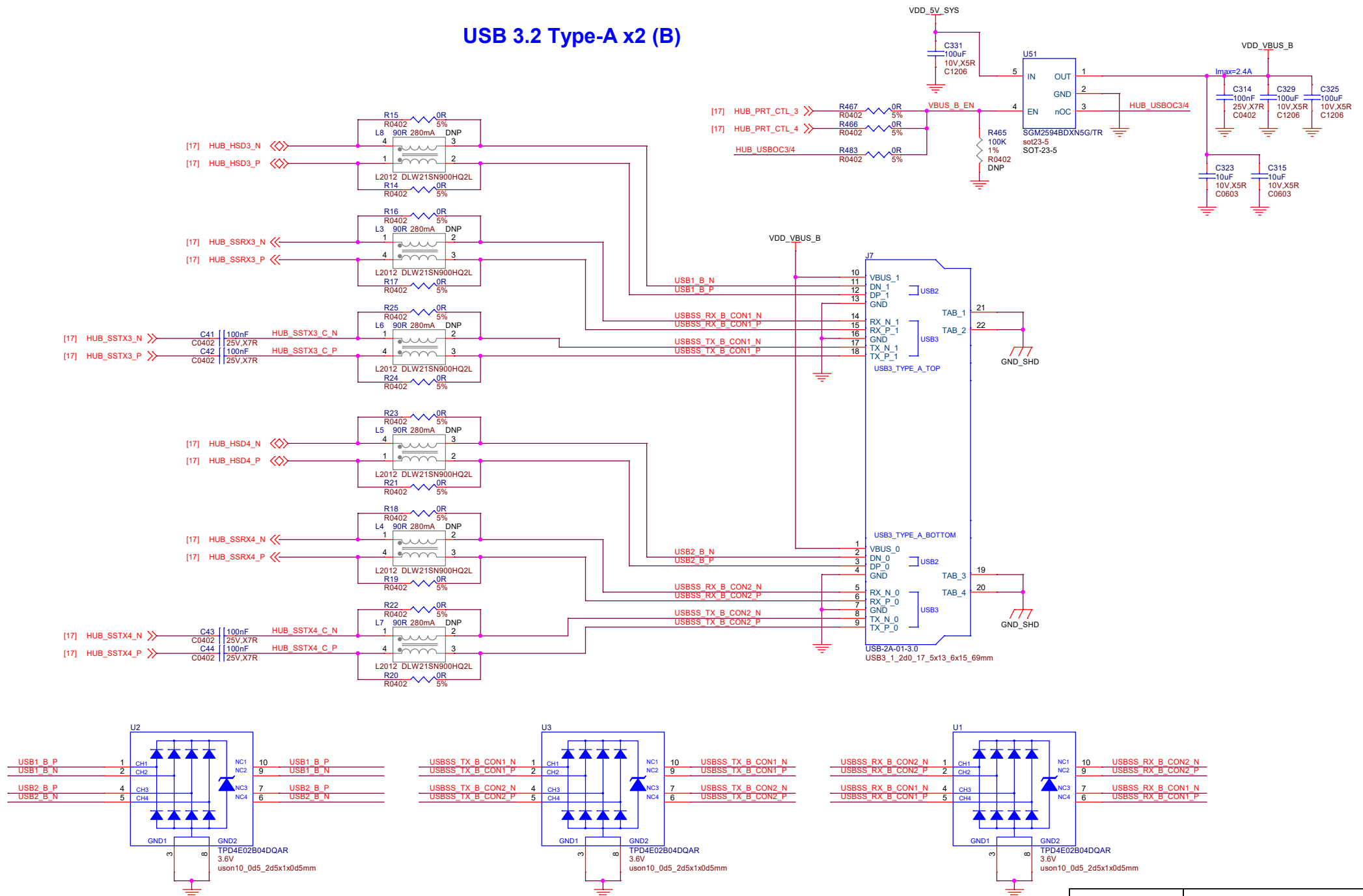
**reComputer J601 Carrier Board**

Size: A2 | Document Number: 17 USB 3.2 HUB | Rev: V1.0  
 Draw By: Seede | Date: Wednesday, May 27, 2026 | Sheet: 17 of 34

# USB 3.2 Type-A x2 (A)

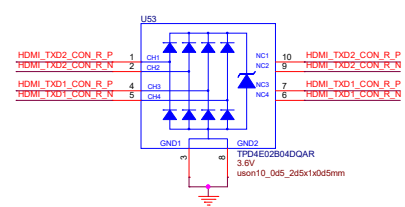
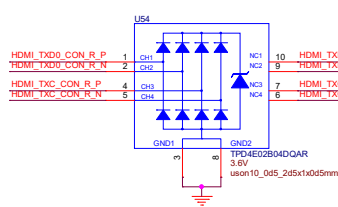
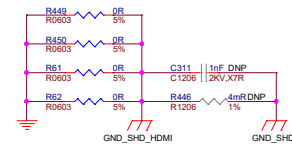
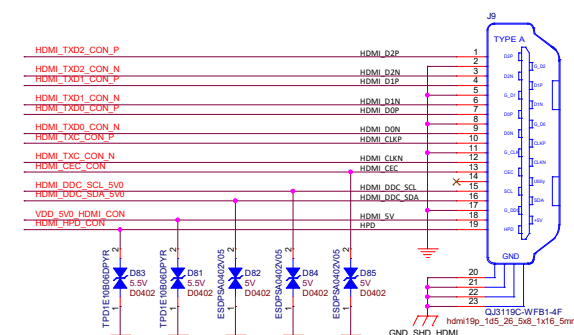
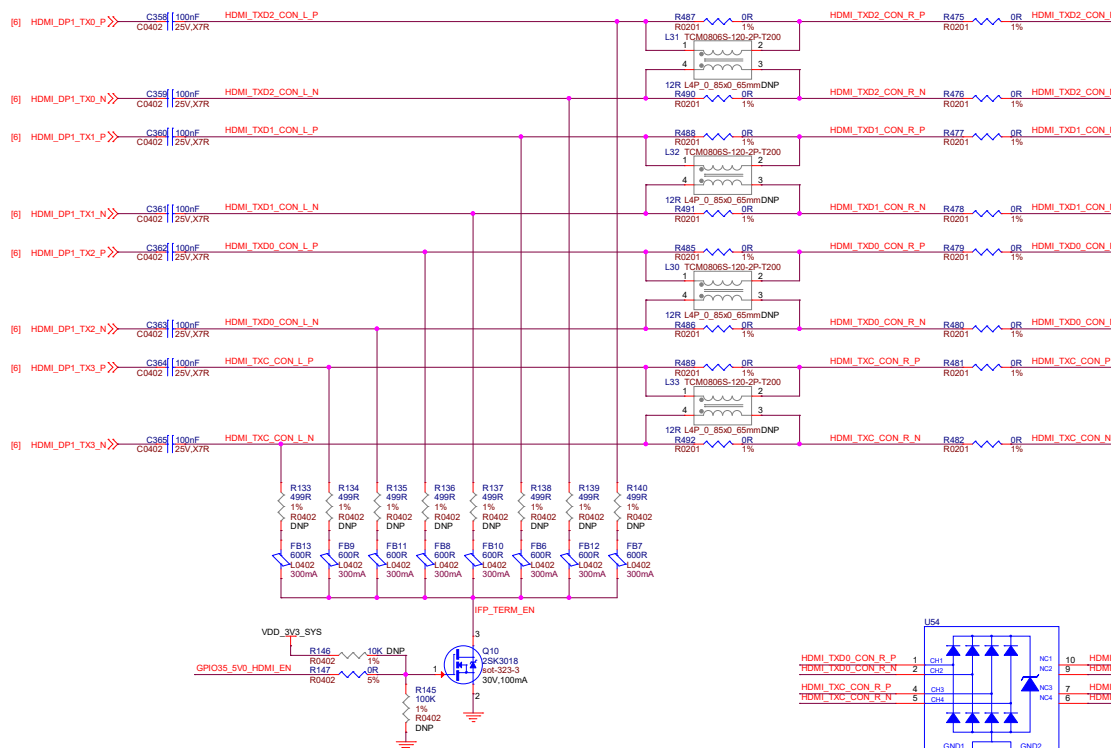
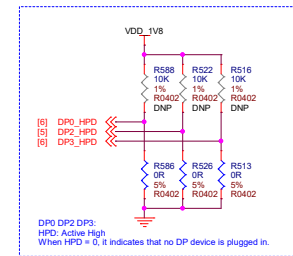
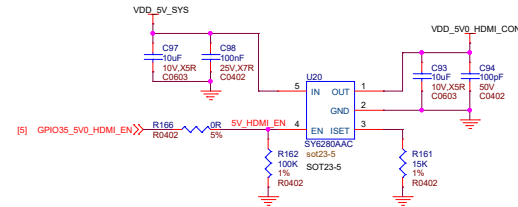


# USB 3.2 Type-A x2 (B)



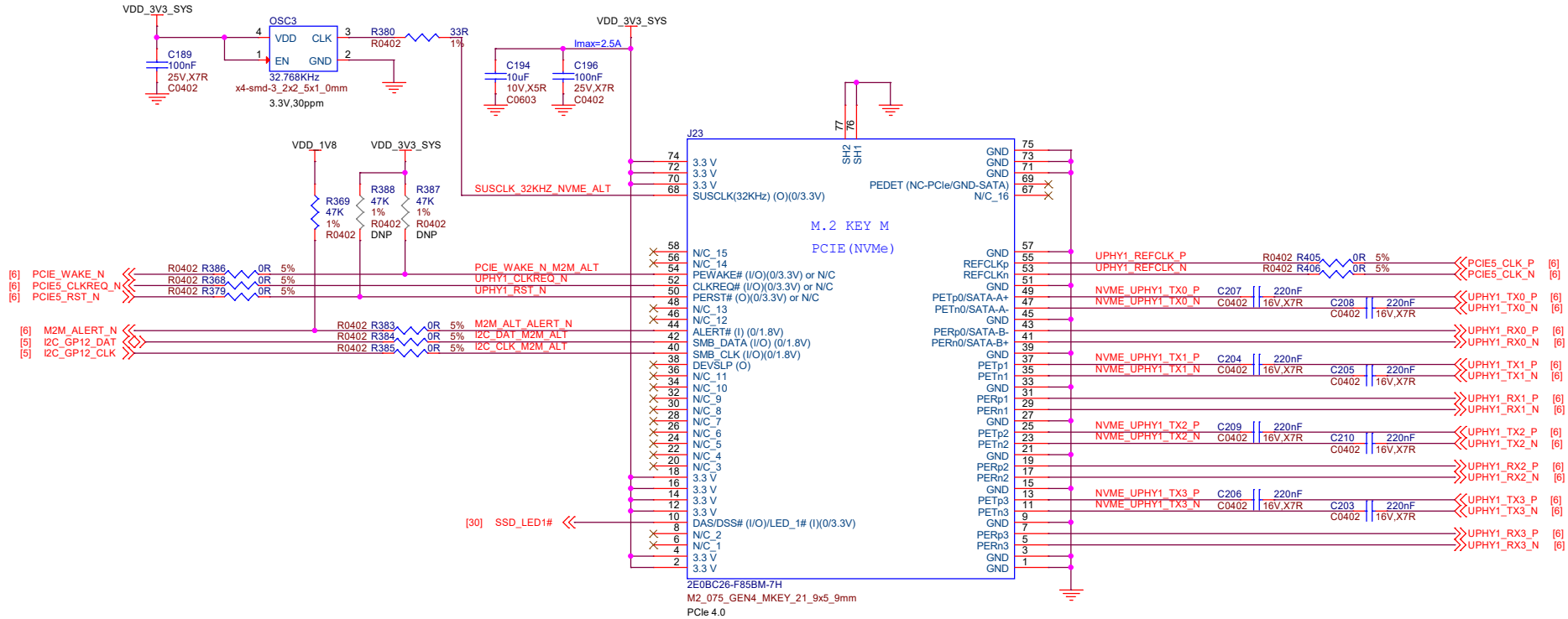
The schematic diagram illustrates the HDMI interface circuit. It shows the connection between the HDMI connector and the board. The circuit includes the following components and connections:

- Power Supply:** VDD\_1V8 and VDD\_5V0 are connected to the HDMI connector.
- Resistors:** R52 (10K, 1%, R0402), R57 (10K, 1%, R0402), R51 (2.2K, 1%, R0402), R56 (2.2K, 1%, R0402), R141 (0R, R0402), R142 (0R, R0402), R113 (160K, 1%, R0402), R112 (33K, 1%, R0402), and R131 (0R, R0402).
- Capacitors:** C56 (100nF, 25V X7R, C0402), C57 (100nF, 50V NPO, C0402), C47 (12pF, 50V NPO, C0402), C55 (12pF, 50V NPO, C0402), and C76 (2pF, 50V NPO, C0402).
- Integrated Circuits:** Q3 (25K3018, sot-323-3, 30V, 100mA), Q6 (25K3018, sot-323-3, 30V, 100mA), Q8 (25K3018, sot-323-3, 30V, 100mA), and D28 (B5819WS SL, 40V, sot\_323).
- Signals:**
  - HDMI\_DDC\_SDA\_5V0 and HDMI\_DDC\_SCL\_5V0 are connected to the HDMI connector.
  - HDMI\_AUX\_N\_I2C0\_DAT and HDMI\_AUX\_CH\_P\_I2C0\_CLK are connected to the HDMI connector.
  - HDMI\_CEC is connected to the HDMI connector.

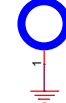


## M.2 Key M (NVMe)

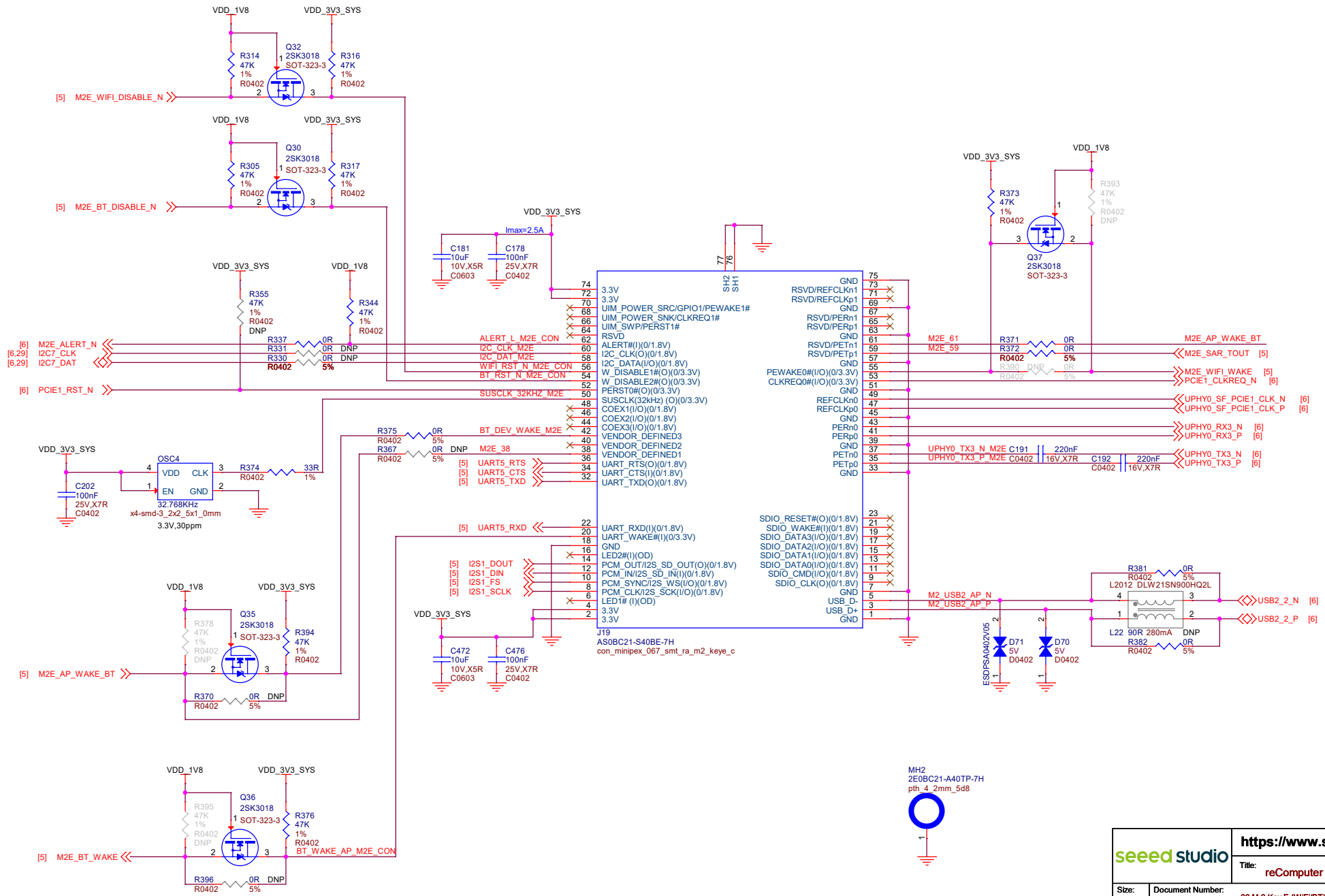
Size:2280,H=8.5MM

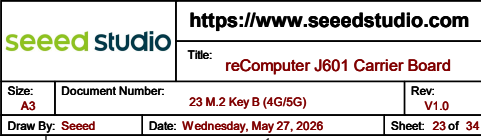


MH1  
SMTS02565CTJ-UL  
p1h\_4\_2mm\_5d8

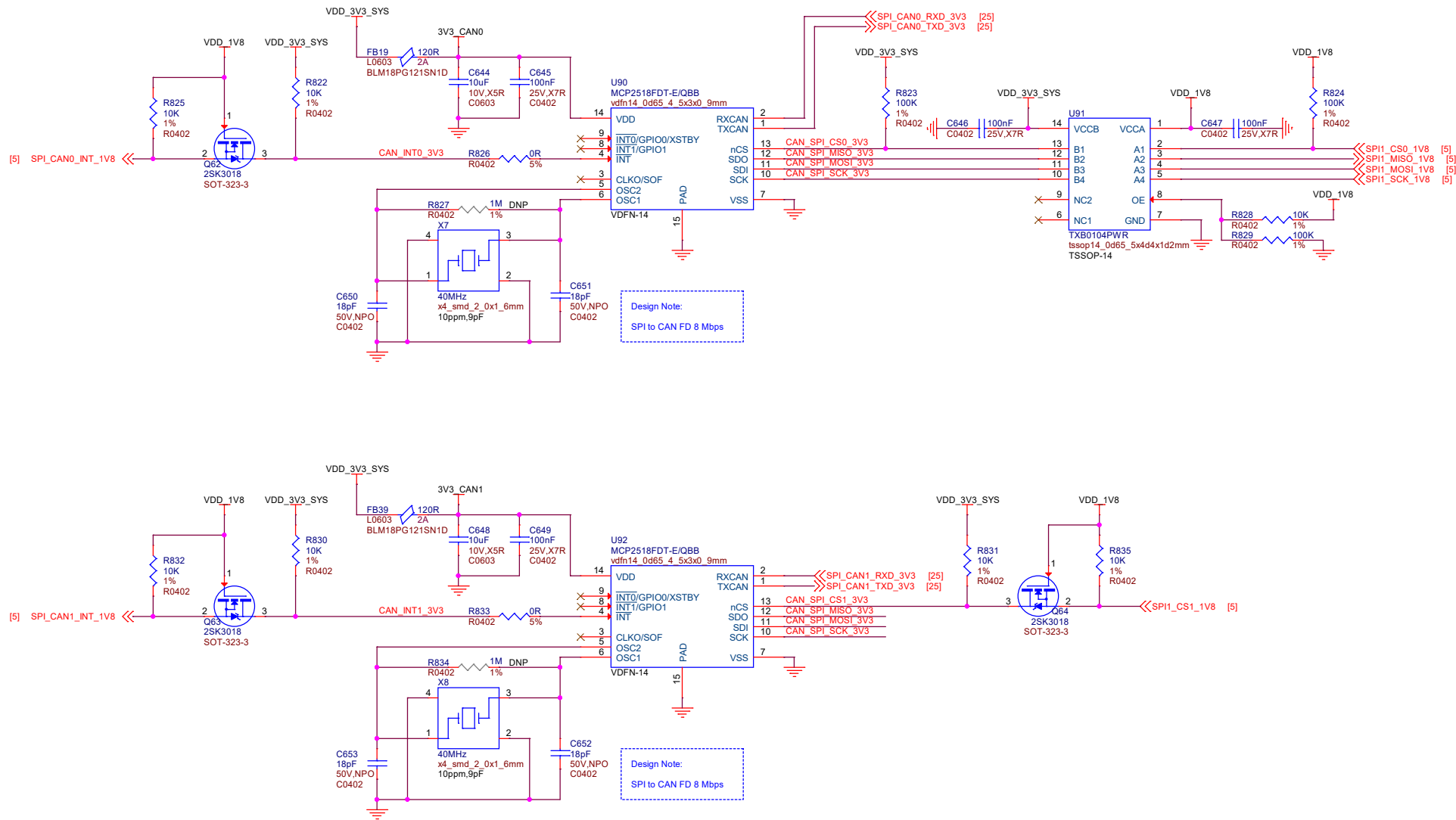


## M.2 Key E (WiFi/BT)

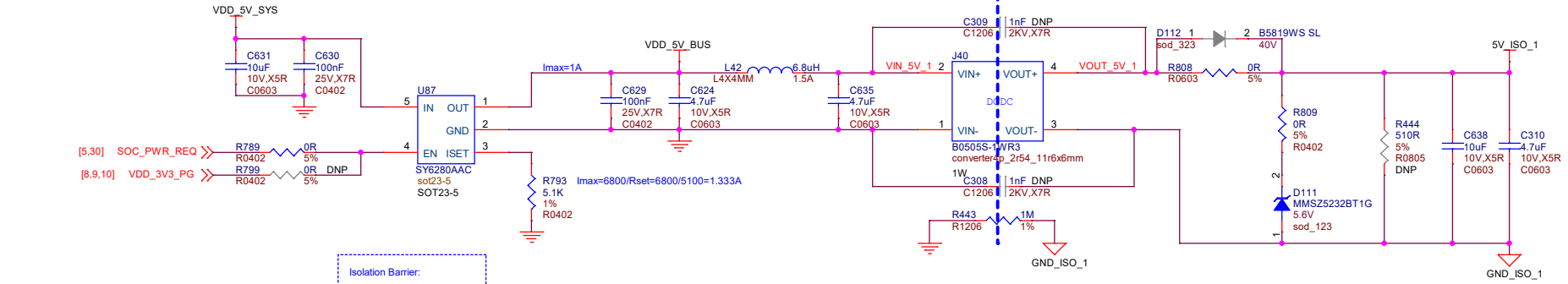




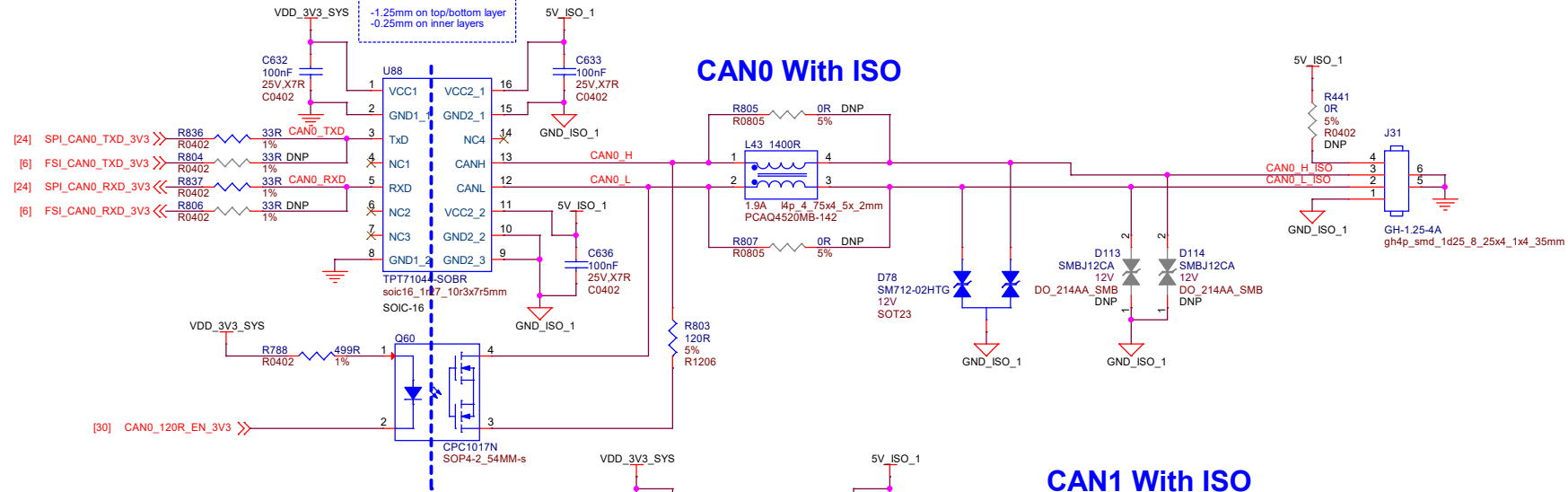




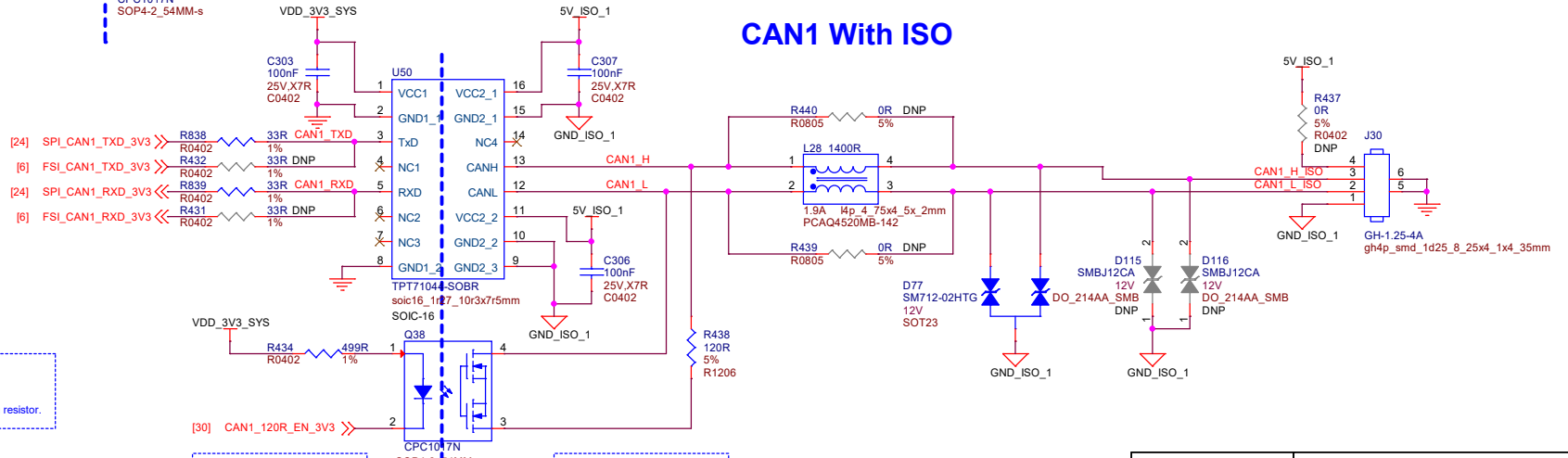
## Isolated DCDC 5V to 5V/200mA



## CAN0 With ISO



## CAN1 With ISO

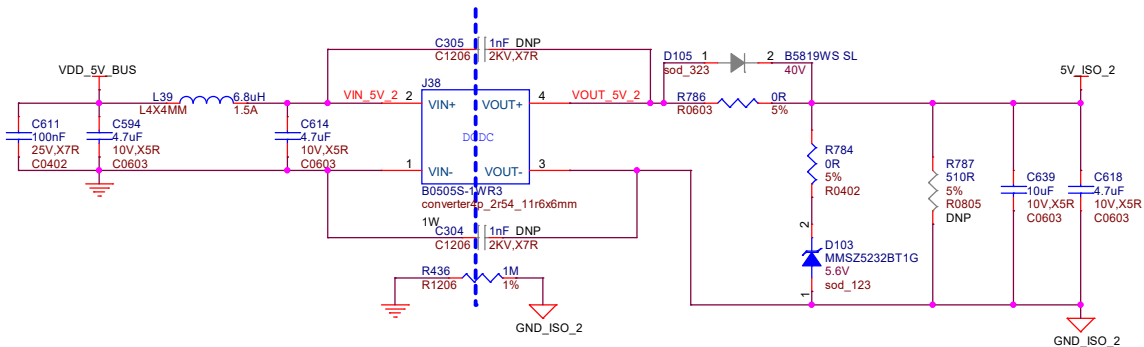


Design Note:  
Terminating Resistor Switch.  
CAN\_120R\_EN=L to enable terminating resistor.

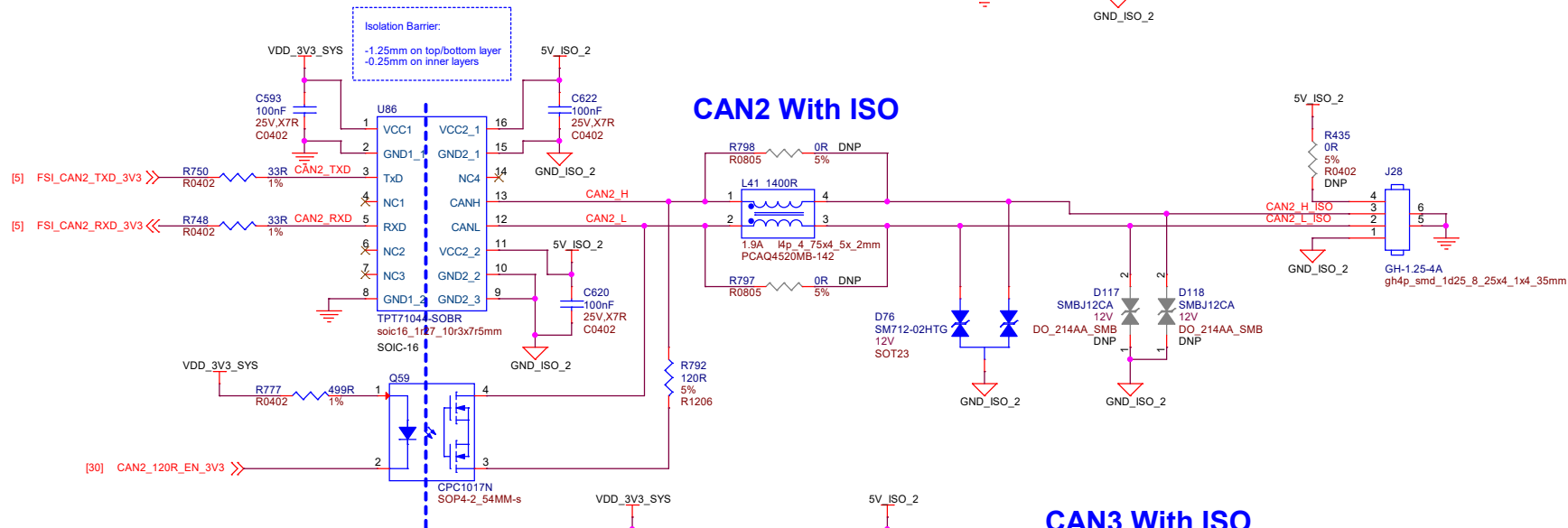
Design Note:  
CAN FD : 5Mbps  
Pin to Pin: TL

Isolation barrier:  
-1.25mm on top/bottom layer  
-0.25mm on inner layers

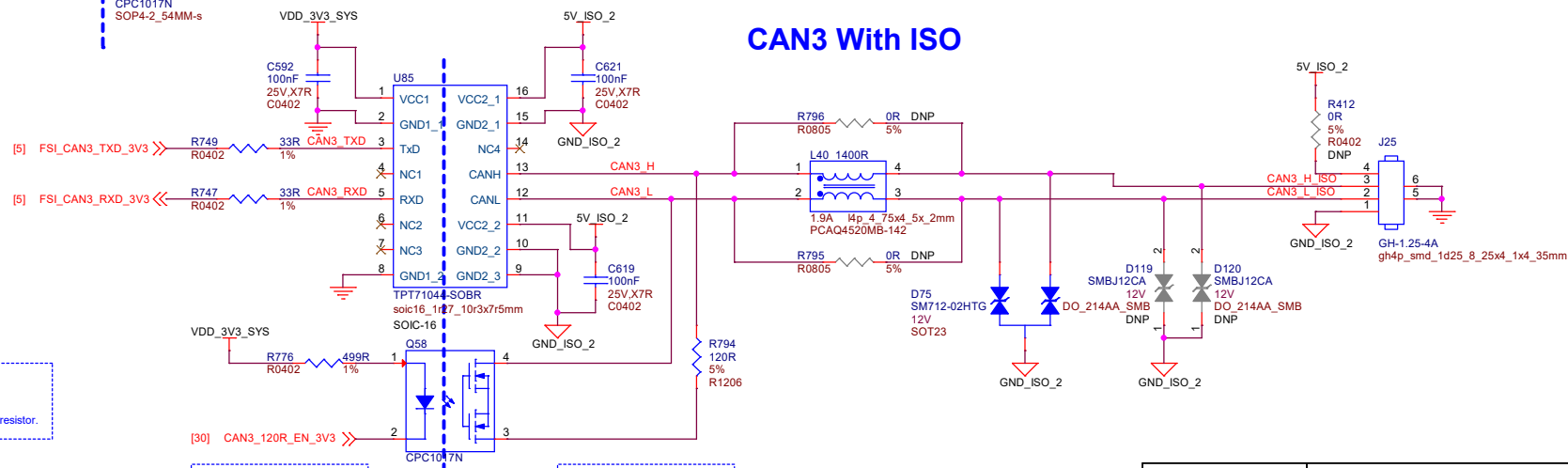
# Isolated DCDC 5V to 5V/200mA



## CAN2 With ISO



## CAN3 With ISO

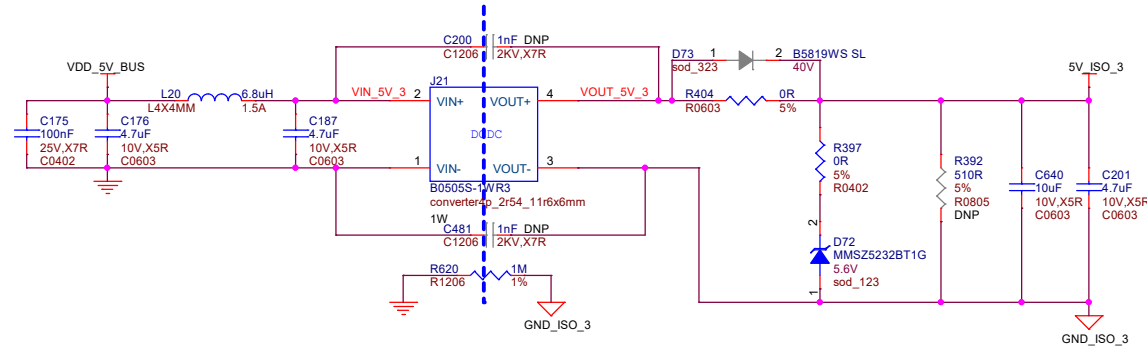


Design Note:  
Terminating Resistor Switch.  
CAN\_120R\_EN=L to enable terminating resistor.

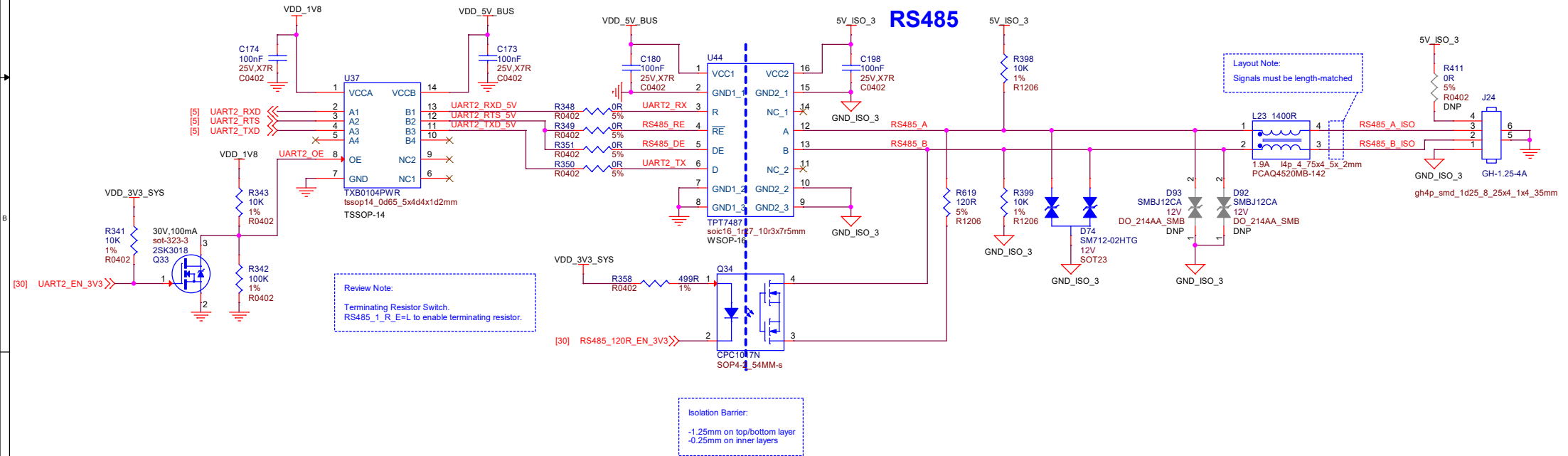
Design Note:  
CAN FD : 5Mbps  
Pin to Pin: TI/ISO1042BDWR

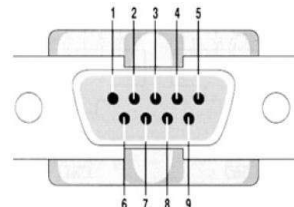
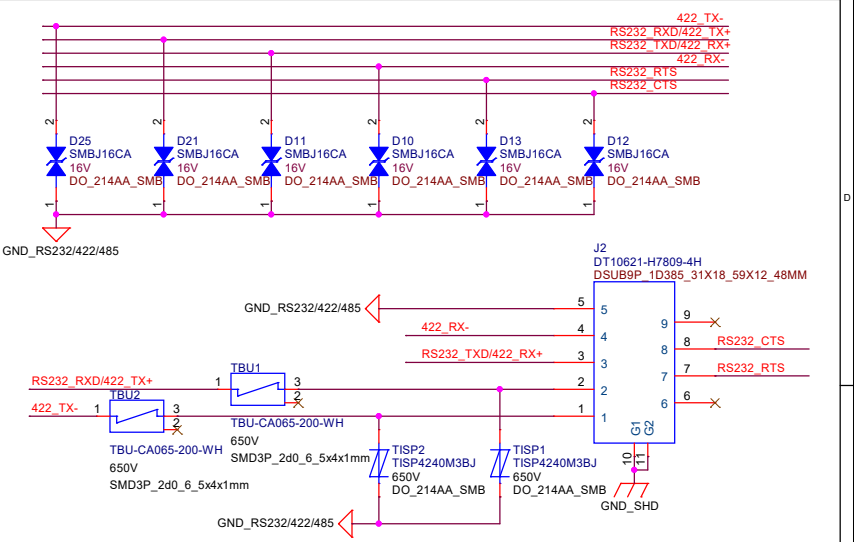
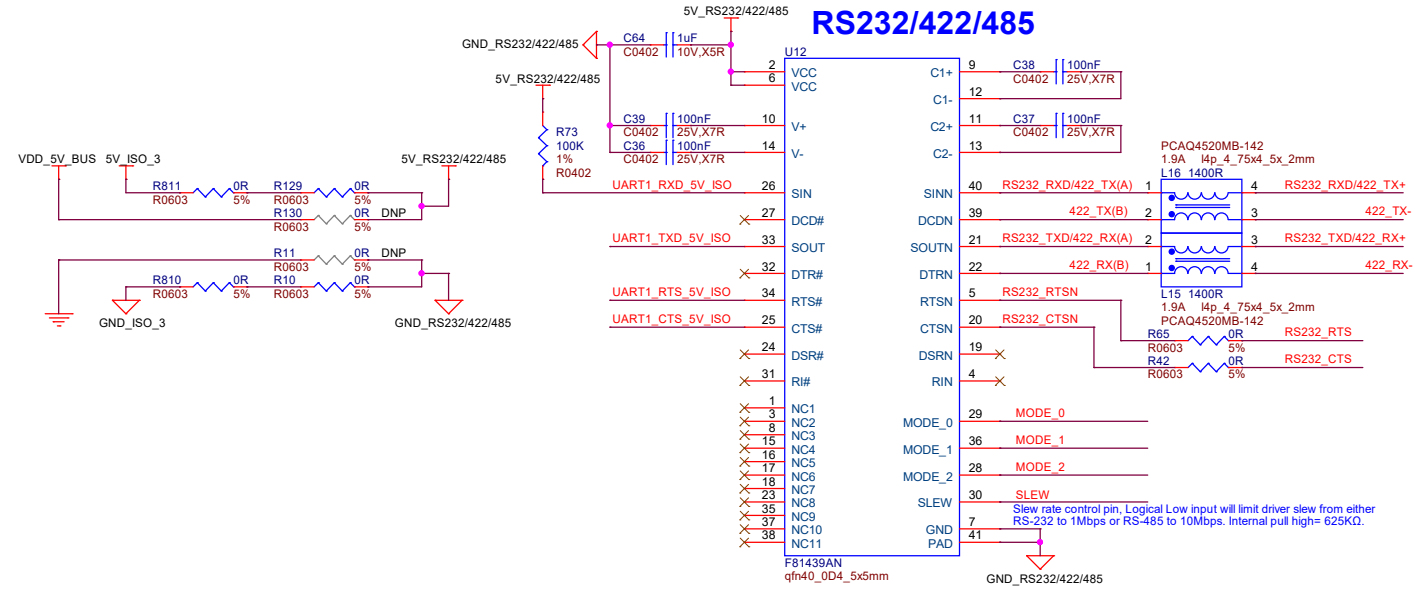
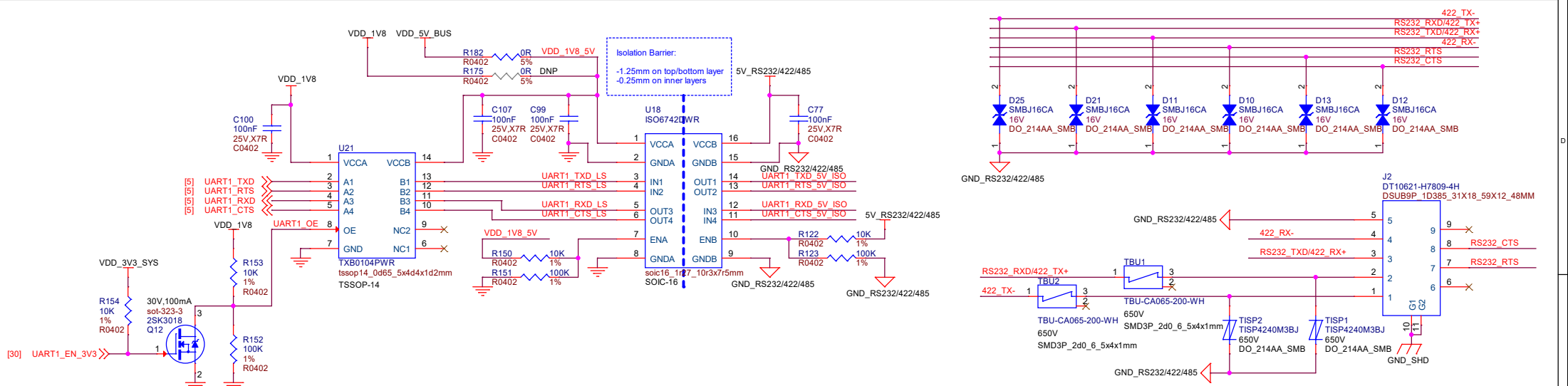
Isolation barrier:  
-1.25mm on top/bottom layer  
-0.25mm on inner layers

## Isolated DCDC 5V to 5V/200mA



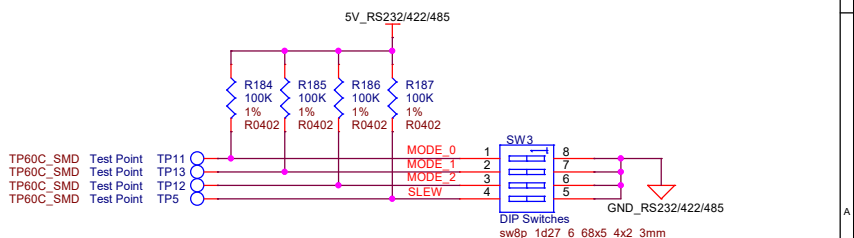
## RS485

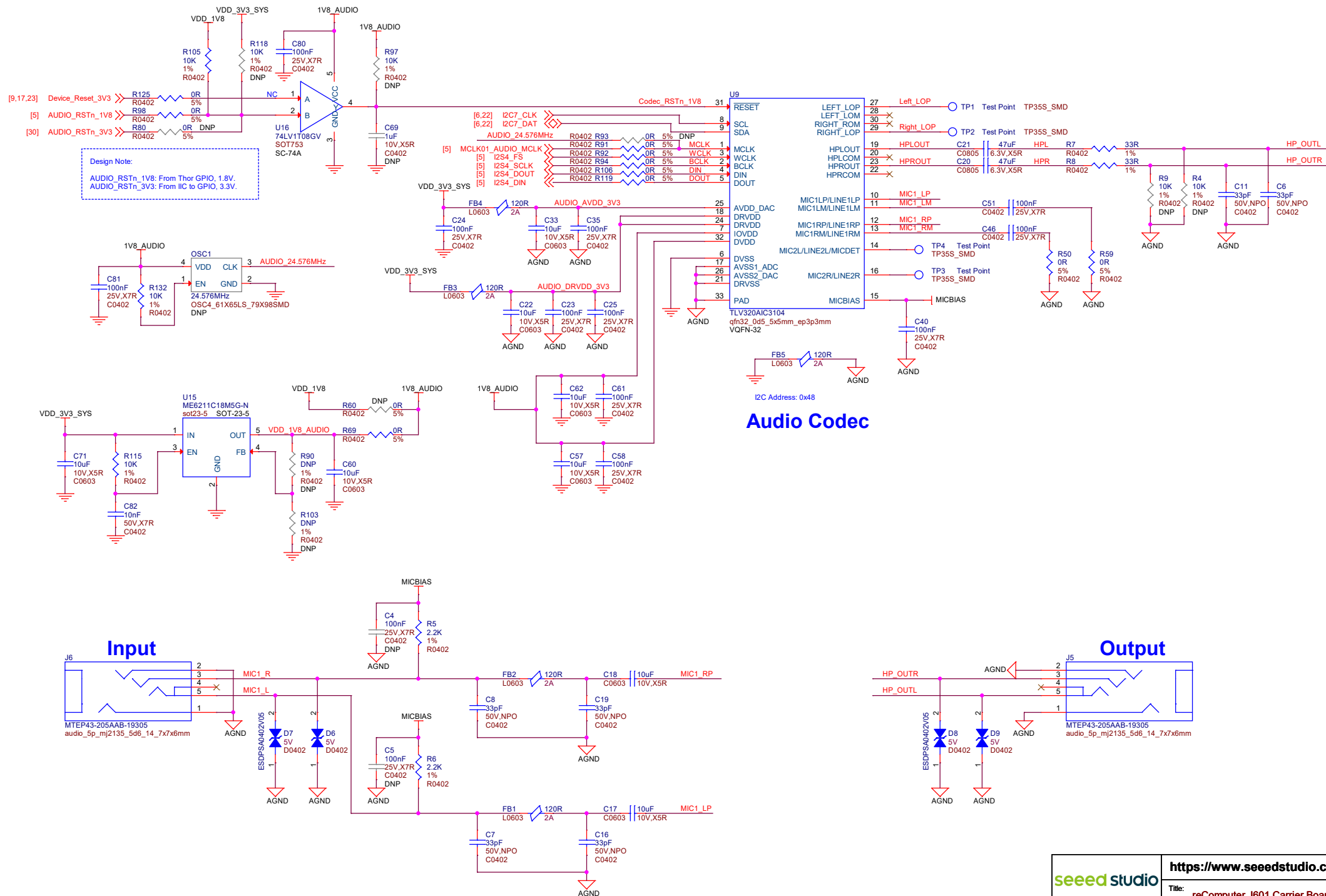




| MODE | 001   | 000/100  | 010/110   |
|------|-------|----------|-----------|
| PIN  | RS232 | RS422    | RS485     |
| 1    |       | TXD- (B) | Data- (B) |
| 2    | RXD   | TXD+ (A) | Data+ (A) |
| 3    | TXD   | RXD+ (A) |           |
| 4    |       | RXD- (B) |           |
| 5    | GND   | GND      | GND       |
| 6    |       |          |           |
| 7    | RTS   |          |           |
| 8    | CTS   |          |           |
| 9    |       |          |           |

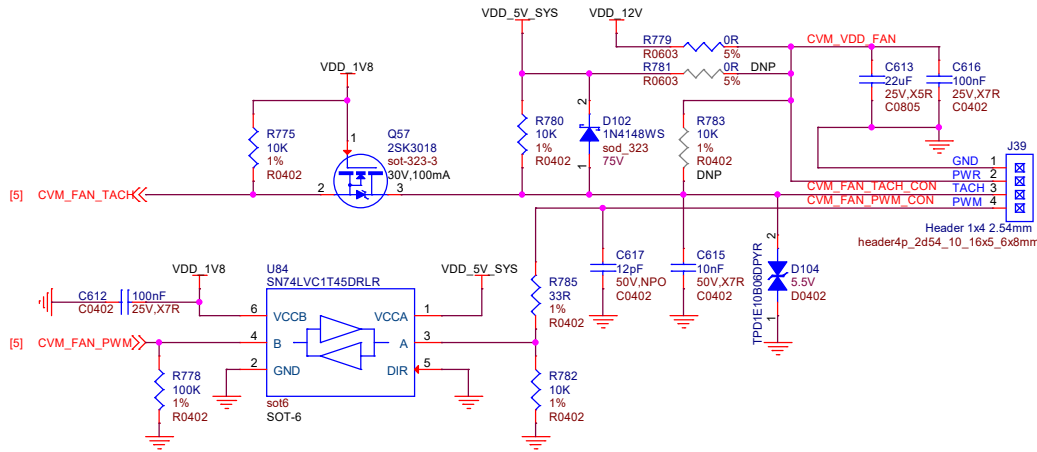
| TABLE 1: Mode Select Configuration for F81439A |                  |                  |                    |                                                           |
|------------------------------------------------|------------------|------------------|--------------------|-----------------------------------------------------------|
| Pin 29<br>MODE_0                               | Pin 36<br>MODE_1 | Pin 28<br>MODE_2 | Mode               | Status                                                    |
| 0                                              | 0                | 0                | RS-422 Full Duplex | 1T/1R RS-422                                              |
| 0                                              | 0                | 1                | Pure RS-232        | 3T/5R RS-232.                                             |
| 0                                              | 1                | 0                | RS-485 Half Duplex | 1T/1R RS-485, TX ENABLE Low Active                        |
| 0                                              | 1                | 1                | RS-485 Half Duplex | 1T/1R RS-485, TX ENABLE High Active                       |
| 1                                              | 0                | 0                | RS-422 Full Duplex | 1T/1R RS-422 with termination resistor and bias resistor. |
| 1                                              | 0                | 1                | Reserved           | Reserved                                                  |
| 1                                              | 1                | 0                | RS-485 Half Duplex | 1T/1R RS-485 with termination resistor and bias resistor. |
| 1                                              | 1                | 1                | Low Power Shutdown | All I/O pins are High Impedance                           |



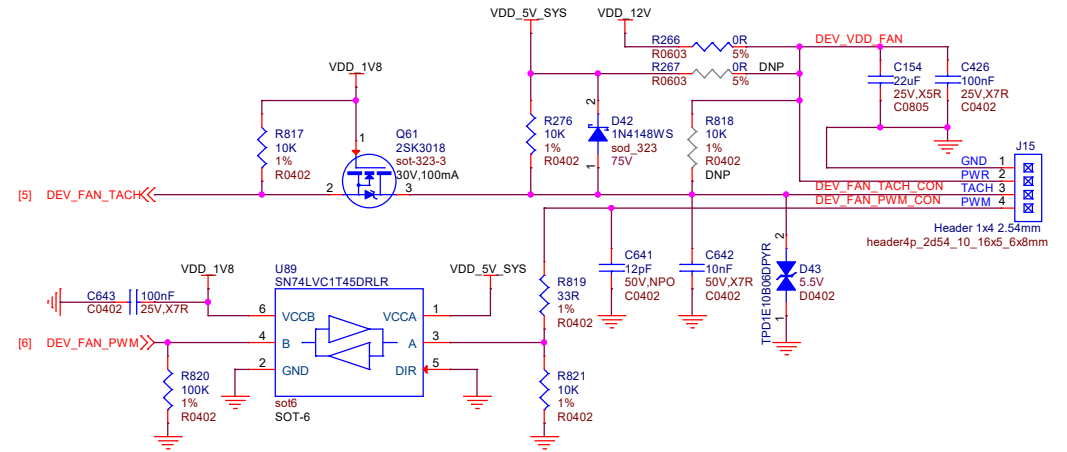




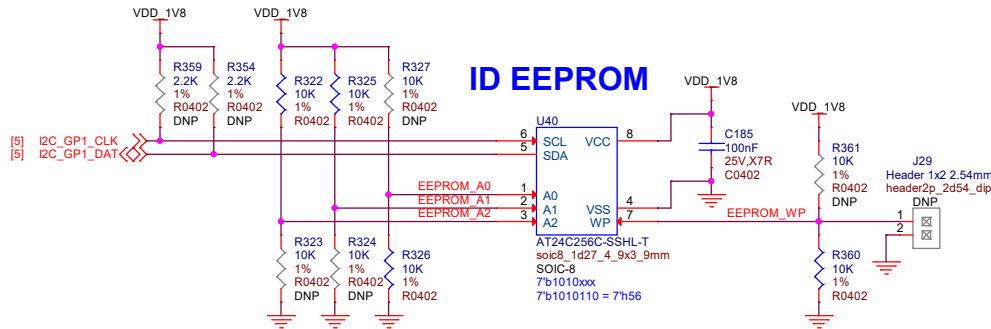
## SoC Fan Header 4pin



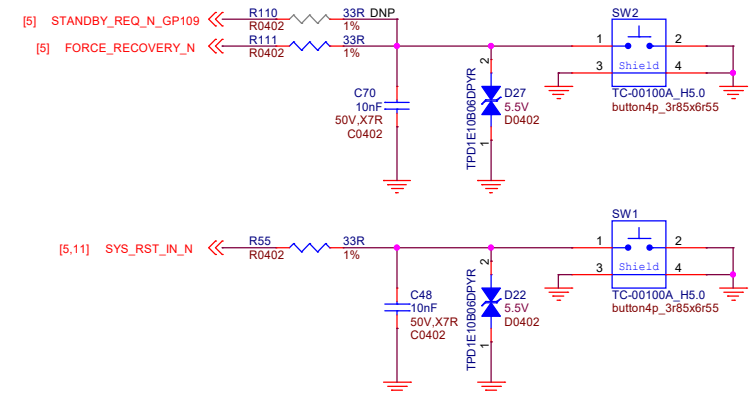
## Device Fan Header 4pin



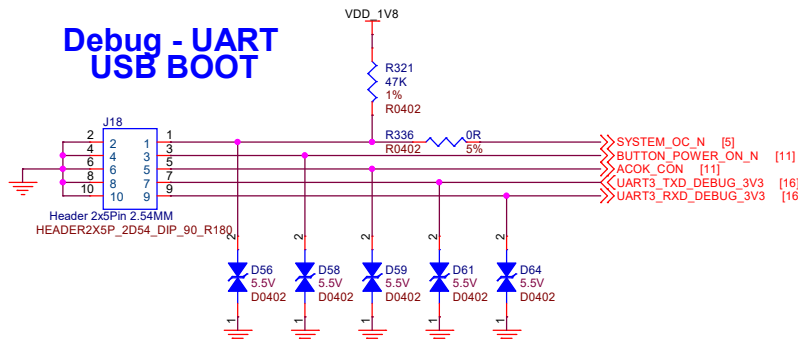
## ID EEPROM



## Button

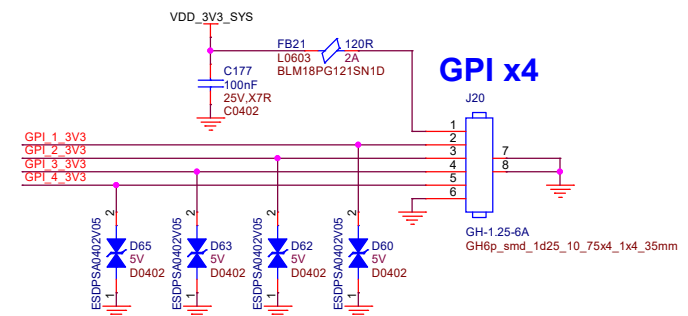
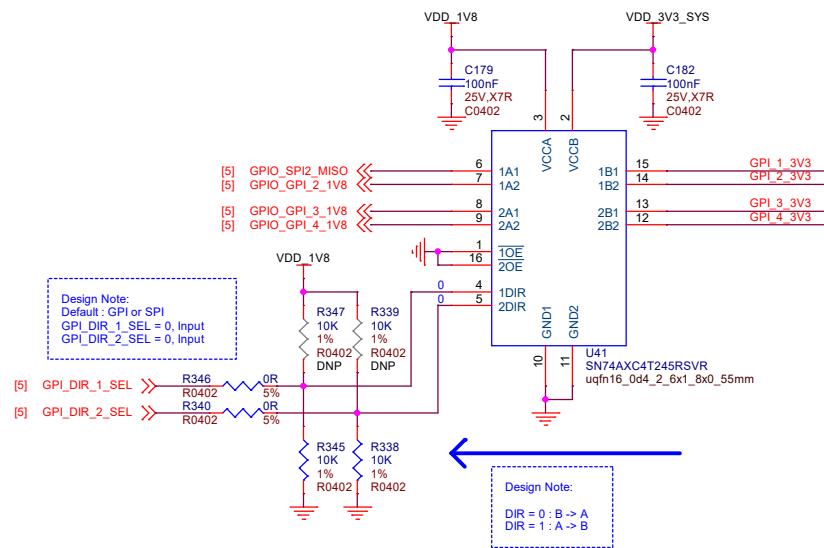
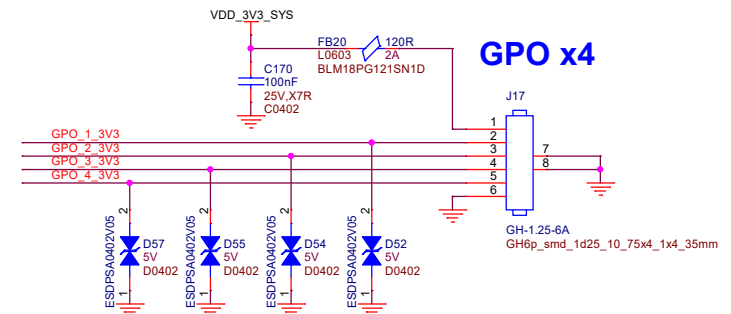
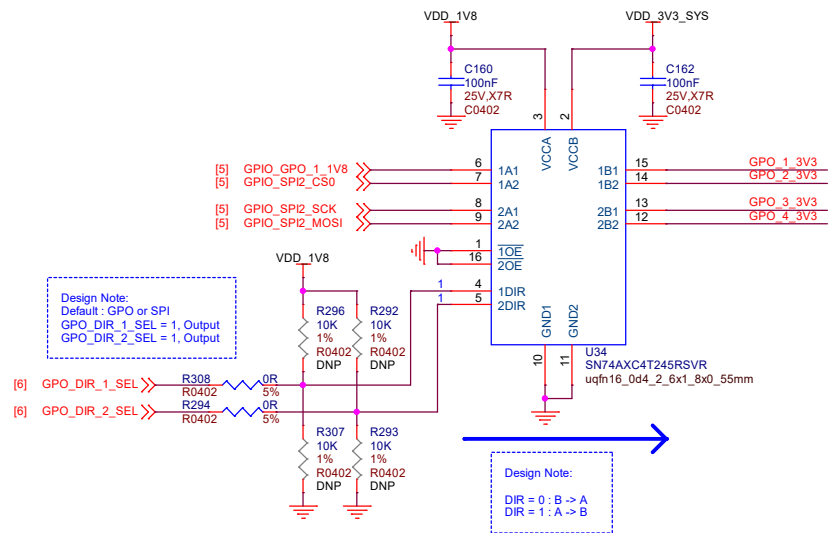


## Debug - UART USB BOOT

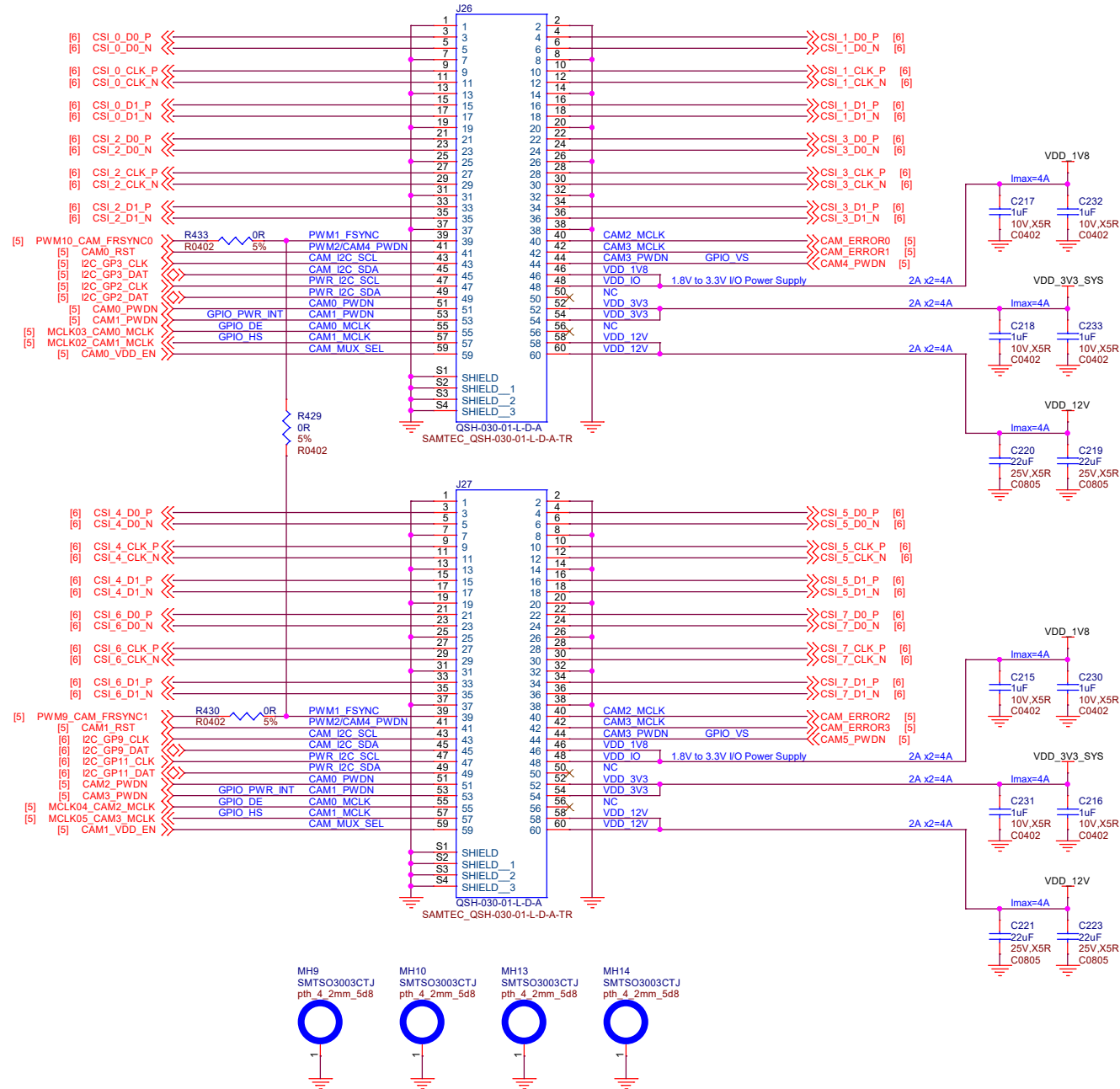








# CSI Expansion Connector



PCB1  
reComputer J601 Carrier Board PCB  
Label1  
SN Label