Specification for 13.3"EPD

Model NO.: T133A01

Product VER: A1

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver, if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
周涛涛		

Version	Content	Date	Producer
A0	New release	2025/04/09	Leslie
A1	Update Mechanical Drawing of EPD module	2025/4/24	Leslie

CONTENTS

1. General Description

T133A01 is a reflective electrophoretic E Ink® Spectra 6 technology display module based on active matrix TFT substrate. It has 13.3” active area with 1200 x 1600 pixels and 3 : 4 aspect ratios. The display is capable to display images at Black/White/Red/Yellow/Blue/Green depending on the display controller and the associated waveform file it used.

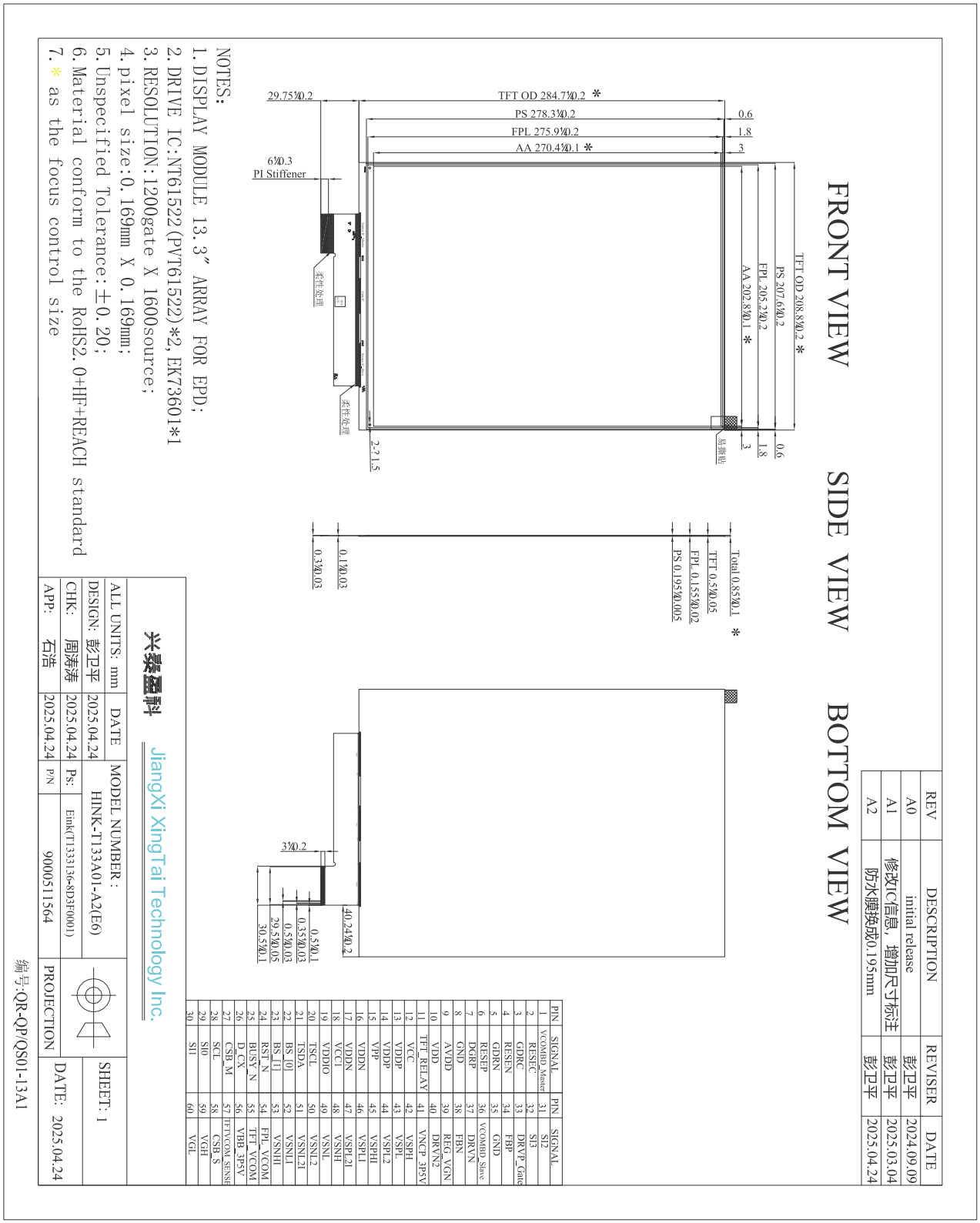
2. Features

- 1200 x 1600 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Display Black/White/Red/Yellow/Blue/Green colors
- High contrast electrophoretic imaging film
- Pure reflective mode
- Bi-stable image
- Portrait mode
- Operation temperature range: 0°C~50°C

3. General Specifications

Parameter	Specifications	Unit	Remark
Screen Size	13.3	Inch	3:4
Display Resolution	1200(H) x 1600(V)	Pixel	Dpi:150ppi
Active Area	202.8 (H) x 270.4 (V)	mm	
Pixel Pitch	0.169 x 0.169	mm	
Pixel Configuration	Square		
Outline Dimension	208.8 (H) x 284.7 (V) x 0.85(D)	mm	Without masking film
Weight	50 ± 10	g	

4. Mechanical Drawing of EPD module



REV	DESCRIPTION	REVISER	DATE
A0	initial release	彭卫平	2024.09.09
A1	修改IC信息，增加尺寸标注	彭卫平	2025.03.04
A2	防水膜换成0.195mm	彭卫平	2025.04.24

PIN	SIGNAL	PIN	SIGNAL
1	VCOMBD_Master	31	SI2
2	RESFC	32	SI3
3	GDRC	33	DRVP_Gate
4	RESFN	34	FBP
5	GDRN	35	GND
6	RESEP	36	VCOMBD_Slave
7	DGRP	37	DRVN
8	GND	38	FBN
9	AVDD	39	REG_VGN
10	VDD	40	DRVN2
11	TFT_RELAY	41	VNCP 3P5V
12	VCC	42	VSPH
13	VDDP	43	VSPL
14	VDDP	44	VSPL2
15	VPP	45	VSPHI
16	VDDN	46	VSPLI
17	VDDN	47	VSPL2I
18	VCCI	48	VSNH
19	VDDIO	49	VSNL
20	TSCL	50	VSNL2
21	TSDA	51	VSNL2I
22	BS_[0]	52	VSNLI
23	BS_[1]	53	VSNHI
24	RST_N	54	FPL_VCOM
25	BUSY_N	55	TFT_VCOM
26	D_CX	56	VBB_3P5V
27	CSB_M	57	TFTVCOM_SENSE
28	SCL	58	CSB_S
29	SI0	59	VGH
30	SI1	60	VGL

NOTES:
1. DISPLAY MODULE 13.3" ARRAY FOR EPD;
2. DRIVE IC:NT61522(PVT61522)*2, EK73601*1
3. RESOLUTION:1200gate X 1600source;
4. pixel size:0.169mm X 0.169mm;
5. Unspecified Tolerance:±0.20;
6. Material conform to the RoHS2.0+HF+REACH standard
7. * as the focus control size

米矽盛科 JiangXi XingTai Technology Inc.			
ALL UNITS: mm	DATE	MODEL NUMBER : HINK-T133A01-A2(E6)	SHEET: 1
DESIGN: 彭卫平	2025.04.24		
CHK: 周涛涛	2025.04.24	Ps: Eink(T133136-8D3F0001)	
APP: 石浩	2025.04.24	P/N 9000511564	PROJECTION
			DATE: 2025.04.24

编号:QR-QP/QS01-13A1

5. Input / Output Interface

5-1) Connector type

Service	Connector	Type Number	Number of Pins	Mating Connector
Interface	P-TWO	9000511564	60	Copper foil 0.5mm pitch

5-2) Pin Assignment

Pin Assignment			
Pin #	**Type**	**Single**	**Description**
1	P	VCOMBD_M	VCOMBD driving voltage (Master)
2	I	RESEC	Current sense input pin for the control loop.(VCOM)
3	O	GDRC	N-Channel MOSFET gate drive control.(VCOM)
4	I	RESEN	Current sense input pin for the control loop. (VDDN)
5	O	GDRN	P-Channel MOSFET gate drive control pin. (VDDN)
6	I	RESEP	Current sense input pin for the control loop. (VDDP)
7	O	GDRP	N-Channel MOSFET gate drive control pin. (VDDP)
8	P	GND	Ground
9	P	AVDD	Analog voltage supply.(DC/DC)
10	P	VDD	Analog /digital voltage supply.
11		NC	No connection and do not connect with other NC pins
12	P	VCC	LDO output pin.
13	P	VDDP	Positive power supply for analog circuit. (+16V ~ +19V)
14	P		
15		NC	No connection and do not connect with other NC pins
16	P	VDDN	Negative power supply for analog circuit. (-19V ~ -16V)
17	P		
18	P	VCC1	Positive power supply only for Oscilltor.

19	P	VDDIO	Power input for IO.
20	I/O	TSCL	I2C Interface to digital temperature sensor Clock pin
21	I/O	TSDA	I2C Interface to digital temperature sensor Data pin
22	I	BS0	Input interface setting. Select 3 wire/ 4 wire/ **Quad** SPI interface.**(Default :H)**
23	I	BS1	Input interface setting. Select 3 wire/ 4 wire/ **Quad** SPI interface.**(Default :H)**
24	I	RES#	Reset.
25	O	BUSY_N	This pin indicates the driver status. Connect with a pull up resistor to VDDIO. BUSY_N = "0" ： Driver is busy, data/VCOM is transforming. BUSY_N = "1" ： Non-busy. Host side can send command/data to driver.
26	I	D/C#	Command/Data input. L: command H: data. (4-wire SPI). Connect to GND in 3-wire mode or standard 4-wire mode.
27	I	CSB_M	Serial communication chip select.(Master)
28	I	SCL	Serial communication clock input.
29	I/O	SI0	Serial communication data input/output (3-wire/4-wire SPI). Serial communication data input (Standard 4-wire SPI).
30	I/O	SI1	Serial communication data input. Serial communication data output. (Standard 4-wire SPI).
31	I	SI2	Serial communication data input. (Standard 4-wire SPI Quad mode)
32	I	SI3	Serial communication data input. (Standard 4-wire SPI Quad mode)
33	O	DRVP_Gate	Driving external N-MOSFET(VGP)
34	I	FBP	Positive charge pump(VGP) feedback pin.
35	P	GND	Ground
36	O	VCOMBD_S	VCOMBD driving voltage (Slave)
37	O	DRVN	Driving external BTJ. (VGN)
38	I	FBN	Negative charge pump feedback pin. (VGN)
39	O	REG_VGN	VGN internal reference voltage output.

40	O	DRVN2	Driving external BTJ. (VNCP_3P5V)
41	P	VNCP_3P5V	Negative power supply for analog bias1 circuit. (for TFT_Vcom) -3.5V deviation +/- 4.5%
42	P	VSPH	Positive source buffer output.
43	P	VSPL	Positive source buffer output.
44	P	VSPL2	Positive source buffer output.
45	P	VSPHI	Positive source voltage.
46	P	VSPLI	Positive source voltage.
47	P	VSPL2I	Positive source voltage.
48	P	VSNH	Negative source buffer output.
49	P	VSNL	Negative source buffer output.
50	P	VSNL2	Negative source buffer output.
51	P	VSNL2I	Negative source voltage.
52	P	VSNLI	Negative source voltage.
53	P	VSNHI	Negative source voltage.
54	O	FPL_VCOM	FPL_VCOM driving voltage
55	O	TFT_VCOM	TFT_VCOM driving voltage
56	P	VBB_3P5V	Negative power supply for analog bias2 circuit. (for TFT_Vcom) -3.5V deviation +/- 4.5%
57	-	NC	No connection and do not connect with other NC pins
58	I	CSB_S	Serial communication chip select.(Slave)
59	P	VGH	Positive Gate driving voltage
60	P	VGL	Negative Gate driving voltage

Note 5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY_N) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

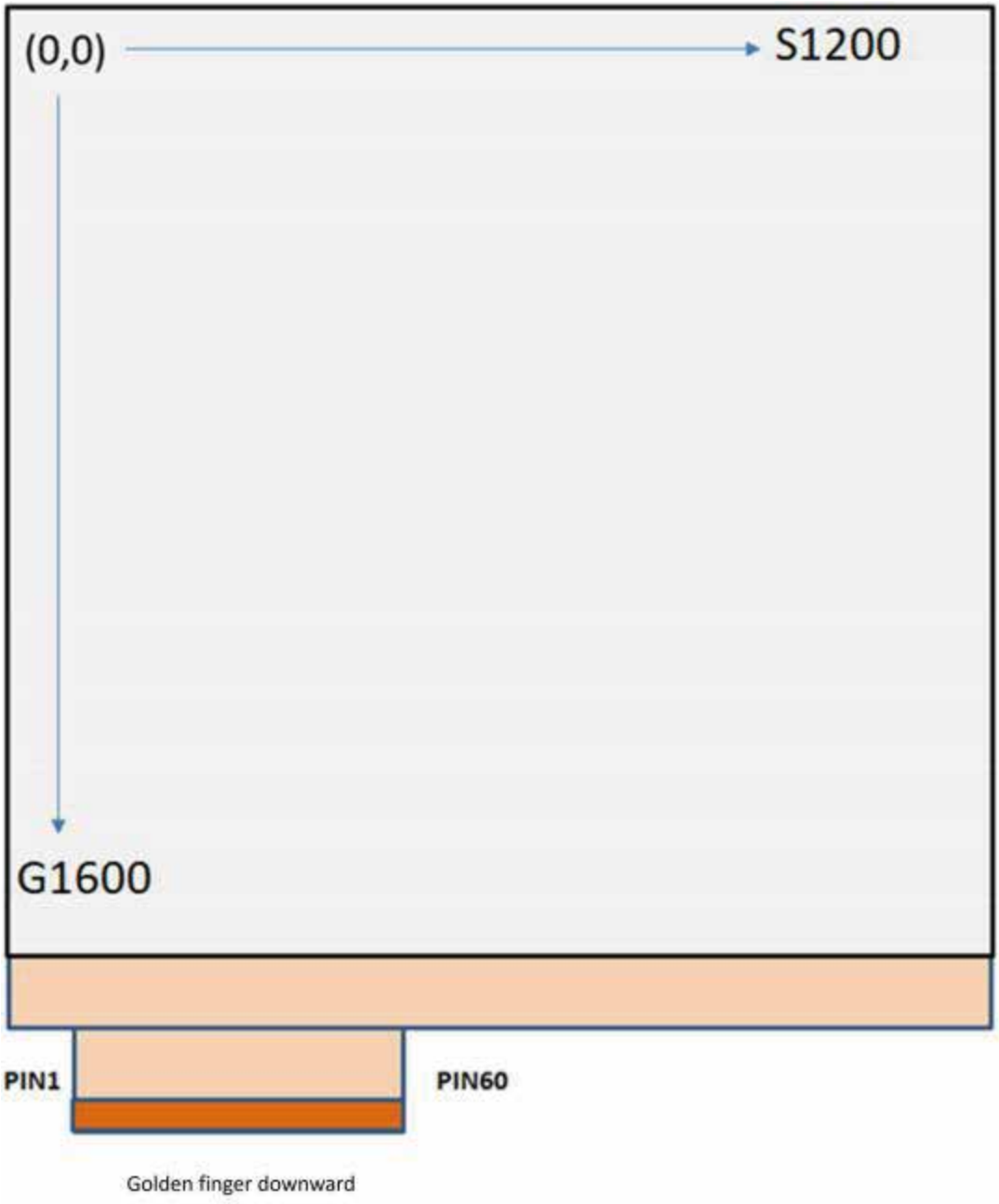
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS0/BS1) is for 3-line SPI /4-line SPI/QSPI selection. Please refer to below Table..

Table: Bus interface selection

BS1	BS0	MPU Interface
L	L	3-lines serial peripheral interface (SPI) – 9 bits SPI
L	H	4-lines serial peripheral interface (SPI)
H	L	Standard 4-wire SPI
H	H	Standard 4-wire SPI (Default)

5-3) Panel Scan Directions



6. Electrical Characteristics

6-1 Absolute Maximum Ratings:

Parameter	Symbol	Rating	Unit
Analog power	VDD	-0.5 to +3.6	V

Note: Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

6-2 Display Module DC characteristics

Display Module DC characteristics: Please follow the table for the normal operation of the panel; otherwise, it may influence the panel's optical performance.

The standby power (P_{STBY}) is the consumed power when the panel controller is in standby mode. This value is only for reference since it depends on the performance of the panel controller (Whether there is wireless transmission function (WiFi & BLE) will seriously affect the power consumption.)

The following specifications apply for: VDD = 3.3V, TA = 25℃

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic supply voltage	VDD		2.4	3.3	3.6	V
IO supply voltage	VDDIO		2.4	3.3	3.6	V
DCDC power input voltage	AVDD		2.4	3.3	6.0	V
LDO output	VCC		1.2	1.3	1.4	V
Oscillator supply voltage	VCC1		1.2	1.3	1.4	V
Positive Gate driving voltage	VGH		26.0	27.0	28.0	V
Negative Gate driving voltage	VGL		-21.0	-20.0	-19.0	V
Positive source buffer output	VSPH		--	Adjusted	--	V
Positive source buffer output	VSPL		--	Adjusted	--	V
Positive source buffer output	VSPL2		--	Adjusted	--	V
Positive source voltage.	VSPHI		--	Adjusted	--	V
Positive source voltage.	VSPLI		--	Adjusted	--	V
Positive source voltage.	VSPL2I		--	Adjusted	--	V
Negative source buffer output	VSNH		--	Adjusted	--	V
Negative source buffer output	VSNL		--	Adjusted	--	V
Negative source buffer output	VSNL2		--	Adjusted	--	V
Negative source voltage	VSNL2I		--	Adjusted	--	V
Negative source voltage	VSNLI		--	Adjusted	--	V

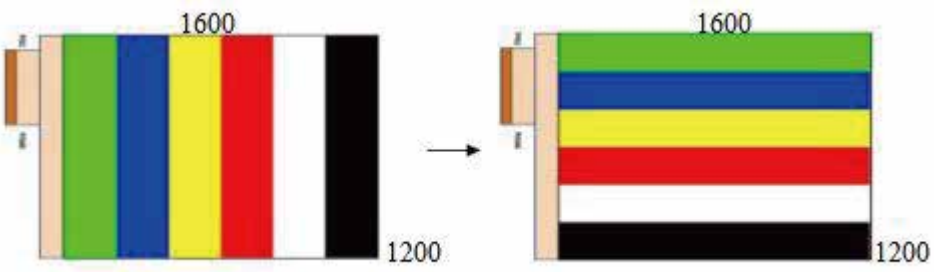
Negative source voltage	VSNHI		--	Adjusted	--	V
VCOM_DC output voltage	VCOM_DC		-4.0	Adjusted	-0.3	V
Low level input voltage	V_{IL}	Digital input pins	GND	--	0.2xVDD	V
High level input voltage	V_{IH}	Digital input pins	0.8xVDD	--	VDD	V
High level output voltage	V_{OH}	Digital output pins, I_{OUT} = 1 mA,VDD =	0.8xVDD	--	--	V

Note: The Module operating current data is measured by using Oscilloscope, and extract the Mean value.

- The typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal color stripe pattern to vertical color stripe pattern. (Note 6-1)
- The high loading power consumption is measured using associated 25℃ waveform with following pattern transition: from full white pattern to noise pattern (including random scattering of4 colors) (Note 6-2)
- The minimum VDD value by 2.4V is based on typical application pattern with stable and continuing power supply. It does not apply on high loading pattern such as Note 6-2.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink
- Vcom value has been set in the IC chip on the panel.
- Issue the command 0x07 with data 0xA5 to let EPD enter deep sleep mode.

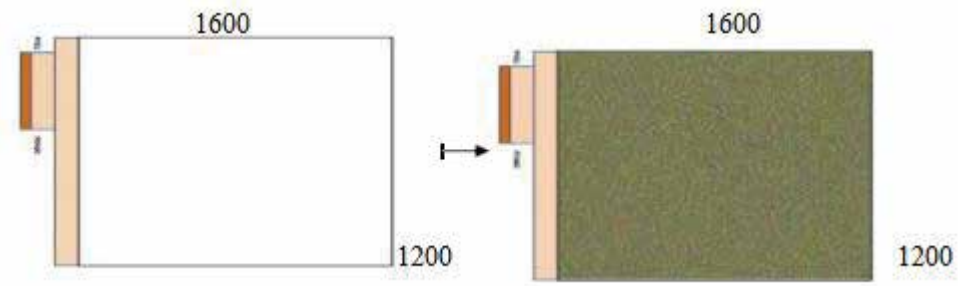
Note 6-1

The typical power consumption



Note 6-2

The high loading power consumption



6-3 Panel AC Characteristics

6-3-1 MCU Interface

6-3-1-1 MCU Interface Selection

In this module, there are 3-wire SPI, 4-wire SPI and standard 4-wire SPI that can communicate with MCU. The

MCU interface mode can be set by hardware selection on BS0 and BS1 pins. Please refer to the following table to

select the bus interface.

Pin Name	Bus Selection		Data/Command Interface		Control Signal		
Bus interface	BS0	BS1	SDA	SCL	CS#	D/C#	RES#
3-wire SPI	L	L	SDIN/OUT	SCLK	CS#	N/A	RES#
4-wire SPI	H	L	SDIN/OUT	SCLK	CS#	L ： Command Input H ： Data Input	RES#
Standard 4-wire SPI	H	H	MOSI ： SDOUT MISO ： SDIN	SCLK	CS#	N/A	RES#

Table 6-1: MCU interface assignment under different bus interface mode Note 6-3: L is connected to GND

Note 6-4: H is connected to VDD

Note 6-5: Suggest Updated once a day;

6-3-1-2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDA, D/C#, CS#.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 6-2: Control pins of 4-wire Serial Peripheral interface

Note 6-5: ↑stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

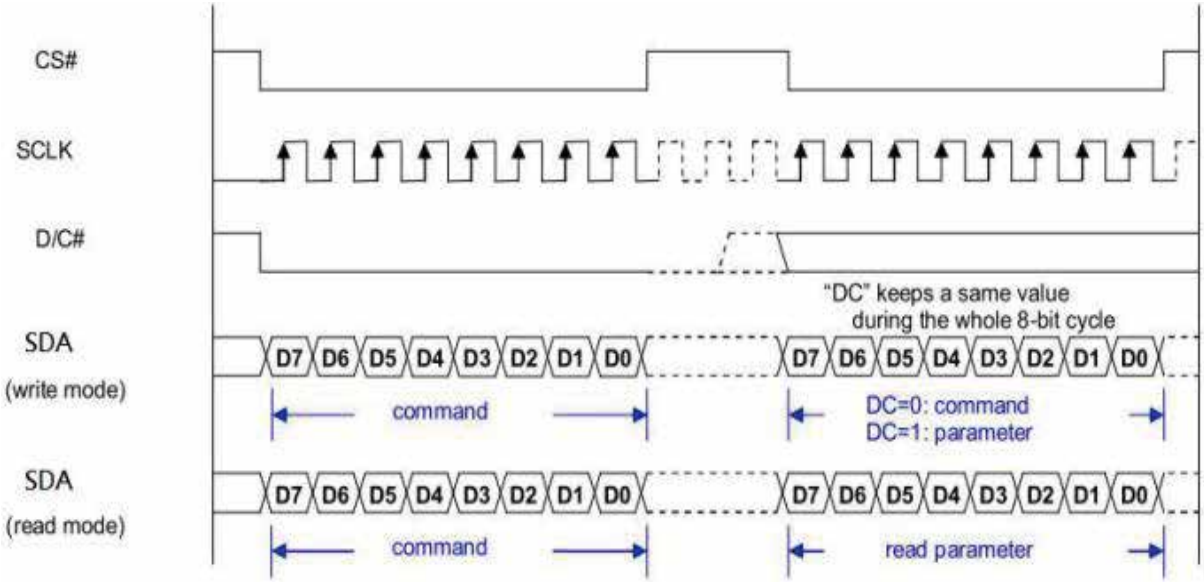


Figure 6-1: Write procedure in 4-wire Serial Peripheral Interface mode

6-3-1-3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDA and CS#.

In 3-wire SPI mode, the pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be

shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tied to GND	↑
Write data	L	Tied to GND	↑

Table 6-3: Control pins of 3-wire Serial Peripheral Interface

Note 6-6: ↑stands for rising edge of signal

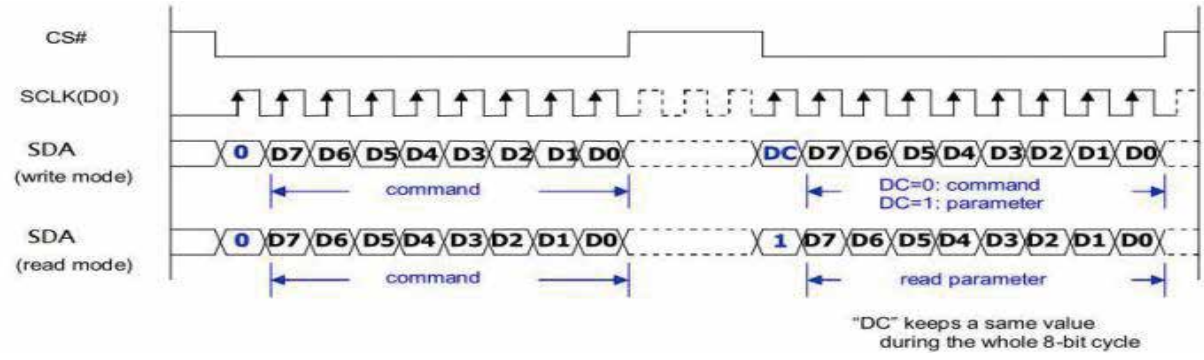
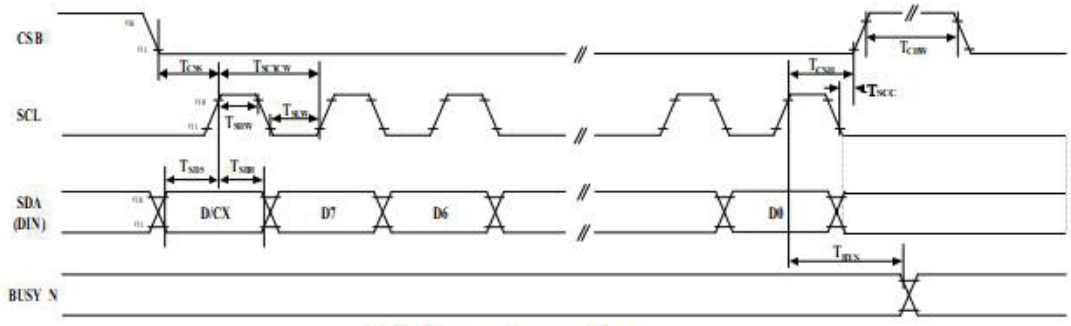


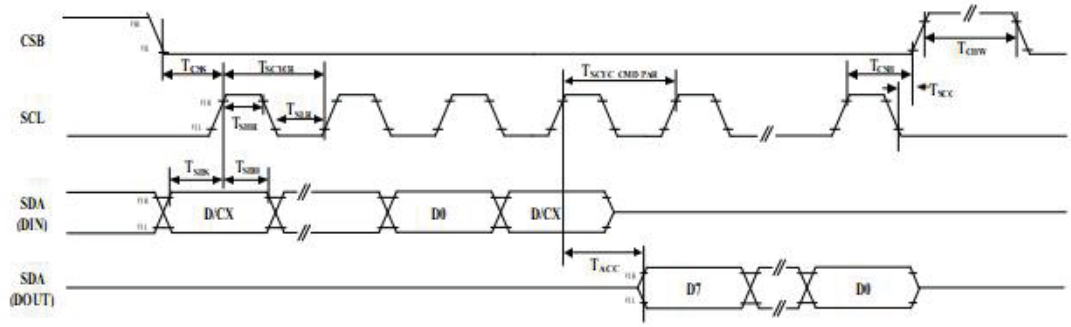
Figure 6-2: Write procedure in 3-wire Serial Peripheral Interface mode

6-3-2 Timing Characteristics of Series Interface

6-3-2-1 3-wire SPI

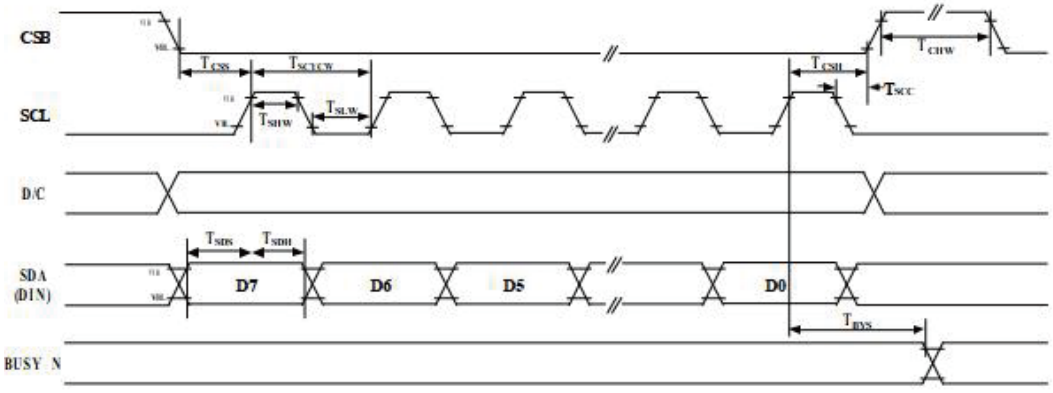


3 pin serial interface characteristics (write mode)

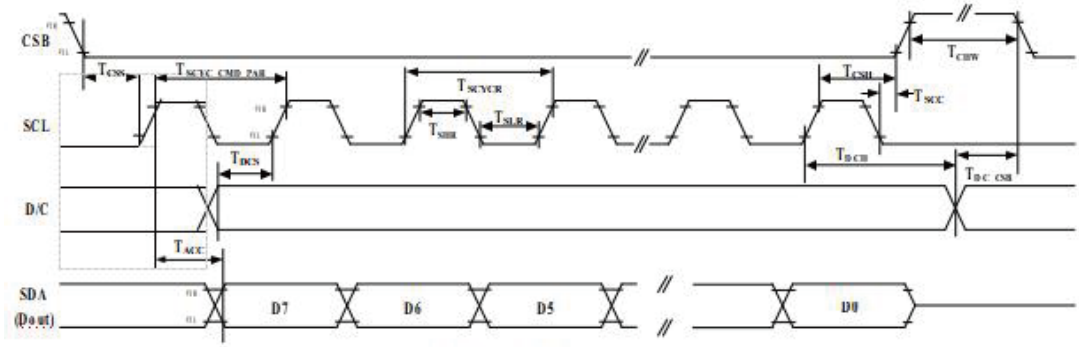


3 pin serial interface characteristics (read mode)

6-3-2-2 4-wire SPI

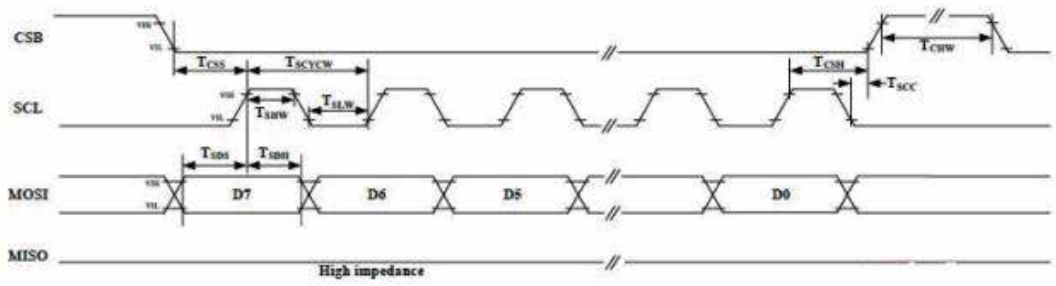


4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)

6-3-2-3 Standard 4-wire SPI



Standard 4 pin serial interface characteristics

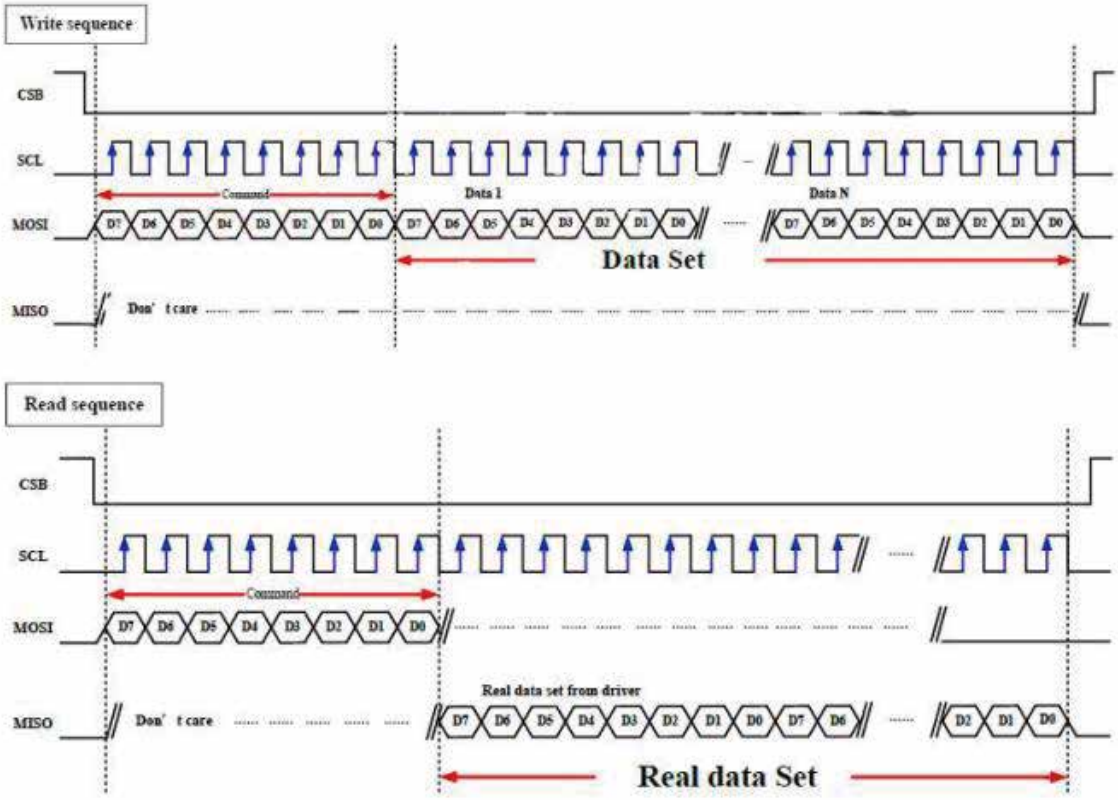


Figure ： Standard 4 pin serial interface protocol

Table 3-wire Timing Table

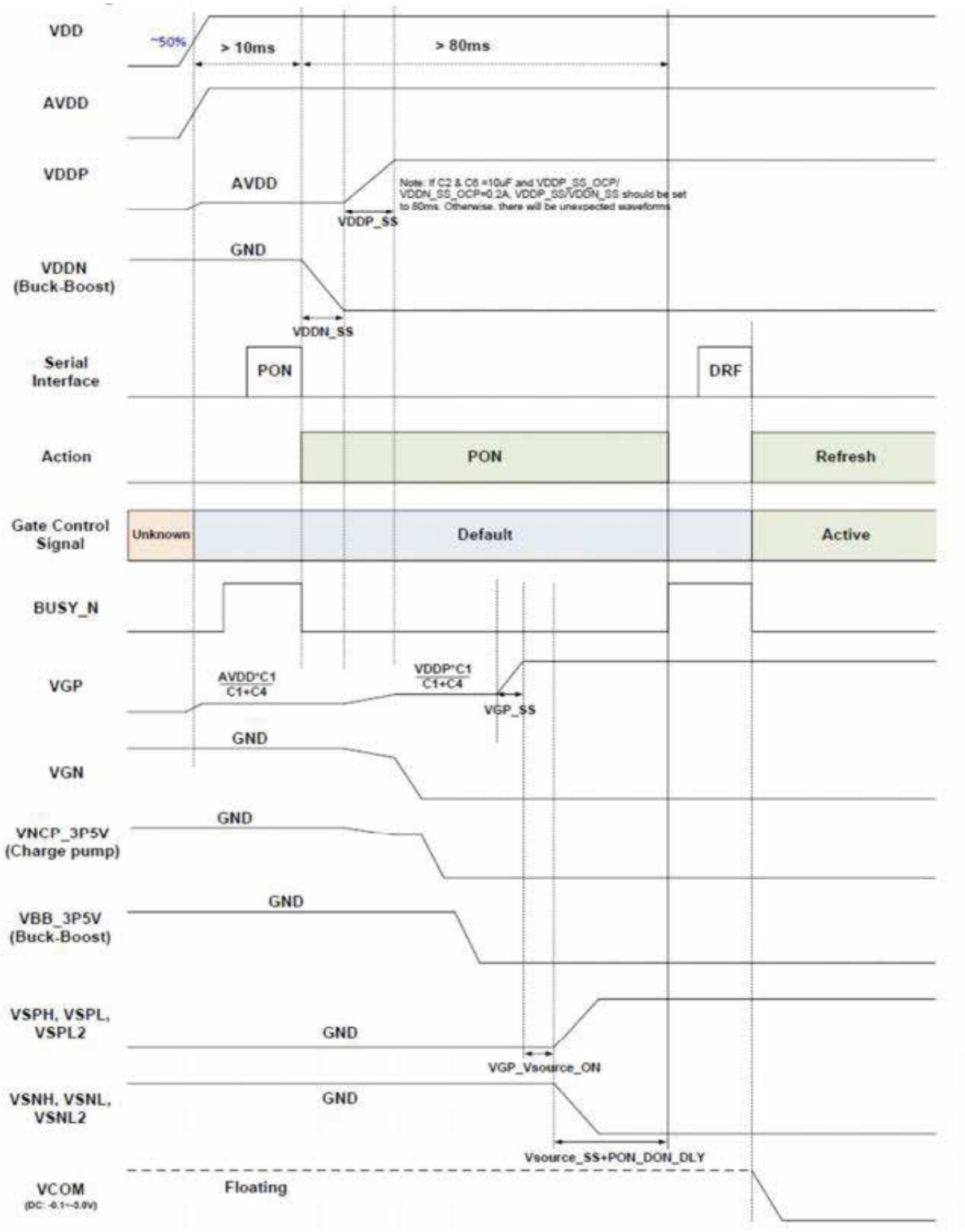
Parameter	Symbol	Min	Typ	Max	Unit	condition
SERIAL COMMUNICATION						
CSB	Tcss	60			ns	Chip select setup time
	Tcsh	65			ns	Chip select hold time
	Tscc	20			ns	Chip select setup time
	Tchw	40			ns	Chip select setup time
SCL	Tscycw	50			ns	Serial clock cycle (Write)
	Tshw	25			ns	SCL “H” pulse width (Write)
	Tslw	25			ns	SCL “L” pulse width (Write)
	Tscycr	150			ns	Serial clock cycle (Read)
	Tshr	60			ns	SCL “H” pulse width (Read)
	Tslr	60			ns	SCL “L” pulse width (Read)
	TSCYC_CMD_PAR	150			ns	Serial clock cycle (Between command and 1st parameter)
SDA	Tsds	30			ns	Data setup time
	Tsdh	30			ns	Data hold time
	TACC			140	ns	Access time
BUSY_N	TBYS			150	ns	BUSY_N setup time

Table 4-wire Timing Table

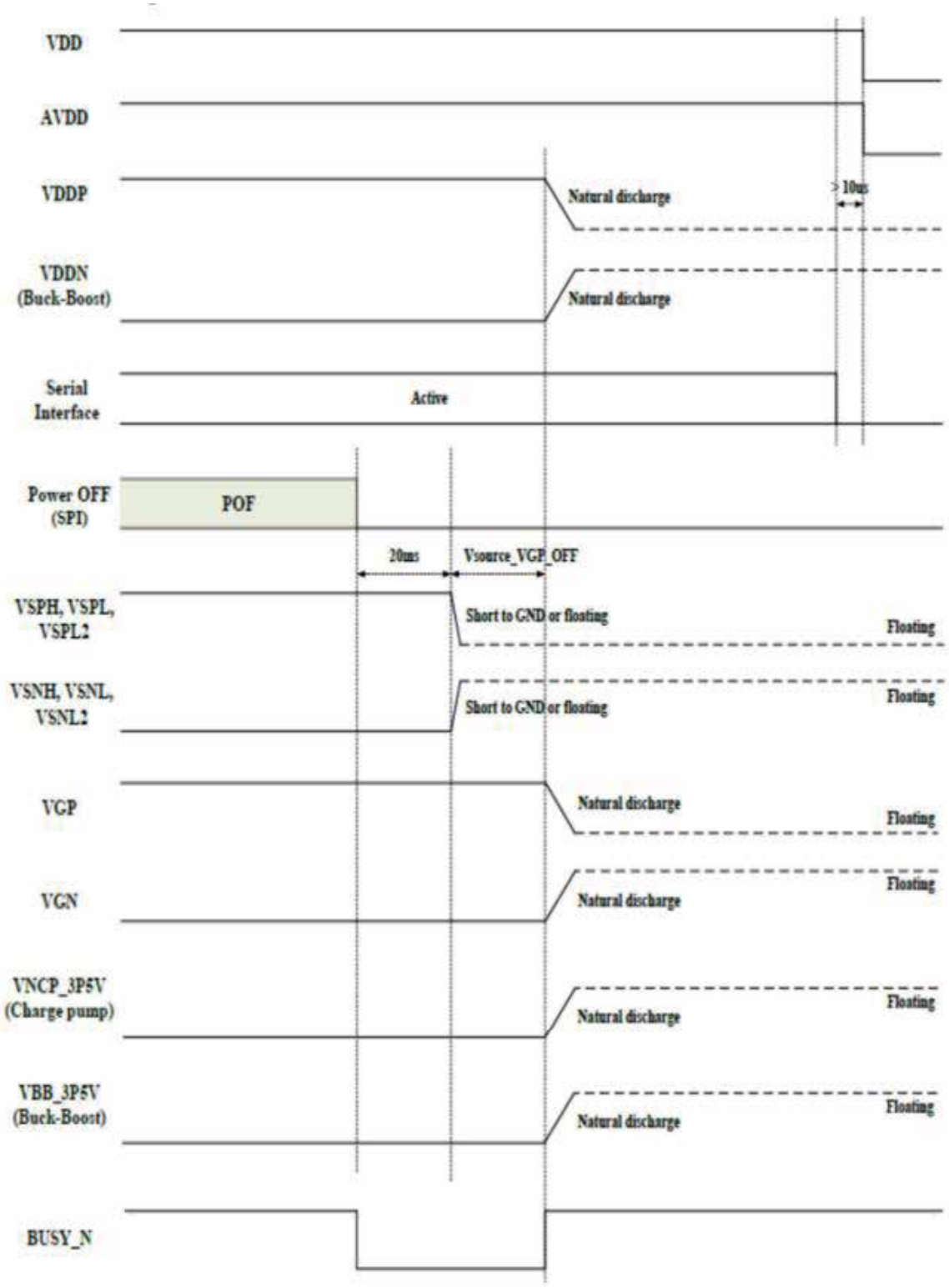
Parameter	Symbol	Min	Typ	Max	Unit	condition
SERIAL COMMUNICATION						
CSB	Tcss	60			ns	Chip select setup time
	Tcsh	65			ns	Chip select hold time
	Tscc	20			ns	Chip select setup time
	Tchw	40			ns	Chip select setup time
SCL	Tscycw	50			ns	Serial clock cycle (Write)
	Tshw	25			ns	SCL “H” pulse width (Write)
	Tslw	25			ns	SCL “L” pulse width (Write)
	Tscycr	150			ns	Serial clock cycle (Read)
	Tshr	60			ns	SCL “H” pulse width (Read)
	Tslr	60			ns	SCL “L” pulse width (Read)
	$T_{SCYC\_CMD\_PAR}$	150			ns	Serial clock cycle (Between command and 1st parameter)
SDA	Tsds	30			ns	Data setup time
	Tsdh	30			ns	Data hold time
	T_{ACC}			140	ns	Access time
BUSY_N	T_{BYS}			150	ns	BUSY_N setup time

7. Power Characteristics

Power ON Sequence



Power OFF Sequence



8. Optical Characteristics

8-1 Specifications

Symbol	Parameter	Conditions	Temperature	Min	Typ.	Max	Unit	Note
R	Reflectance	White	25°C	30	34	-	%	Note 8-1
CR	Contrast Ratio	-	25°C	15	22	-	-	-
T_{update}	Update time	-	25°C	-	12	-	sec	-

Symbol	Parameter	Conditions	Temperature	L* Typ.	a* Typ.	b* Typ.	△E2000 Max.	Note
WS	White State L*/a*/b* value	White	25°C	66.5	-4	0	6	Note 8-1
DS	Dark State L*/a*/b* value	Dark	25°C	12	7	-11	6	Note 8-1
RS	Red State L*/a*/b* value	Red	25°C	26.5	41	30	6	Note 8-1
YS	Yellow State L*/a*/b* value	Yellow	25°C	62	-11	65	6	Note 8-1
BS	Blue State L*/a*/b* value	Blue	25°C	34	3.5	-37	6	Note 8-1
GS	Green State L*/a*/b* value	Green	25°C	35	-22	15	8	Note 8-1

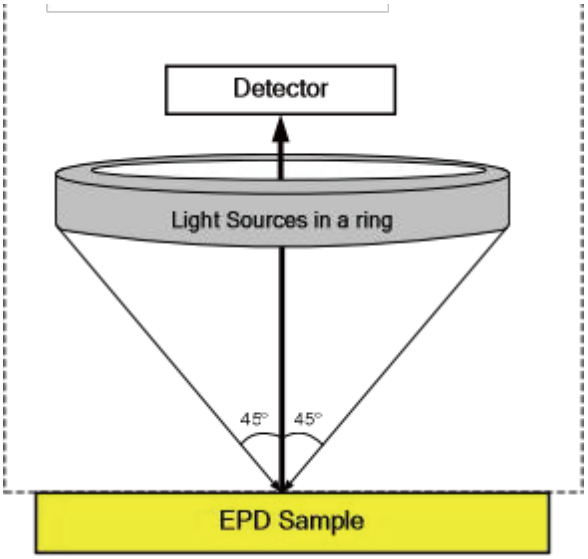
WS: White state, DS: Dark state, RS: Red state, YS: Yellow state, BS: Blue state, GS:Green state

Note 8-1 ： Luminance meter ： Eye - One Pro3 plus Spectrophotometer

8-2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd) ：

CR = Rl/Rd



8-3 Reflection Ratio

The reflection ratio is expressed as：

R = Reflectance Factor white board x (Lcenter / Lwhite board)

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9.Handling,Safety, and Environment Requirements and Remark

WARNING
The display may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
4) Acetic acid type and chlorine type materials for the cover case are not desirable because he former generates corrosive gas of attacking the PS at high temperature and the latter cause's circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other condition these are stress ratings only

Application information
Where application information is given, it is advisory and does not form part of the specification

10.Reliability Test

	TEST	CONDITION	REMARK
1	High Temperature Storage	T = 60℃35% RH, 240Hrs Test in White pattern	ongoing
2	Low Temperature Storage	T = -25℃, 240Hrs Test in White pattern	ongoing
3	High Temperature Operation	T = 50℃30% RH, 240Hrs 150s interval between updates	ongoing
4	Low Temperature Operation	T = 0℃, 240Hrs 150s interval between updates	ongoing
5	High-Temperature, High-Humidity Operation	T = +40℃, RH = 90%, 240Hrs 150s interval between updates	ongoing
6	High Temperature, High-Humidity Storage	T = 60℃ 80% RH, 240Hrs Test in White pattern	ongoing
7	Heat Shock	-25℃(30 min) ~60℃(30 min) 50 cycle, 1Hr/cycle Test in White pattern	ongoing
8	Electrostatic Discharge	(Machine model) +/- 200V ; 0Ω, 200pF	ongoing

Actual EMC level to be measured on customer application.

Note：

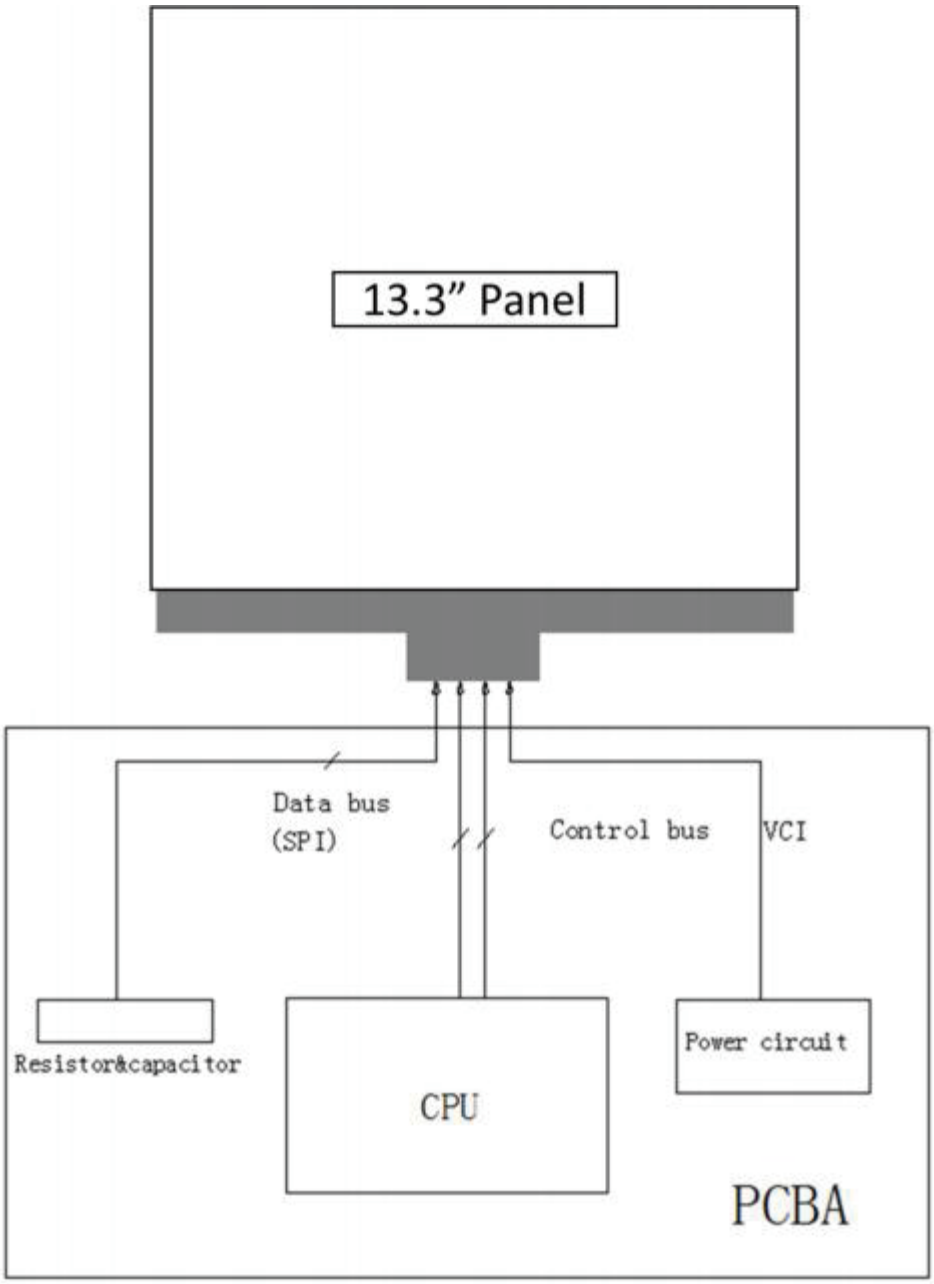
1. The protective film must be removed before temperature test.
2. For operation test, image update interval time 150s

< Criteria >

In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

3. Reliability verification of new products is ongoing, and this reliability condition is not considered as a final reliability result

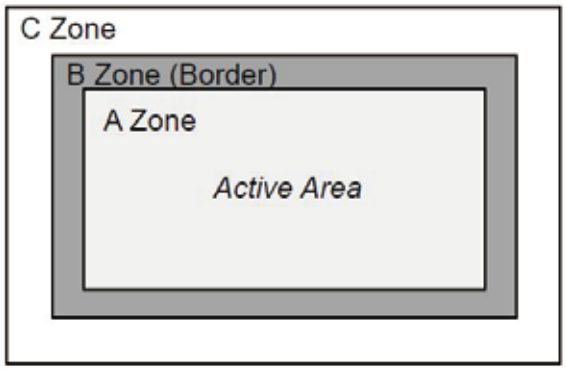
11. Block Diagram



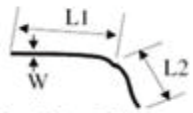
12. Shipment inspection specification

12.1 Zone Definition

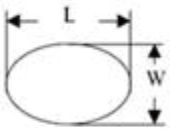
A Zone: Active Area
B Zone: Border Area
C Zone: From B Zone edge to panel edge



12.2 Line/Spot defect size



L = L1 + L2



D = (L + W) / 2

12.3 Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	208.8 (H) x 284.7 (V) x 0.85(D)	**Unit：** ㎜	**Part-A**	Active area	**Part-B**	Border area
Environment	**Temperature**	**Humidity**	**illuminance**	**Distance**	**Time**	**Angle**
	19℃～25℃	50±5%RH	1000~1500Lux	300 ㎜	35Sec	45°
Defect type	**Inspection method**	**Standard**		**Part-A**		**Part-B**
Spot	Electric Display	D≤0.35 ㎜		Ignore		Ignore
		0.35 ㎜＜D≤0.52 ㎜		N≤10		Ignore
		0.52 ㎜＜D≤0.65 ㎜		N≤3		Ignore
		D＞0.65 mm		Not Allow		Ignore
Display malfunction	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜，W≤0.1 ㎜		Ignore		Ignore
		1.0mm＜L≤9.0mm，0.1＜W≤0.2mm, DS>20mm		N≤2		Ignore
		L＞9.0 ㎜，W＞0.2 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.4mm		Ignore		Ignore
		0.4mm≤D≤0.6mm，DS>10mm		N≤4		Ignore
		D＞0.6 mm		Not Allow		Ignore
Corner /Edge chipping	Visual/Film card	It shall not affect the electrode circuit. The edge of the chipped corner shall be ≤ 8mm; The length X ≤ 8mm, the width Y ≤ 1mm. There shall be no cracks, and it shall not be an acute angle. And it shall not affect the electrode circuit. Only one such defect is allowed on each side.				
		 				
TFT warping	T≤5mm 					
Remark	1.Cannot be defect & failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					

	L=long W=wide D=point size N=Defects NO
Mura	Refer to limit samples defined by E-INK

12.4 Barcode

FF

ABBBBBBBBB

CCCDDDEEEE

What is the QR code after picture being scanned and read? It consist of 30 numbers and letters, here is explanation for it.

QR Code: ABBBBBBBBBFFCCCDDDEEEEGHIJKKLL

① A means Factory code, e.g.: H (HINK)
② BBBBBBBBB refers to product model name, which is in consistent with specification part number. E.g.: E0213A189 or E0266A120; when the total code is less than 9, it would be added suffix with **. e.g.: E027A45** or E0154A78*
③ FF means production workshop
④ CCC means date of production
⑤ DDD means production batch
⑥ EEEE means FPL lot
⑦ G means MP/Sample/Trial/Repair
⑧ HIJ:(H——TFT;I——PS;J——EC Glue)
⑨ KK means IC type
⑩ LL means serial number

13. Packing

Full carton: 12 pcs tray with products and 1 pcs empty tray.
Last carton: less 12pcs tray with products and 1 pcs empty tray. The packager will add the right amount of EPE to box so that the added EPE's height approximately close to the EPE height around the inside of the box.