



# P9813

## 一、 INTRODUCTION

P9813 is a full-color LED driver, using CMOS technology and providing 3 constant-current driver as well as 256 grade modulation output. It adopts 2-wire transmission scheme (data and clock), and built-in clock regeneration to enhance the transmission distance. it is suitable for driving the transform of display lighting 、 character and animation. According to different controllers and customers' requirements, It can be operating online or offline.

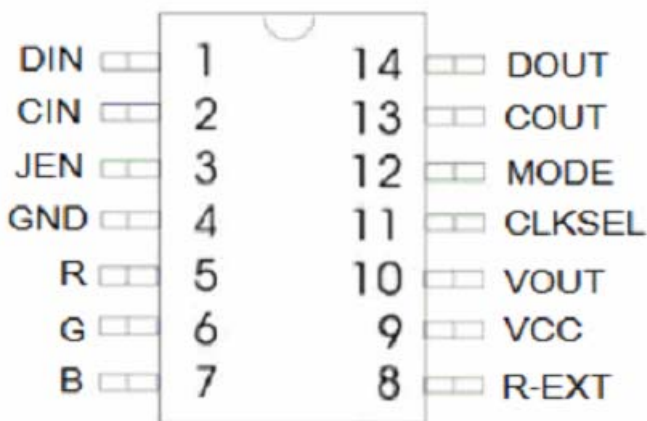
P9813 is excellent in performance, clear in visual effect, visual effect clear, simple cascade; data transmission stability, anti-interference ability and other characteristics.

Provide sop1414(P9813S14)package, DI14(P9813DIP)package, COB packaging mode Die.

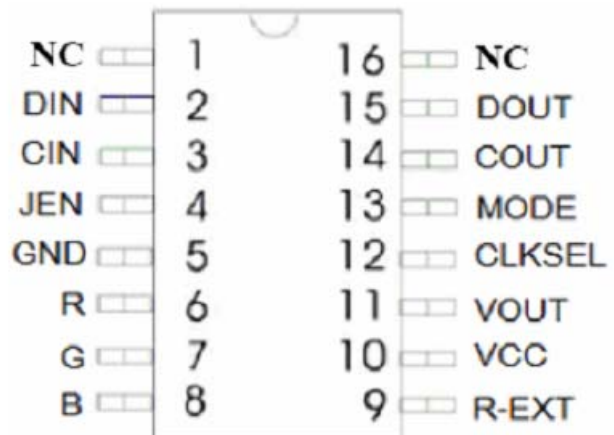
## 二、 Features

- IC input voltage 5V-6.5V; built-in LDO, 4.5V regulator output;
- Single external resistor feedback mode, three-way drive, each drive current 0-45ma;
- Checking function with the input signal;
- Built-in ring oscillator(1.2MHZ) to support ongoing FREE-RUN modulation output, maintaining the screen still function;
- Serial input data the maximum clock frequency 15MHZ;
- PLL data signal regeneration, 1MHZ data transfer speeds of up to 1024 Cascade Point Light;
- LED drive port voltage 17V, can be connected in series 6 LED;

## 三、 Pins map:



P9813-SOP14 package



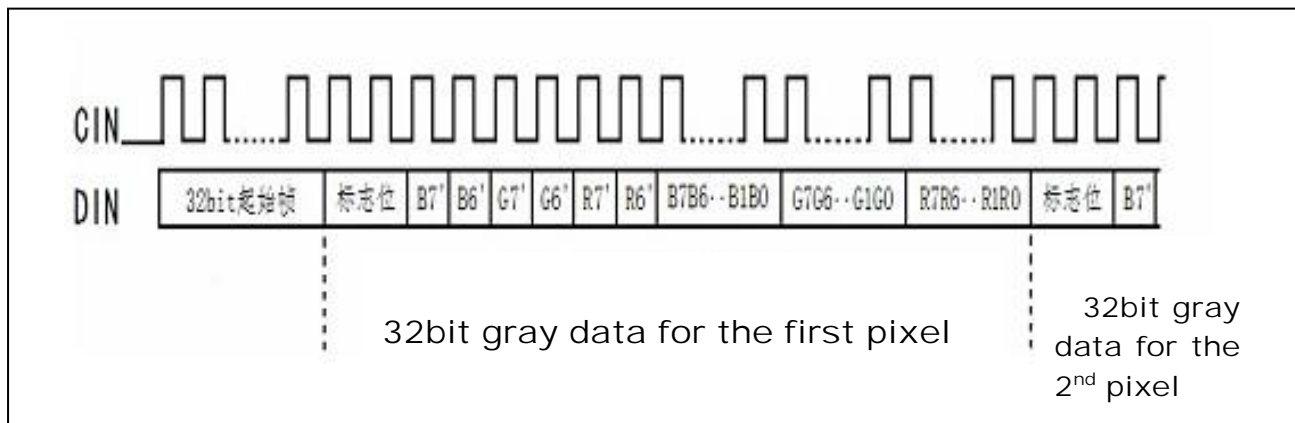
P9816-SSOP16 package



**四、Pin function description(P9813 S14\ DIP14)**

| Pin   | Symbol | Function  |
|-------|--------|---|
| 1     | Din    | Serial data input. Built-in pull. high  |
| 2     | Cin    | Serial clock input, built-in pull. high   |
| 3     | JEN    | JEN=1,timing no parity,JEN=0,timing verification,drive mode,built-in pull-up                |
| 4     | GND    | GDN   |
| 5,6,7 | R,G,B  | RGB output of three=way drive external feedback mode,access resistance                      |
| 8     | R-EXT  | Adjustable output current resistance  |
| 9     | VCC    | Supply voltage,5-6.5V   |
| 10    | VOUT   | Internal operating voltage.VCC>5V time,5V regulator output,while VCC<5V                     |
| 11    | CLKSEL | CLKSEL=1,output clock back,CLKSEL=0,output clk forward                                      |
| 12    | MODE   | MODE=1,output is constant current drive mode,mode=0,output is the plug-in constant pressure |
| 13    | COUT   | Serial clock output.  |
| 14    | DOUT   | Serial Date output.   |

**五、P9813 communication protocol**





1. The ic will latch a bit of data when the rising edge of the clock coming, And the data should changed after the falling edge of the clock;
2. The flag bits is two "1";
3. The verify dta B7'is equal to ~B7,and B6'1S ~B6,B7 and B6 are the gray data of blue
4. the serial data is MSB first ,and the sortorder is blue ,green, red

## 六、 ELECTRICAL PARAMETERS

**Electrical parameters (Ta = 25 °C, Vss = 0 V)**

▲absolution parameters:

| Parameters                 | Symbol | Range  | Units |
|----------------------------|--------|--|-------|
| Supply voltage             | VDD    | 4.5 ~9   | V     |
| LED light voltage          | VLED   | 3-12   | V     |
| Data clock frequency       | FCLK   | 20   | MHZ   |
| Maximum LED output current | Iomax  | 60   | mA    |
| Channel current deviation  | DIO    | Between output channels <3%<br>Between chips <5% | %     |
| Power dissipation          | PD     | <400   | mW    |

|                       |      |           |                          |
|-----------------------|------|-----------|--------------------------|
| Welding temperature   | TM   | 300(8S)   | <input type="checkbox"/> |
| Operating temperature | Topt | -40 ~ +80 | <input type="checkbox"/> |
| Storage temperature   | Tstg | -65 ~+120 | <input type="checkbox"/> |

Note: exceeding the maximum ratings may cause permanent damage to the device

▲Recommend that the working parameters:

| Parameter                 | Symbol | Range        | Unit |
|---------------------------|--------|--------------|------|
| Supply voltage            | VDD    | 4.5-7.5      | V    |
| Regulator output voltage  | VOUT   | 4.5 ±0. 3%   | V    |
| Input voltage             | VIN    | -0.4VOUT+0.4 | V    |
| Data clock frequency      | FCLK   | 0-15         | MHZ  |
| high level width of Clock | TCLKH  | >30          | ns   |
| low level width of Clock  | TCLKL  | >30          | ns   |
| data set-up time          | TSETUP | >10          | ns   |
| Data hold time            | THOLD  | >5           | ns   |
| Dissipation               | PD     | <350         | mW   |
| Operating temperature     | TOP    | -40-+80°C    | °C   |



**▲ timing parameters (T=25°C, VCC=5V)**

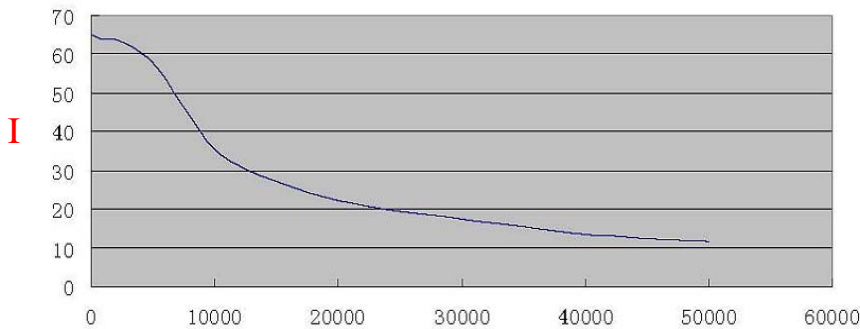
| Parameters                                      | Symbol | Range         |      | Units |
|---|--------|---------------|------|-------|
| Maximum input signal rise time and fall time    | TR     | VCC=5V        | <500 | ns    |
|   | TF     |               | <400 |       |
| Cascading output signal rise time and fall time | TTHH   | CL=30pF,RL=1K | <15  | ns    |
|   | TTHL   |               | <15  |       |
| maximum Cascading output signal delay time      | TPD    | CL=30pF,RL=1K | <12  | ns    |
|   | TCO    |               | <12  |       |
| Minimum turn on time of drive output            | TONMIN | IOUT=20mA     | 200  | ns    |
| Maximum turn on and off time of drive output    | TON    | IOUT=20mA     | <80  | ns    |
|   | TOFF   |               | <80  |       |

**The normal working condition for logic level (Ta = -20 ~ +70℃, Vss = 0 V)**

| Parameters               | Symbol | Min     | Typical | Max    | Units | Test Conditions |
|--------------------------|--------|---------|---------|--------|-------|-----------------|
| Logic supply voltage     | VDD    |         | 5       |        | V     | —               |
| High level input voltage | VIH    | 0.7 VDD | —       | VDD    | V     | —               |
| Low level input voltage  |        |         | —       | 0.3VDD | V     | —               |

**七、 Resistor to adjust the input current**

**As shown,IC connected through a resistor to adjust the external input current**



Current adjust the resistor

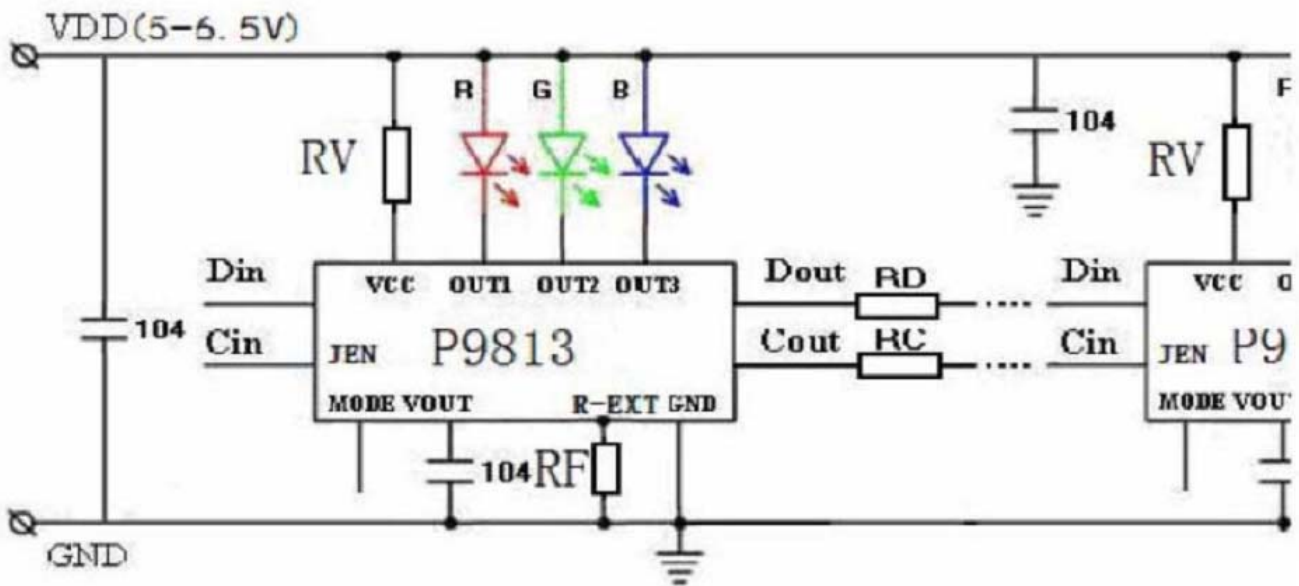


## Typical resistor values:

|                |              |              |               |
|----------------|--------------|--------------|---------------|
| Resistance     | 24K $\Omega$ | 10K $\Omega$ | 6.8K $\Omega$ |
| Output Current | 20mA         | 36mA         | 46mA          |

## 八、 Typical Applications;

### 1.simple circuit (small point source)

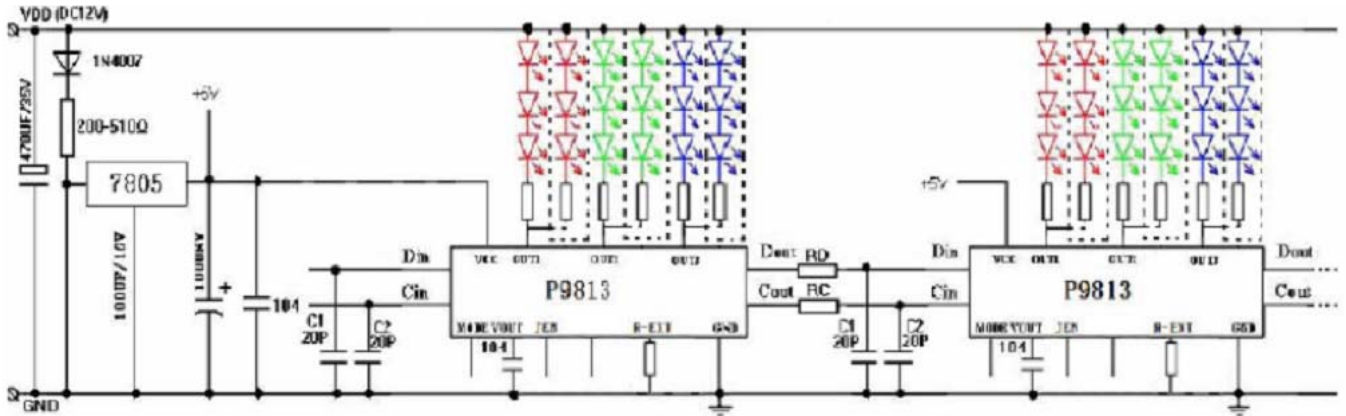


The circuit drive current from the RF resistance adjustment 0-45mA, and CLKSE, MODE ports are vacant, JEN port parity enable, choose according to customer needs

PS: RD, RC, RV resistance were selected to 39 $\Omega$ , 39 $\Omega$ , 3.6 $\Omega$

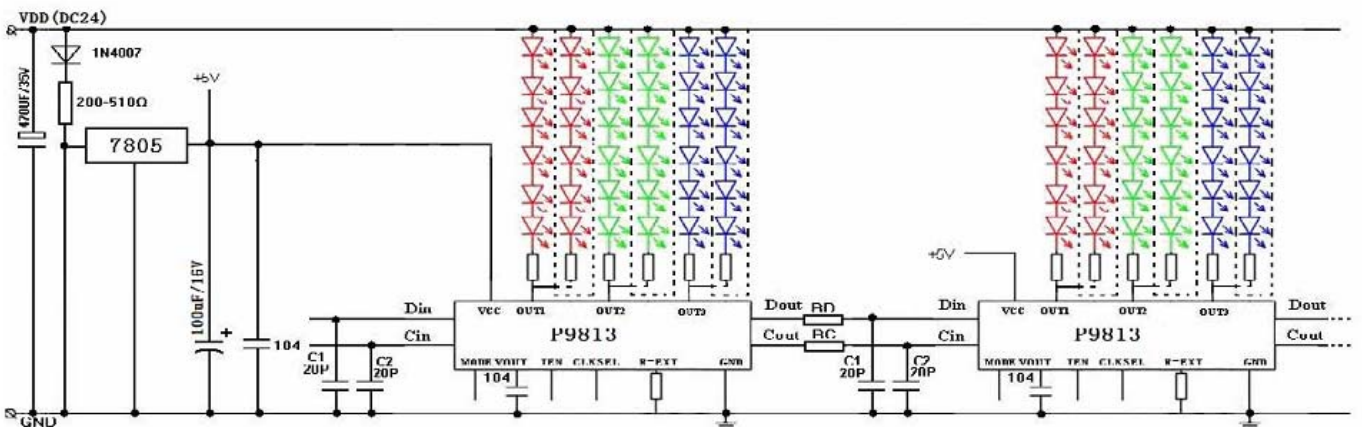


2. P9813 12V applications:



Dotted line part can be omitted, which according to the customer to modify the actual situation. Output current adjustment method according to the “seven, resistance to adjust output current”

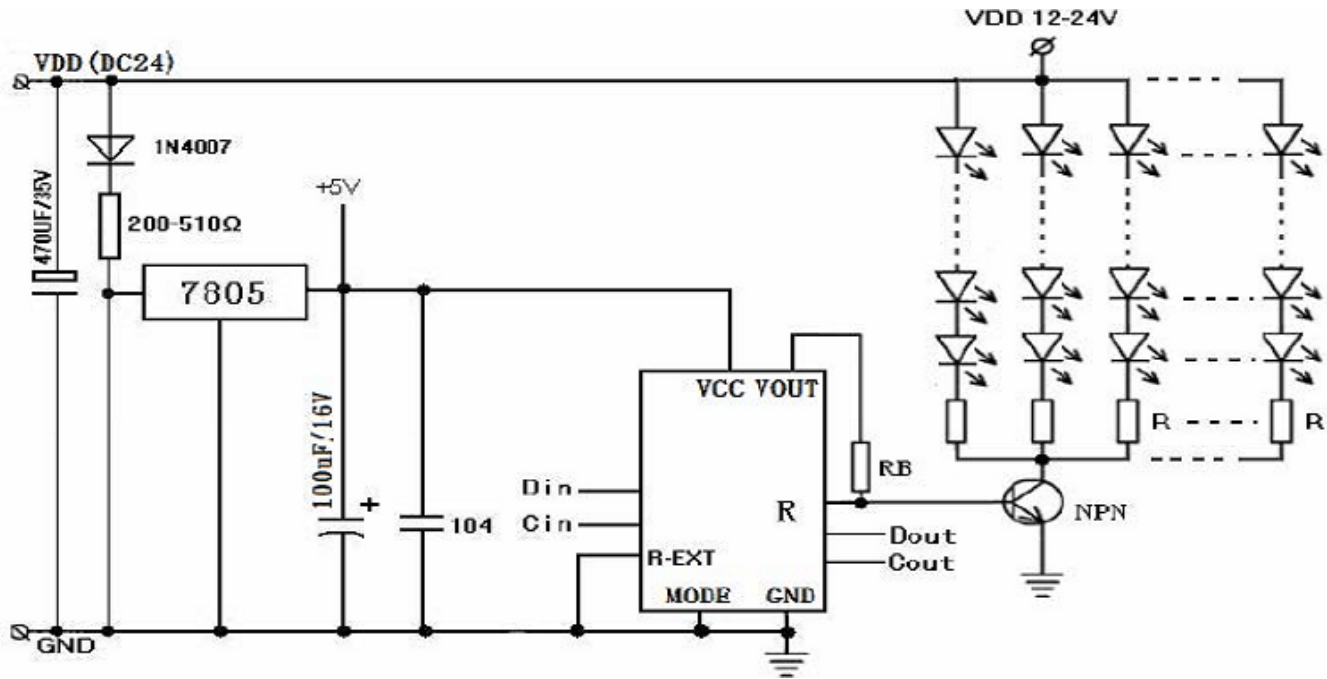
3. P9813 24V applications:



Dotted line part can be omitted, which according to the customer to modify the actual situation. Output current adjustment method according to the “seven, resistance to adjust output current”



5. Plug-in constant voltage drive mode among all the way to the output as an example)



This mode is the case for multi-led, in fact, through the R-side output level control external NPN transistor to drive multiple LED

Limiting resistor calculation- $R=(VDD-V_{LED}-V_{CE})/18mA$

Work in the switch area where the transistor, VCE is the transistor saturation voltage, and generally 0.5V-0.8V. the base resistance RB desirable 2K-5K, in front of other signal connections to the same pattern. VLED single lamp is generally preferable to red light: 1.8V-2V, green; 3V-3.5V, blue light: 3V-3.5V

The model commonly used in multi-channel "first string and the" connection, in view of any one LED in series branch circuit, it will lead to slip all the LED is off, so the use of the connection should follow the following principles; slip LED series number is generally 3 to 6, should be more not less parallel branches.

Jen enable clients to choose according to customer needs.

6. Cascade signal driver capability, and connection method

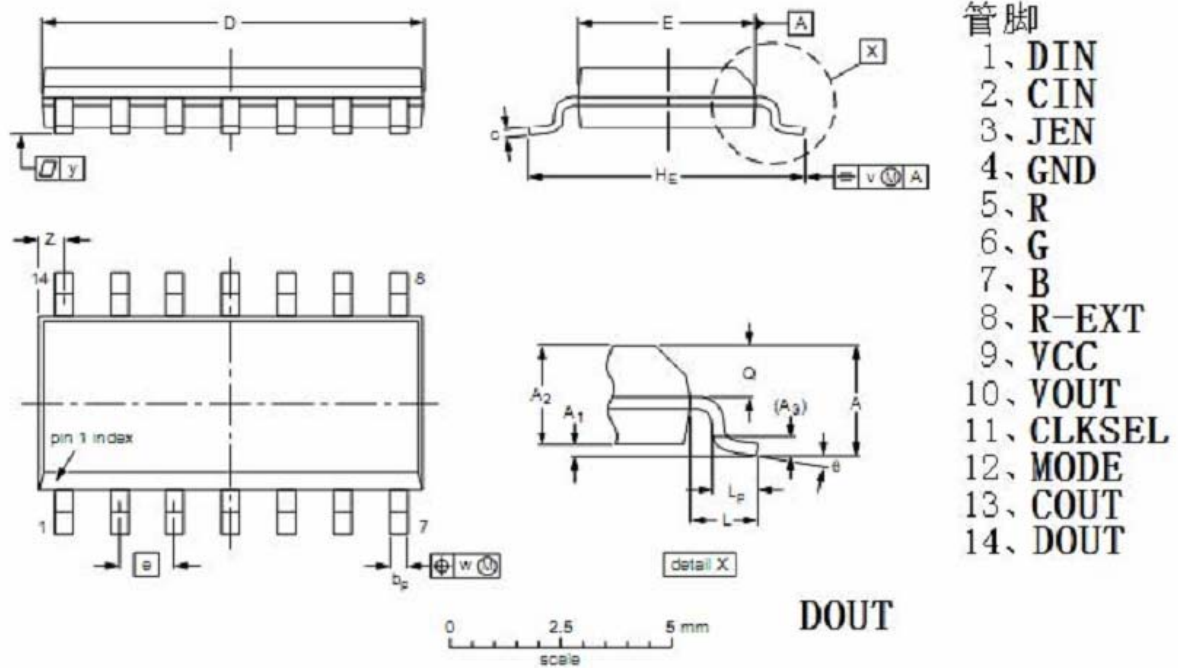
- As chip design push-pull drive circuit, making the cascade signal drive capability have increased significantly. Twisted pair is recommended to increase the transmission distance. To enhance the anti-interference ability in the position near the IC input, the addition of two 20P decoupling capacitors.
- Proposed transmission close at DOUT and COUT mouth and then output to the lower series resistance in order to prevent signal reflection; operating voltage in the 4.5V-12V with resistance to 39Ω resistor, the resistance should be installed close to the IC's output





- Application of small point source (F8 point source), the propose power between the chip VCC pin plus a 3.6Ω resistor (RV), Add a resistor ,VDDin the 5V-5.3V, it can effectively reduce human error led to the VDD and GND short-circuit burned IC
- Recommended operating voltage 24V, DIN and CIN in the mouth of the ESD protection tube connected to protect against high input voltage damage.

## 九: Package size

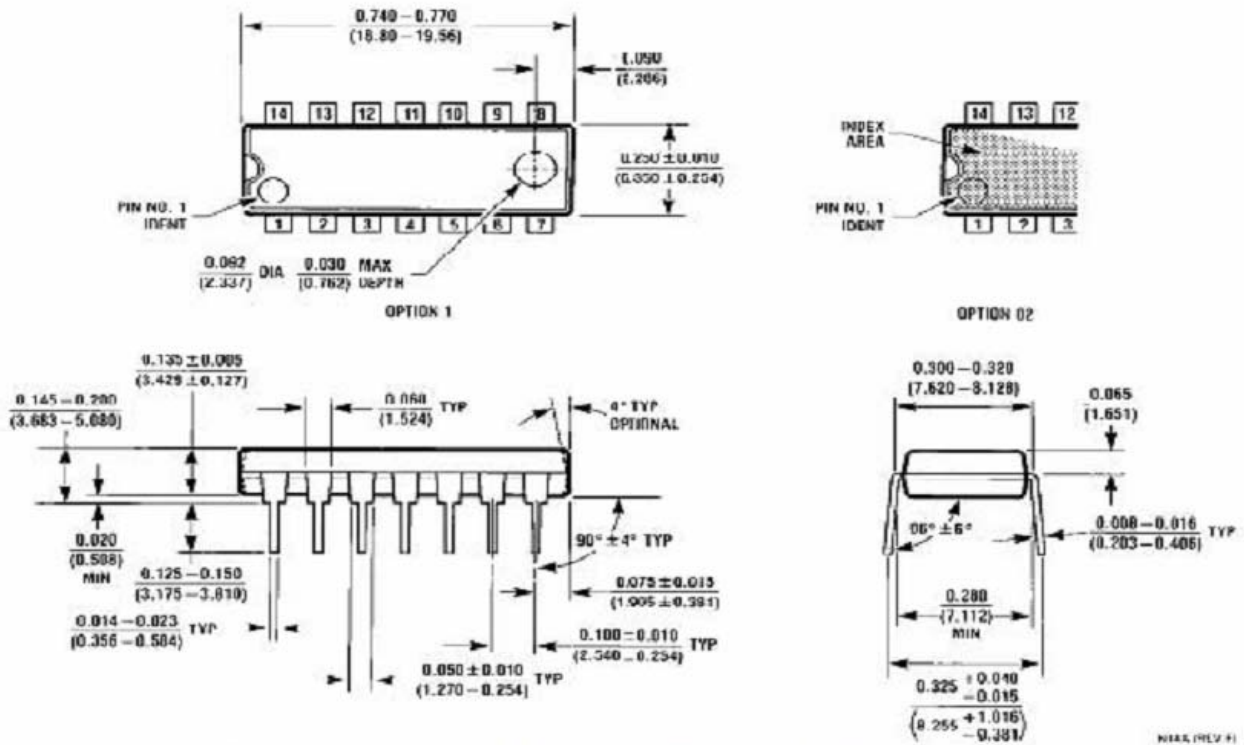


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c               | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|-----------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 1.75   | 0.25<br>0.10   | 1.45<br>1.25   | 0.25           | 0.49<br>0.36   | 0.25<br>0.19    | 8.75<br>8.55     | 4.0<br>3.8       | 1.27 | 6.2<br>5.8     | 1.05  | 1.0<br>0.4     | 0.7<br>0.6     | 0.25 | 0.25 | 0.1   | 0.7<br>0.3       | 8°<br>0° |
| inches | 0.069  | 0.010<br>0.004 | 0.057<br>0.049 | 0.01           | 0.019<br>0.014 | 0.010<br>0.0075 | 0.35<br>0.34     | 0.16<br>0.15     | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012   |          |

P9813 (SOP-14)





14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

P9813 (DIP -14)