TD Release Notes

========== DECEMBER 2018 (r4.3.815) ==========

Updates & fixes:

1. The LVCEPL33/LVDS33 input pad can work correctly now.
2. EF2: Correct the BRAM256K simulation model.
3. Fix a syntax error of BRAM128K/BRAM256K/ROM in IP generator.
4. Add an error message while user specified a non-existed ADC channel.
5. Property fixes: Infer_fsm/opt_timing(placement) can take effect correctly now.
6. HDL parser: support special characters in port names
7. Fix a bug which may cause wrong #TREG number in area report.
8. Fix a routing bug while connecting CE pins of FIFO/BRAM to GND.
9. Consider the extra delay of wires which go across the DSP/BRAM while calculating the wire delay, this fix may induce 1%~2% performance drop in timing report on average.
10. SvfGen: loading device with 'spi write status to enable QE' instruction for ef2 program_spi.

========== DECEMBER 2018 (r4.3.633) ==========

New Features:

1. Support VHDL library analysis.
2. Improve the routability of clock net routing.
3. SvfGen: TDE file could be generated along with merging SVF files now.
4. SvfGen: JTAG loading rate is adjustable for JTAG_STUDIO.

Updates & fixes:

1. Fix a synthesis error if the outputs of RAMFIFO are empty.
2. Fix a package error in EF2 devices.
3. Fix a bit file error while instancing MSLICEs directly in a design.
4. Correct some bit configurations according to drive strength calibration of output pad.
5. Fix a bug that SVF for SRAM may not work under some circumstances.
6. Update the format of output verilog files for simulation.

========== OCTOBER 2018 (r4.3.174) ==========

New Features:

1. Improve Device Chain functions:
   a. Add ***Verify*** function in ***SVF for SPI***.
   b. Add ***Erase SRAM*** function in SVF creator, in order to erase SRAM and clear Done flag.
   c. Add ***Check Status Done*** in SVF creator, in order to check whether the programming is success
   d. Add ***Program Pin to Low*** option in refresh function so that this pin can be set to '0' during refreshing.
   e. Support converting BIN file to SVF file
   f. Support merging SVF files for programming the device chain.
2. Add a new IP ***RAM FIFO*** into IP Generator.
3. Now TD can infer multi-array which is initialized by a loop into DRAM automatically, while the opt_ram option is set to HIGH (default).
4. Chipview can show the location information of package on IO pad now.
5. Improve usability of the encrypt and download tools for EF2 devices
6. New route algorithm to improve routability.
7. New timing-driven router to improve timing while the effort is set to HIGH.

Updates & fixes:

1. Fix bugs in PLL phase shifting, **it may change the value of PLL parameters CLKCi_CPHASE and CLKCi_FPHASE, and the bit/svf file will be affected accordingly.**
2. Fix the PLL output clock missing issue when the output of clkc0 is disabled, **the value of PLL parameter SYNC_ENABLE is changed to DISABLE, which may affect bit/svf file as well**.
3. SVF for SPI updates: increase the wait time of 4K sector erasure to **150,000/1,500,000 TCK (1MHz/10MHz)**, and decrease the wait time of page programming to **5,000/50,000 TCK (1MHz/10MHz)**.
4. Fix the bug that Bitgen property -> persis_bit does not take effect, **change the default value of persit_bit to 1 for EF2**, and solve the compatibility problem for existed projects.
5. Remove Bitgen property -> crc_comp, and the CRC check will be always ON.
6. Update HDL parser for Windows platform to fix a hierarchy tree problem in GUI.
7. Remove a false warning while creating or closing a project.
8. Fix a bug that IP Generator may fail to generate sim.v if the project path contains a space char.
9. IO Constraint tool will not delete the *set_inst_assignment* statements in ADC file anymore.
10. Fix a bug that bank or location may be not assigned automatically in IO Constraint tool.
11. Fix a bug that a wrong LVDS pair location is assigned by IO Constraint tool.
12. The max level of InDelay/OutDelay could take effect correctly now.
13. Fix a bug that changing device or top module name may induce crash.
14. Fix a GCLK routing bug, clock net will not tend to route through common interconnect resources now.
15. Fix a bug of MASK format in SVF file for verifying SPI.
16. Fix the timing bar display issue of Chipwatcher while switching the setup and data table of

GUI.

17. Fix a bug about USB driver conflict in Windows.