seeed studio

XIAO ESP32-S3 Series Datasheet

XIAO ESP32-S3 Series

Microcontroller Development Board

Version: 1.0

Date: 2026/11/03

Status: Controlled Document

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The following safety precautions must be observed during all phases of operation, such as usage, service, or repair of the Seeed Studio XIAO ESP32-S3. As an open-source hardware device with exposed electronic components, special care must be taken regarding electrostatic discharge (ESD), electrical connections, and environmental conditions.

If this board is incorporated into a final product, the system integrator is responsible for ensuring compliance with all applicable safety standards and notifying end-users of relevant safety information by incorporating these guidelines into the product manuals. Seeed Studio assumes no liability for customers' failure to comply with these precautions.

Power Safety	Use a regulated 5 V USB supply. Verify battery polarity before connecting the BAT pads. Use signal levels compatible with 3.3 V logic.
ESD Protection	This product is an ESD-sensitive device without an enclosure. Always wear an ESD wrist strap or touch a grounded metal object before handling the board. Direct contact with pins or RF circuits without protection may cause electrostatic damage to the core components.
Battery & Heat	Battery safety and thermal management. Only use 3.7V Li-ion/Li-Po batteries with built-in protection circuits. The chip temperature may rise during heavy Wi-Fi usage. Avoid prolonged full-load operation in enclosed or high-temperature environments to prevent overheating.
Compliance	Engineering development board, not a final consumer product. Intended for prototyping, testing, and educational use. Integrators are responsible for ensuring the final product complies with all applicable regulations (FCC, CE, RoHS, etc.). Do not use in critical life-support systems.

About the Document

Revision History

VERSION	DATE	AUTHOR	DESCRIPTION
0.1	2026/1/19	Citric, Zeller	Creation of the document
1.0	2026/11/3	Citric	Initial release

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1. Introduction

1.1 Overview

Seeed Studio XIAO ESP32-S3 series leverages 240MHz Xtensa 32-bit LX7 dual-core processor, supporting both WiFi and BLE 5.0 wireless connectivities, a 2.4GHz FPC antenna, allows for deep sleep mode with power consumption as low as **18.39μA for the XIAO ESP32-S3 Standard version** while supporting lithium battery charging management. Ideal for the Internet of Things, Smart Homes, Wireless wearable devices, Robotics, etc.

This series includes the following models:

1. **XIAO ESP32-S3:** Base version with 14 commonly used pins. Available in Pre-Soldered and Un-Soldered SKU configurations. The Pre-Soldered SKU ships with 2.54 mm pin headers and the top-side B2B connector populated. The Un-Soldered SKU ships without factory-soldered pin headers and without the B2B connector.

2. **XIAO ESP32-S3 Sense**: Sensor version featuring an expansion board with an integrated OV5640 camera, digital microphone, and external MicroSD card slot. Offers 16 commonly used pins. Ideal for AI vision and voice applications.

3. **XIAO ESP32-S3 Plus**: An expanded version that adds 9 additional GPIO pads to the base model's 14 commonly used pins. Suitable for customers requiring more pins.

Feature:

- **Powerful MCU Board:** Incorporate the ESP32-S3 32-bit, dual-core, Xtensa processor chip operating up to 240 MHz, mounted multiple development ports, Arduino / MicroPython supported.
- **Advanced Functionality:** Detachable OV5640 camera sensor with a fixed-focus lens for 2592×1944 resolution, integrating an additional digital microphone.
- **Great Memory for more Possibilities:** All versions include 8 MB PSRAM. Standard and Sense have 8 MB Flash; Plus has 16 MB Flash. The Sense expansion board provides a MicroSD slot supporting up to 32 GB SDHC cards with FAT32.
- **Outstanding RF performance:** Support 2.4GHz Wi-Fi and BLE dual wireless communication, achieves a measured line-of-sight range of ≥98 m (Wi-Fi) and ≥110 m (Bluetooth LE) with the supplied antenna (see Table 6-8).
- **Thumb-sized Compact Design:** 21 x 17.8mm, adopting the classic form factor of XIAO, suitable for space-limited projects like wearable devices.

- Pre-trained AI models from SenseCraft AI for no-code deployment.

1.2 Specification

Table 1-1. XIAO ESP32-S3 Series Specifications

Feature	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
Processor	ESP32-S3R8 Xtensa® LX7 dual-core, 32-bit processor, up to 240 MHz		
Wireless	2.4GHz Wi-Fi (802.11 b/g/n) Bluetooth® 5 (LE) & Mesh		
Antenna	External 2.4GHz FPC Antenna (Connected via U.FL; included in retail packages)		
Memory	On-chip 8 MB PSRAM On-board 8 MB Flash		On-chip 8 MB PSRAM On-board 16 MB Flash
Interface	1x UART, 1x I2C, 1x SPI, 11x GPIOs 9x ADC On-board JTAG & USB Pads 1x B2B Connector (Pre-Soldered Ver. Only) 1x Type-C USB	1x UART, 1x I2C, 1x I2S 1x SPI, 13x GPIOs 9x ADC On-board JTAG & USB Pads 1x B2B Connector 1x Type-C USB	2x UART, 1x I2C, 1x I2S, 2x SPI, 20x GPIOs 13x ADC On-board JTAG & USB Pads 1x B2B Connector 1x Type-C USB
Buttons & LEDs	1x Reset button, 1x Boot button 1x User LED (Yellow), 1x Charge LED (Red)		
Camera	-	OV5640	-
Microphone	-	MSM261DGT006	-
Operating Voltage	3.3 V [1]		
Input Voltage Range	5 V (USB) / 3.7 V (Battery)		
Battery Charging	Built-in PMIC		Built-in PMIC
Dimensions	21 x 17.8 x 5.0 mm	21 x 17.8 x 15 mm (with Expansion Board)	21 x 17.8 x 5.0 mm
Weight	~2.17 g ~2.64 g (with antenna)	~4 g ~4.47 g (with antenna)	~2.17 g ~2.64 g (with antenna)
Working Temp.	-20 ℃ ~ +65 ℃		

[1] *Note: The logic level of the ESP32-S3 chip is 3.3V.*

1.3 Performance

Table 1-2. XIAO ESP32-S3 Series Performance Characteristics

Parameters	Conditions	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
Processing Performance				
CPU Frequency	Max	240 MHz		
Wireless Performance				
Wi-Fi TX Power	802.11b	19.97 dBm		
BLE TX Power	Standard EVT, default setting	19.73 dBm		
Camera Performance				
Resolution	Max	-	2592 × 1944	-
Frame Rate	QSXGA (sensor-level)	-	15 fps	-
Microphone Performance				
Sensor Model	-	-	MSM261DGT006	-
SNR	-	-	65 dB	-
Power Consumption (Measured Current)[2]				
Modem-sleep	CPU On, RF Off	35.08 mA	39.62 mA[3]	38.41 mA
Light-sleep	CPU Paused	2.10 mA	2.98 mA[3]	2.26 mA
Deep-sleep	RTC Only	18.39 μA	2.28 mA[3]	19.40 μA

[2] Note: Current was measured at 25℃ with a 3.7 V Li-Po battery supply and no external load. See Table 4-6 for the operating conditions.

[3] Note: The Sense current values were measured using an OV3660-equipped unit with the expansion board attached. Microphone and SD-card communication were disabled for Light-sleep and Deep-sleep. These values are historical reference measurements for the OV3660 configuration.

1.4 Functional Block Diagram

The system architecture of the XIAO ESP32-S3 series is illustrated in Figure 1-1. The diagram highlights the interconnections between the core ESP32-S3 SoC, the power management subsystem, and the distinct expansion capabilities for the Sense and Plus models.

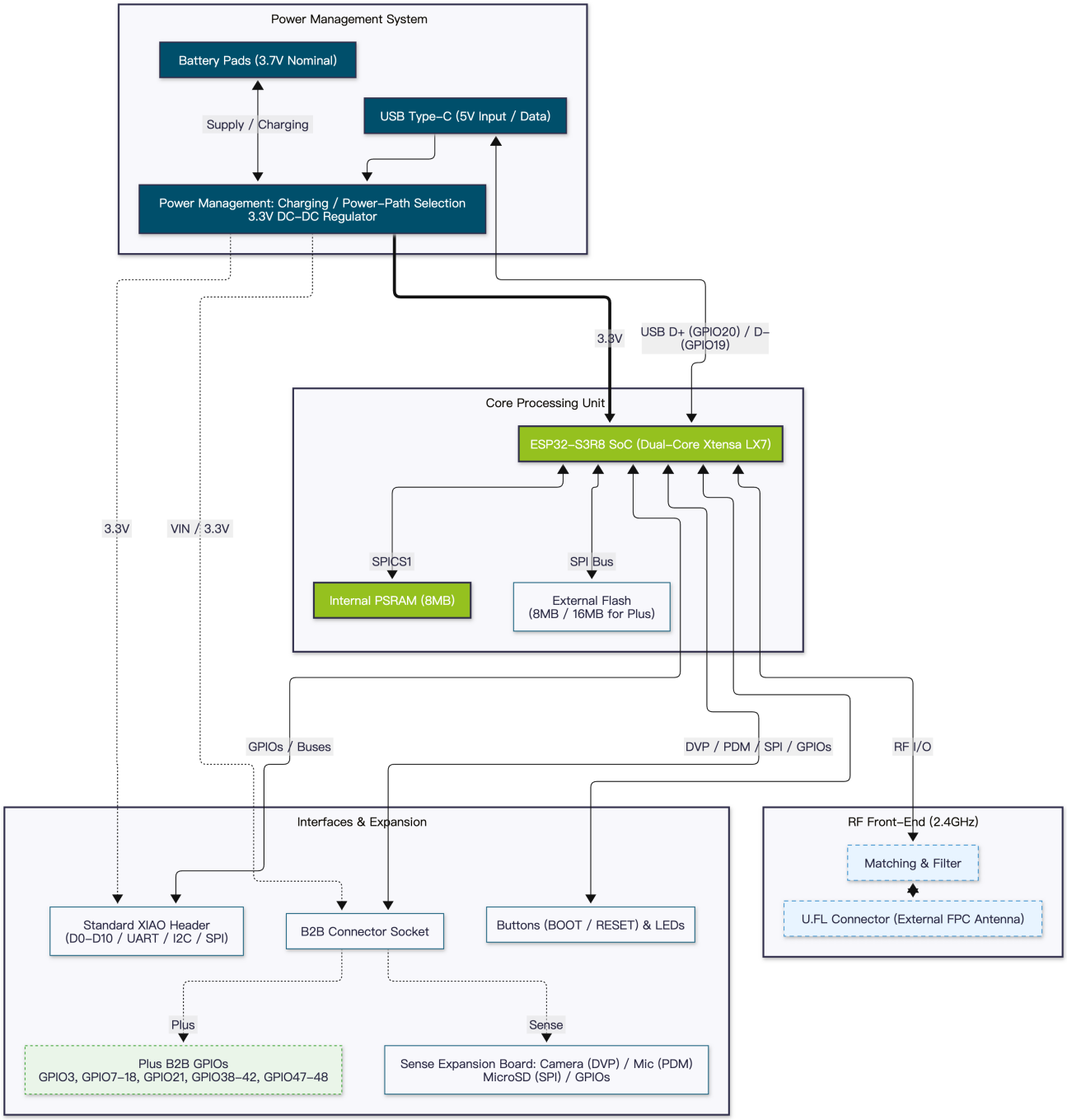


Figure 1-1. Functional Block Diagram of XIAO ESP32-S3 Series

Key Functional Modules:

- Core Processing Unit: Powered by the Espressif ESP32-S3R8 SoC (Dual-Core Xtensa® LX7, up to 240 MHz). The system integrates 8MB of PSRAM for high-performance data processing. The external SPI Flash capacity varies by model configuration (8MB for Standard/Sense, 16MB for Plus).
- Power Management System: The board features a flexible power input architecture supporting both USB Type-C (5V) and Lithium-Ion Battery (3.7V) inputs. The integrated

Power Management Unit (PMU) manages battery charging and regulates the system voltage to a stable 3.3V via a high-efficiency DC-DC regulator.

- B2B Expansion Interface (Dual-Mode): The high-density B2B connector provides specialized functionality depending on the connected peripheral or board variant:
    - For Sense Model: Routes dedicated high-speed DVP signals for camera interface and PDM signals for the digital microphone.
    - For Plus Model: The B2B connector is compatible with the Wio-SX1262 extension board and is not compatible with the plug-in camera sensor board. The nine additional GPIOs (D11–D19) are routed to the staggered edge pads.
- RF Front-End: The 2.4GHz Wi-Fi and Bluetooth LE 5.0 subsystem connects to an external FPC antenna via an on-board U.FL connector, ensuring optimal RF performance and range.

1.5 Application Scenarios

Thanks to its compact thumb-sized form factor, powerful dual-core processing, and rich interface options, the XIAO ESP32-S3 series is an ideal solution for a wide variety of AIoT and wearable applications.

1.5.1 General Applications (All Series)

Applicable to Standard, Sense, and Plus models.

- **Smart Home & Matter Ecosystem**: Miniaturized controllers for smart lights, automated curtains, and environmental sensors compatible with Home Assistant or Matter.
- **Wearable Devices**: Health trackers, smart jewelry, and bio-signal monitors due to the ultra-small footprint (21 x 17.8 mm).
- **IoT Sensor Nodes**: Low-power wireless nodes for monitoring temperature, humidity, and soil moisture in agriculture or industrial settings.
- **Wireless HID Devices**: Custom wireless keyboards, mice, and game controllers leveraging the ESP32-S3's native USB HID and Bluetooth HID capabilities. Compatible with community firmware projects for wireless input devices.
- **STEM Education & Prototyping**: A breadboard-friendly tool for students and makers to learn MicroPython, Arduino, and ESP-IDF.

1.5.2 XIAO ESP32-S3 Sense Specific Applications

Leveraging the on-board Camera, Digital Microphone, and Edge AI capabilities.

- **Edge AI & Machine Vision**: On-device object detection, symbol classification, and

anomaly detection using TinyML frameworks (e.g., Edge Impulse).

- **Voice Interaction**: Offline voice command recognition, wake-word detection, and audio recording for smart speakers.
- **Smart Surveillance**: Low-power video doorbells, baby monitors, and pet cameras with local image processing.
- **Touch-free Interface**: Gesture recognition systems for controlling appliances without physical contact.
- **Face Detection**: Simple face detection and recognition for access control prototypes.

1.5.3 XIAO ESP32-S3 Plus Specific Applications

Leveraging the larger 16MB Flash storage and extended GPIO breakout.

- **High-Capacity Data Loggers**: Long-term recording of sensor data (GPS logs, industrial vibration data) directly to the on-board 16MB Flash without external SD cards.
- **Complex Industrial Controllers**: Scenarios requiring simultaneous connection of multiple peripherals (relays, displays, sensors) utilizing the 9 extra GPIOs.
- **Mesh Network Nodes**: Acting as a robust node in Wi-Fi Mesh networks requiring substantial firmware storage for OTA (Over-the-Air) updates.
- **Portable HMI Displays**: Driving larger SPI/8080 displays with rich graphical user interfaces (GUI) stored in the high-capacity flash.

2 Series Version Description

This chapter describes the versions of the XIAO ESP32-S3 Series.

2.1 Version Overview

The XIAO ESP32-S3 Series is based on the powerful Espressif ESP32-S3 SoC (Dual-core Xtensa® LX7, up to 240 MHz) and offers three distinct hardware variations to meet diverse application requirements.

While all versions share the same thumb-sized footprint (21 × 17.8 mm), underlying hardware architecture, and software development environment, they differ significantly in I/O availability and integrated peripherals. This unified ecosystem ensures that code developed for the standard version can be easily migrated to the Sense or Plus versions with minimal modifications, providing a scalable path from prototype to industrial deployment.

Table 2-1. Available SKU Summary

SKU	Version	Header Configuration	B2B Connector	Package Type	Included Accessories
113991114	XIAO ESP32-S3 Standard	Un-Soldered	Not populated	1 pc retail package	Board, antenna, 7-pin headers ×2
102010573	XIAO ESP32-S3 Standard	Un-Soldered	Not populated	3 pcs retail package	Boards ×3, antennas ×3, 7-pin headers ×6
100092361	XIAO ESP32-S3 Standard	Un-Soldered	Not populated	Tape and reel	Board only
102010634	XIAO ESP32-S3 Standard	Pre-Soldered	Populated	1 pc retail package	Board with soldered headers, antenna
113991115	XIAO ESP32-S3 Sense	Un-Soldered	Populated	1 pc retail package	Board, Sense expansion board, antenna, 7-pin headers ×2, heatsinks ×2
102010635	XIAO	Pre-Soldered	Populated	1 pc retail package	Board with soldered

SKU	Version	Header Configuration	B2B Connector	Package Type	Included Accessories
	ESP32-S3 Sense				headers, Sense expansion board, antenna, heatsinks ×2
102010671	XIAO ESP32-S3 Plus	Un-Soldered	Populated	1 pc retail package	Board, antenna, 7-pin headers ×2
101991469	XIAO ESP32-S3 Plus	Un-Soldered	Populated	Tape and reel	Board only

Pre-Soldered and Un-Soldered describe whether the pin headers are factory-soldered. For Standard, the B2B connector is populated on the Pre-Soldered SKU and is not populated on the Un-Soldered SKUs.

2.2 Hardware Differences

The following table lists the hardware differences between the different versions of the XIAO ESP32-S3 Series.

Table 2-2. Hardware Specification Comparison

Feature	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
Expansion Board	-	Included (B2B Connection)	-
B2B Connector	Pre-Soldered SKU only	Populated	Populated
Camera Interface	-	FPC Connector (24-pin)	-
Supported Sensors	-	OV5640[4] / OV3660 / OV2640 (legacy compatible)	-
Microphone	-	Digital PDM Microphone	-
SD Card Slot	-	MicroSD (SPI Mode)	-
Flash Memory	8 MB	8 MB	16 MB
GPIO Availability	11x (Standard Header)	13x (Standard + Sense)	20x (Standard + Interleaved)

Feature	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
Battery Pads	√	√	√
U.FL Connector	Populated	Populated	Populated
Dimensions	21 × 17.8 × 5.0 mm	21 × 17.8 × 15 mm[5]	21 × 17.8 × 5.0 mm

[4] *Note: A fixed-focus OV5640 camera is supplied with all current XIAO ESP32-S3 Sense kits. The transition began in October 2026 following the discontinuation of the previous OV2640 and OV3660 camera modules. OV2640 and OV3660 are retained as legacy camera references.*

[5] *Note: Thickness includes the main board and the expansion board connected.*

2.3 Sense Expansion Board Description

The following describes the B2B expansion board for the XIAO ESP32-S3 Sense, divided into three modules: the Camera Module, the Microphone Module, and the MicroSD Card Interface Module.

2.3.1 Camera Module

The Sense expansion board connects the camera through an 8-bit DVP interface. The ESP32-S3 supplies the camera master clock, while the sensor provides PCLK, VSYNC, HREF, and the image data bus. Pin assignments are listed in Table 2-4.

The Sense kit is supplied with a fixed-focus OV5640 camera through the 8-bit DVP interface. The separately sold OV5640 camera (SKU 114993115) uses an autofocus lens and has different optical and mechanical specifications. OV2640 and OV3660 remain supported as legacy camera options.

2.3.1.1 Sensor Specifications

Table 2-3. Supported Camera Sensor Specifications

Parameter	OV2640 (Legacy)	OV3660 (Legacy)	OV5640 (Retail)	OV5640 (Sense Standard)
Max Resolution	2 MP	3.1 MP	5 MP	5 MP
Active Array Size	1600 × 1200	2048 × 1536	2592 × 1944	2592 × 1944
Lens Size	1/4"	1/5"	1/4"	1/4"

Parameter	OV2640 (Legacy)	OV3660 (Legacy)	OV5640 (Retail)	OV5640 (Sense Standard)
Focal length	3.29 mm	4.2 mm	3.29 mm	-
Aperture	-	-	Approx. F2.8	F2.2
Focus Type	Fixed Focus (FF)	Fixed Focus (FF)	Autofocus (AF)	Fixed Focus (FF)
Focus range	0.3 m ~ ∞	0.2 m ~ ∞	1m to infinity (specified focusing distance)	Minimum shooting distance: 20cm
Pixel Size	2.2 µm x 2.2 µm	1.4 µm x 1.4 µm	1.4 µm x 1.4 µm	1.4µm×1.4µm
Sensitivity	0.6 V/Lux-sec		-	-
White Balance	Auto			
Gain	Auto			
Exposure Control	Auto			
Dynamic Range/SNR	50 dB / 40 dB	70 dB / 34 dB	68 dB / 36 dB	68dB / 36dB (sensor-level)
Maximum Image Transfer Rate[6]	15 fps @ UXGA/SXGA 30 fps @ SVGA 60 fps @ CIF	15 fps @ UXGA 30 fps @ SXGA	15 fps @ QSXGA 30 fps @ 1080p 45 fps @ 1280 x 960 60 fps @ 720p	15fps @ QSXGA 30fps @ 1080p 45fps @ 1280×960 60fps @ 720p
Output Formats	YUV(422/420)/YCbCr422/ RGB565/555 8-bit compressed data 8/10-bit Raw RGB data	YUV/YCbCr 4:2:2; RGB565/555/444; RAW RGB	8/10-bit RGB RAW output	RAW RGB; RGB565/555/444; YUV422/420; YCbCr422; JPEG
Field of View (FOV)	69° (Stock Lens)	102° (Stock Lens)	69° (Stock Lens)	68°
Sensor Power Consumption	Active: 140 mW (UXGA YUV mode) Standby: 600 µA	Active: 90 mW Standby: 20 µA	Active: 140 mW Standby: 20 µA	-
Dimensions	8.5 x 8.5 x 5.5 mm	8 x 8 x 4.5 mm	8.5 x 8.5 x 5.5 mm	8 x 8 x 4.5 mm

Parameter	OV2640 (Legacy)	OV3660 (Legacy)	OV5640 (Retail)	OV5640 (Sense Standard)
Work Temp.	-20℃ ~ 70℃			

[6] *Note: Frame rates are theoretical maximums from the sensor datasheet. Actual performance depends on ESP32-S3 clock speed, resolution settings, and JPEG compression quality.*

The standard Sense OV5640 camera uses a fixed-focus F2.2 lens with a 68° field of view and a specified minimum shooting distance of 20cm. The separately sold OV5640 camera (SKU 114993115) uses a different autofocus lens assembly. Sense board-level current measurements in this datasheet were obtained using an OV3660-equipped unit; measurements for the current OV5640-equipped Sense are not yet available.

2.3.1.2 Pin Assignment

The pin mapping for the DVP interface is consistent across all supported sensors.

Table 2-4. Camera Interface Pin Assignment

Camera Signal	XIAO GPIO	Function Description
MCLK	GPIO 10	Master Clock
PCLK	GPIO 13	Pixel Clock
VSYNC	GPIO 38	Vertical Sync
HREF	GPIO 47	Horizontal Reference
SDA	GPIO 40	SCCB Data (I2C)
SCL	GPIO 39	SCCB Clock (I2C)
DVP_Y2	GPIO 15	Data Bit 2
DVP_Y3	GPIO 17	Data Bit 3
DVP_Y4	GPIO 18	Data Bit 4
DVP_Y5	GPIO 16	Data Bit 5
DVP_Y6	GPIO 14	Data Bit 6
DVP_Y7	GPIO 12	Data Bit 7
DVP_Y8	GPIO 11	Data Bit 8
DVP_Y9	GPIO 48	Data Bit 9

2.3.2 Microphone Module

The following table presents parameters of the Microphone Module.

Table 2-5. Microphone Module Parameters

Parameters	Specification
Sensor Model	MSM261DGT006
Type	Digital PDM Output
Signal-to-Noise Ratio (SNR)	65 dB
Pin Assignment	PDM_CLK - GPIO42 PDM_DATA - GPIO41

2.3.3 MicroSD Card Interface Module

The expansion board provides a MicroSD card slot using SPI mode. The card shares SCK, MISO, and MOSI with D8, D9, and D10, and uses a separate chip-select signal. The interface supports the FAT32 file system and the SPI-mode SD-card drivers in Arduino and ESP-IDF.

Table 2-6. SD Card Interface Module Parameters

Parameters	Specification
Interface Type	MicroSD Card Interface
Interface Protocol	SPI
File System Support	FAT32
Capacity Support	Up to 32 GB (SDHC)
Pin Assignment	SCK - D8 (GPIO7) MOSI - D10 (GPIO9) MISO - D9 (GPIO8) CS - GPIO21 / USER_LED by default

2.4 Software Compatibility

All XIAO ESP32-S3 series versions share the same software development environment and base firmware, with the primary difference being driver support for specific peripherals.

Code that uses D0–D10, the default buses, and native GPIO numbers is portable across all

versions, with the following considerations:

1. Examples for the camera and microphone supplied with the Sense expansion board use the Sense peripheral pin assignments. External peripherals on other versions require the corresponding wiring and driver configuration.
2. Flash memory capacity differences may affect firmware size limitations.

Table 2-7. Supported Development Platforms for the XIAO ESP32-S3 Series

Development Environment	*XIAO ESP32-S3*	*XIAO ESP32-S3 Sense*	*XIAO ESP32-S3 Plus*
Arduino IDE	✓	✓	✓
PlatformIO	✓	✓	✓
ESP-IDF	✓	✓	✓
MicroPython	✓	✓	✓
CircuitPython	✓	✓	✓
Rust	✓	✓	✓
MicroBlocks	✓	✓	✓
Zephyr	✓	✓	✓
NuttX RTOS	✓	✓	✓
FreeRTOS	✓	✓	✓
TASMOTA	✓	✓	✓
ESPHome	✓	✓	✓

Platform compatibility depends on the board target, firmware release, Flash configuration, and peripheral drivers. Select the target that matches the board version and verify the camera, microphone, and storage drivers required by the application.

2.5 Version Selection Guide

The XIAO ESP32-S3 series offers tailored solutions for various development stages:

1. **XIAO ESP32-S3 (Standard):** Features a compact layout with 11 multiplexed GPIOs (I2C/SPI/UART). It is the most cost-effective choice for standard IoT nodes, beginner projects, and space-constrained installations requiring basic wireless connectivity. Note:

The on-board B2B connector is **only available on the Pre-Soldered version**. The Un-Soldered version does not include this connector.

2. **XIAO ESP32-S3 Sense:** Comprises the standard main board plus a specialized expansion shield. This version integrates a camera sensor, digital microphone, and SD card slot. It is purpose-built for Edge AI applications such as computer vision (TinyML) and voice recognition assistants.
3. **XIAO ESP32-S3 Plus:** Designed for advanced industrial and high-I/O applications. Unlike the Sense version, the Plus model does not ship with an expansion board. However, it retains the B2B connector and features an additional high-density staggered pad layout to break out 9 extra GPIOs (D11-D19) between the standard headers. Coupled with an upgraded 16 MB Flash, this version is capable of hosting large file systems, complex GUIs (LVGL), or OTA partitions, making it the robust choice for professional product integration.

Table 2-8. Recommended Application Scenarios

Application Scenario	Recommended Version	Key Advantage
Cost-Sensitive IoT Nodes	XIAO ESP32-S3	Minimum footprint & lowest cost
Edge AI (Vision/Voice)	XIAO ESP32-S3 Sense	Integrated Camera & Mic
Audio Recording	XIAO ESP32-S3 Sense	On-board PDM Mic & SD Slot
Complex Industrial Control	XIAO ESP32-S3 Plus	Full GPIO Breakout
Large Data Logging	XIAO ESP32-S3 Plus	16 MB Flash Storage

3. Pins

This chapter details the physical pin distribution, hardware interfaces, and logical pin definitions of the XIAO ESP32-S3 series. Thanks to the powerful GPIO matrix and IO MUX of the ESP32-S3 SoC, most digital peripheral signals (such as I2C, SPI, UART, and I2S) can be flexibly routed to any available GPIO pin. The default mappings shown in this chapter correspond to the standard Arduino Board Support Package (BSP) definitions.

3.1 Pinout Diagram

The following pinout diagrams illustrate the physical locations and default multiplexed functions of the edge castellations (standard headers) and high-density surface-mount pads across different versions.

3.1.1 XIAO ESP32-S3

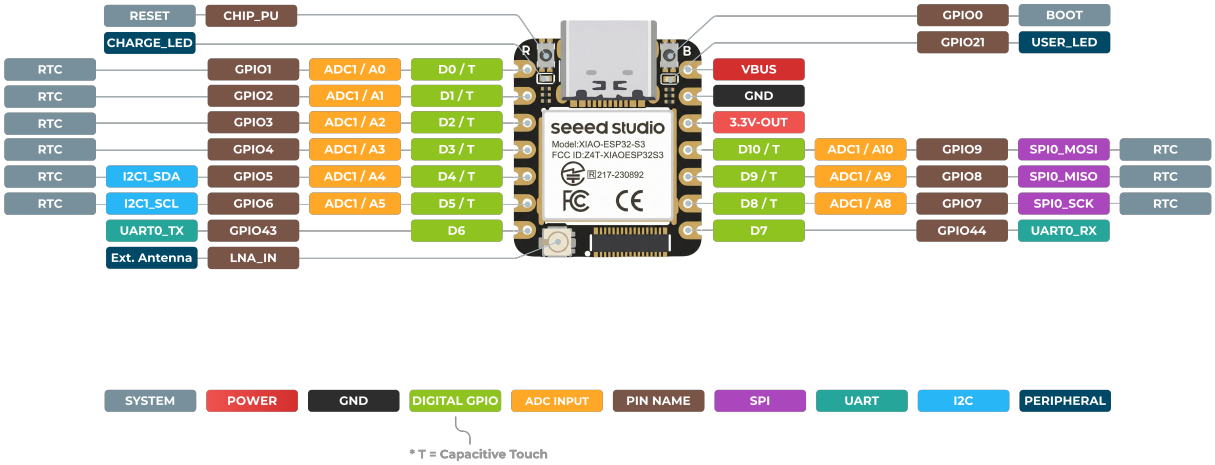


Figure 3-1. XIAO ESP32-S3 Front Pinout Diagram

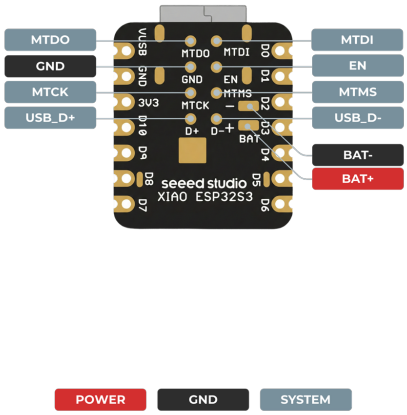


Figure 3-2. XIAO ESP32-S3 Back Pinout Diagram

3.1.2 XIAO ESP32-S3 Sense

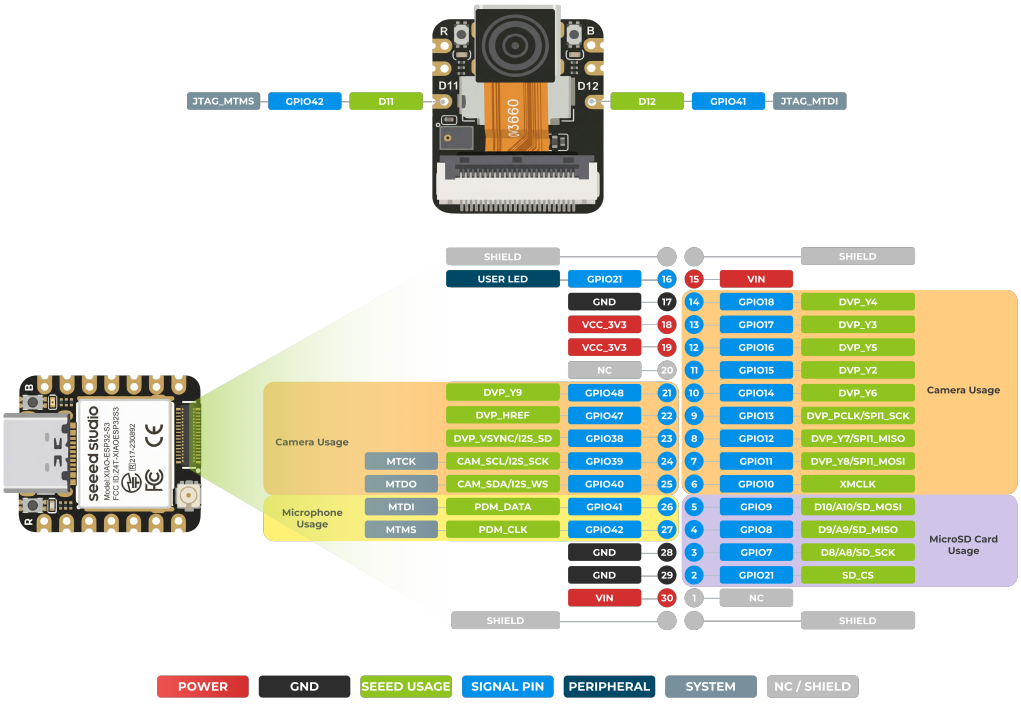


Figure 3-3. XIAO ESP32-S3 Sense Front Pinout (OV3660 Reference Assembly)

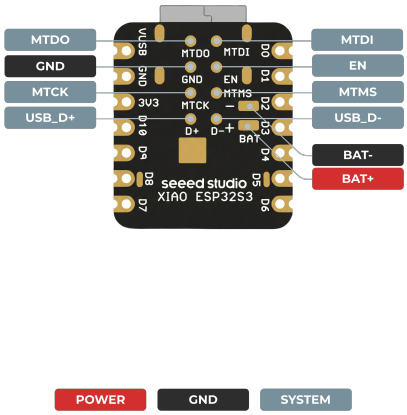


Figure 3-4. XIAO ESP32-S3 Sense Back Pinout Diagram

3.1.3 XIAO ESP32-S3 Plus

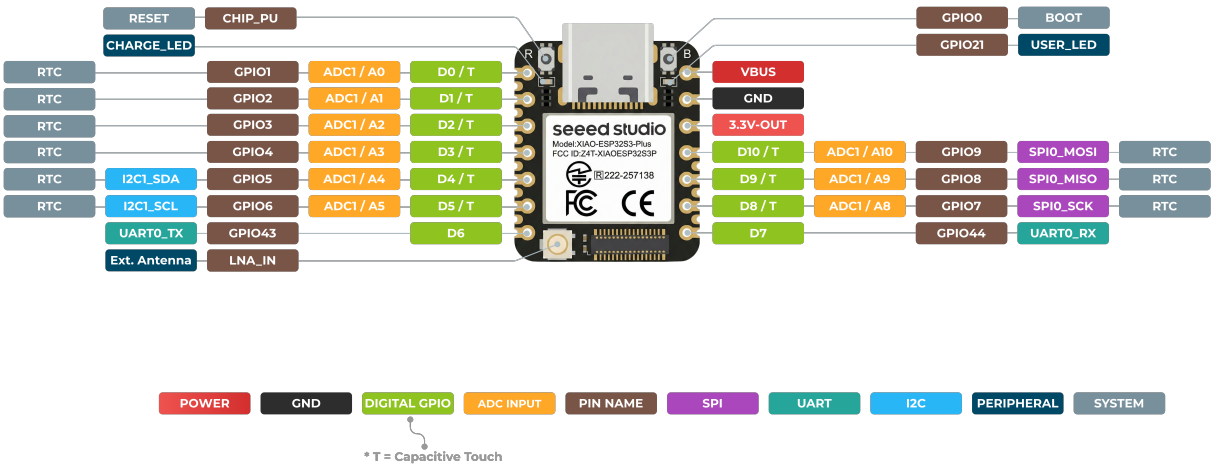


Figure 3-5. XIAO ESP32-S3 Plus Front Pinout Diagram

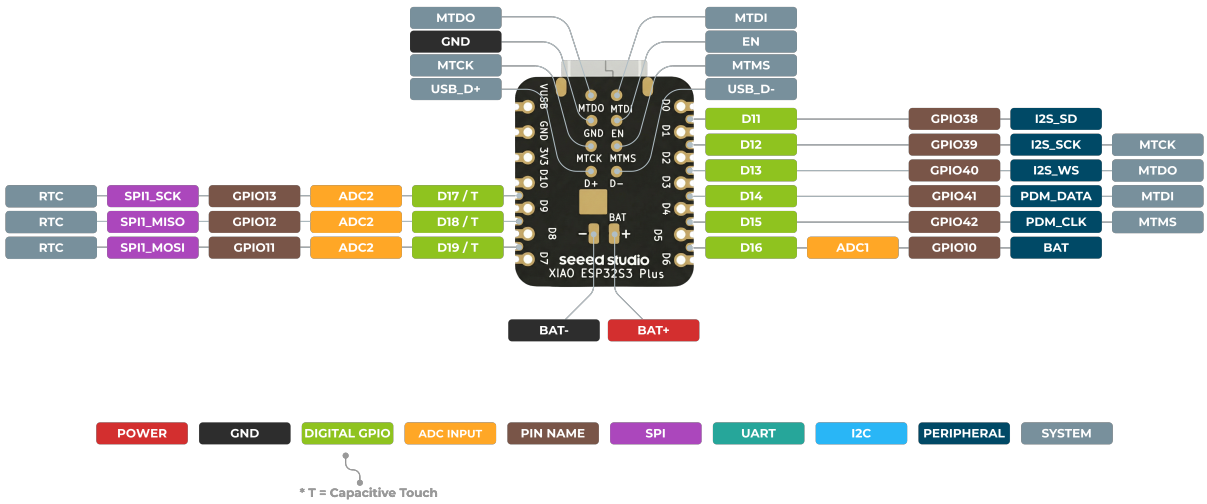


Figure 3-6. XIAO ESP32-S3 Plus Back Pinout Diagram

3.2 Pin Parameter Definitions

The XIAO ESP32-S3 series offers a versatile range of I/O signals via the ESP32-S3's GPIO matrix. The table below categorizes the signal types and their corresponding functional definitions used throughout this document.

Table 3-1. Pin Parameter Definitions

Parameter	Pin Type	Function Description
VBUS	Power I/O	5V Power Input / Output. Outputs 5V when the board is powered via USB. Alternatively, it can be used as a 5V power input to supply the board when USB is disconnected.
GND	Ground	System ground reference.
3.3V-OUT	Power Output	3.3V regulated power output from the on-board DC-DC converter.
Dx	Digital GPIO	Standard Arduino-style digital pin numbering. Supports bidirectional digital input and output.
Ax / ADCx	Analog Input	Analog input channel routing to the internal Analog-to-Digital Converter (ADC1 / ADC2) for voltage measurement.

Parameter	Pin Type	Function Description
GPIOx	Native GPIO	Native ESP32-S3 hardware GPIO numbering. Directly corresponds to the Espressif chip datasheet.
T	Touch Pin	Supports capacitive touch sensing functionality.
I2S_SD / I2S_SCK / I2S_WS	I2S Interface	Inter-IC Sound (I2S) synchronous serial protocol lines for digital audio data transmission.
I2Cx_SDA / I2Cx_SCL	I2C Interface	Inter-Integrated Circuit (I2C) data and clock lines for synchronous serial communication.
SPIx_MOSI / SPIx_MISO / SPIx_SCK	SPI Interface	Serial Peripheral Interface (SPI) bus for high-speed synchronous serial communication.
UARTx_TX / UARTx_RX	UART Interface	Universal Asynchronous Receiver-Transmitter data lines for serial communication.
MTCK / MTDO / MTDI / MTMS	JTAG Interface	Standard JTAG interface pins for hardware-level firmware debugging and programming.
USB_Dx	USB Interface	Native USB 2.0 OTG data lines.
EN	Control Input	Hardware Reset pin (Active Low). Pulling this pin to GND triggers a system reset of the microcontroller.

3.3 Detailed Pin Description

The following table outlines the general pin definitions for the XIAO ESP32-S3 core board. This includes pins exposed on the standard edge headers, as well as internal test pads and peripheral connectors. The listed multiplexing options (MUX) represent the default configurations within the standard Board Support Package (BSP).

Table 3-2. XIAO ESP32-S3 Standard Edition Pin Definitions

XIAO Pin	SoC Pin	IO MUX Function			I/O Type	Other Name For XIAO
VBUS	-	-	-	-	POWER	-
3V3	-	-	-	-	POWER	-
GND	GND	-	-	-	POWER	-
D0	GPIO1	ADC1_CH0	TOUCH1	-	I/O/T	A0 / RTC
D1	GPIO2	ADC1_CH1	TOUCH2	-	I/O/T	A1 / RTC
D2	GPIO3	ADC1_CH2	TOUCH3	-	I/O/T	A2 / RTC / Strapping

XIAO Pin	SoC Pin	IO MUX Function			I/O Type	Other Name For XIAO
						(JTAG source)
D3	GPIO4	ADC1_CH3	TOUCH4	-	I/O/T	A3 / RTC
D4	GPIO5	ADC1_CH4	TOUCH5	SDA	I/O/T	A4 / RTC
D5	GPIO6	ADC1_CH5	TOUCH6	SCL	I/O/T	A5 / RTC
D6	GPIO43	U0TXD	-	-	I/O	-
D7	GPIO44	U0RXD	-	-	I/O	-
D8	GPIO7	ADC1_CH6	TOUCH7	SCK	I/O/T	A8 / RTC
D9	GPIO8	ADC1_CH7	TOUCH8	MISO	I/O/T	A9 / RTC
D10	GPIO9	ADC1_CH8	TOUCH9	MOSI	I/O/T	A10 / RTC
BOOT	GPIO0	-	-	-	I/O	-
RESET	-	-	-	-	-	-
MTDI	GPIO41	MTDI	-	-	I/O	-
MTDO	GPIO40	MTDO	-	-	I/O	-
MTCK	GPIO39	MTCK	-	-	I/O	-
MTMS	GPIO42	MTMS	-	-	I/O	-
D+	GPIO20	USB_D+	-	-	I/O	-
D-	GPIO19	USB_D-	-	-	I/O	-
BAT+	-	-	-	-	POWER	-
BAT-	-	-	-	-	POWER	-
EN	-	-	-	-	-	-
USER LED	GPIO21	-	-	-	I/O	LED_BUILTIN

3.4 Version-Specific Pin Assignments

The XIAO ESP32-S3 series includes specialized versions (Sense and Plus) that extend the core capabilities through distinct hardware designs. Rather than relying on a single expansion method, these versions utilize different physical interfaces to access the ESP32-S3's remaining

GPIOs:

- **Sense Version**: Utilizes the top-mounted Board-to-Board (B2B) connector to interface with a dedicated expansion board.
- **Plus Version**: Achieves I/O expansion directly on the main PCB without requiring an expansion board. It employs a high-density staggered pad layout-inserting additional contact pads directly between the standard headers-to break out the extra GPIOs.

This section details the specific resource allocation and pin mapping for both the onboard peripherals and the extended I/O interfaces found on these versions.

3.4.1 Sense Expansion Board Peripherals

The Sense Expansion Board integrates a camera module, a digital PDM microphone, a MicroSD card slot, and two additional expansion GPIO pads. These peripherals are hardwired to specific GPIO interfaces of the ESP32-S3 via the B2B connector. The table below summarizes the dedicated pin assignments for all built-in peripherals on the Sense board.

Table 3-3. XIAO ESP32-S3 Sense B2B connector Pin Definitions

Peripheral	Signal Name	ESP32-S3 GPIO	I/O	Function Description
Camera	XMCLK	GPIO10	O	Master Clock output to camera.
	CAM_SDA	GPIO40	I/O	SCCB (I2C) Data line.
	CAM_SCL	GPIO39	O	SCCB (I2C) Clock line.
	DVP_PCLK	GPIO13	I	Pixel synchronization clock input.
	DVP_VSYNC	GPIO38	I	Vertical synchronization signal (Frame Sync).
	DVP_HREF	GPIO47	I	Horizontal reference signal (Line Sync).
	DVP_Y[9:2]	GPIO48, 11, 12, 14, 16, 18, 17, 15	I	8-bit Parallel Video Data Bus.
Microphone	PDM_CLK	GPIO42	O	Clock output to PDM Microphone.
	PDM_DATA	GPIO41	I	PDM bitstream input from Microphone.
MicroSD Slot	CS	GPIO21	O	SPI Chip Select (Active Low).
	SCK	GPIO7	O	SPI Serial Clock.
	MOSI	GPIO9	O	SPI Master Out Slave In.

Peripheral	Signal Name	ESP32-S3 GPIO	I/O	Function Description
	MISO	GPIO8	I	SPI Master In Slave Out.
	J3 Pad[7]	-	-	Connects MicroSD pull-up resistors (Hardware Config).
Expansion	J2 Pad[8] / D12	GPIO41	I/O	Extra digital I/O. Shared with PDM_DATA. Cut JP2 to isolate the microphone.
	J1 Pad[8] / D11	GPIO42	I/O	Extra digital I/O. Shared with PDM_CLK. Cut JP1 to isolate the microphone.

[7] Note: The MicroSD card slot utilizes the standard SPI bus pins (D8/SCK, D9/MISO, D10/MOSI), allowing users to connect additional SPI peripherals to the same bus.

By default, the MicroSD card Chip Select (CS) signal is routed to GPIO21 / USER_LED through R12. Advanced users can remap SD_CS to D2 / GPIO3 by changing the 0Ω resistor configuration.

[8] Note: The expansion pads J1 (D11) and J2 (D12) share the same GPIO lines (GPIO42 and GPIO41) with the onboard PDM microphone. If you intend to use J1 and J2 for external digital peripherals, it is highly recommended to cut the JP1 and JP2 solder jumpers. This isolates the microphone circuit and prevents signal interference.

3.4.2 Plus Version Extended I/O

The Plus version enhances the I/O capabilities by utilizing a high-density staggered pad layout to break out 9 extra GPIOs (D11-D19) between the standard headers. This brings the total number of usable GPIOs to 20, making it ideal for complex user applications. The table below describes the default hardware functions and BSP mappings of these extended pins.

Table 3-4. XIAO ESP32-S3 Plus Extended Pinout

XIAO Pin	SoC Pin	IO MUX Function	I/O Type	Example Function	Notes (Important)
D11	GPIO38	GPIO	I/O	I2S_SD	On the Sense version, D11 is mapped to GPIO42 - NOT the same GPIO.
D12	GPIO39	MTCK	I/O	I2S_SCK	Shares GPIO39 with external JTAG MTCK. USB Serial/JTAG remains an alternative. Sense D12 maps to GPIO41.
D13	GPIO40	MTDO	I/O	I2S_WS	Shares GPIO40 with external JTAG MTDO. USB Serial/JTAG remains an alternative.

XIAO Pin	SoC Pin	IO MUX Function	I/O Type	Example Function	Notes (Important)
D14	GPIO41	MTDI	I/O	UART1_RX	Shares GPIO41 with external JTAG MTDI and Sense PDM_DATA (Sense D12).
D15	GPIO42	MTMS	I/O	UART1_TX	Shares GPIO42 with external JTAG MTMS and Sense PDM_CLK (Sense D11).
D16	GPIO10	FSPICS0 / ADC1_CH9	I/O/T	ADC	RTC GPIO (Supports Deep Sleep Wakeup)
D17	GPIO13	FSPIQ / ADC2_CH2	I/O/T	SPI1_SCK	RTC GPIO
D18	GPIO12	FSPICLK / ADC2_CH1	I/O/T	SPI1_MISO	RTC GPIO
D19	GPIO11	FSPID / ADC2_CH0	I/O/T	SPI1_MOSI	RTC GPIO

3.4.3 Pin Name Mapping Varies Between Versions

The extended pin names D11 through D15 do not map to the same physical GPIOs across different board versions.

Table 3-5. Pin Name Mapping Varies Between Versions

Pin Name	Sense Version (GPIO)	Plus Version (GPIO)
D11	GPIO42 (PDM_CLK)	GPIO38
D12	GPIO41 (PDM_DATA)	GPIO39
D13	-	GPIO40
D14	-	GPIO41
D15	-	GPIO42

GPIO42 appears as D11 on Sense but as D15 on Plus. GPIO41 appears as D12 on Sense but as D14 on Plus. On Standard and Sense, D11 and D12 are board labels only and are not defined in the Arduino board package. On Plus, D11–D19 are Arduino pin names. Use the native GPIOxx identifiers when writing cross-platform firmware.

3.5 GPIO Resource Mapping & Conflicts

The ESP32-S3 chip used in the XIAO series has a finite number of GPIO pins, and the ultra-compact XIAO form factor (21 × 17.8 mm) constrains how many can be physically broken out. To

maximize functionality within this footprint, the hardware design extensively utilizes pin multiplexing-assigning multiple logical functions to the same physical GPIO.

This approach provides flexibility but introduces potential resource conflicts when two or more functions attempt to use the same GPIO simultaneously. Understanding these conflicts is essential for successful hardware and firmware design.

This section categorizes the conflicts into three levels:

- **Internal Conflicts (Single Version)**: Multiplexing within one board version.
- **Cross-Version Naming Conflicts**: The same Arduino-style Dx pin name mapping to different GPIOs on different versions.
- **Cross-Version Hardware Conflicts**: Incompatibility when mounting the Sense Expansion Board on the Plus main board.

3.5.1 Standard Version Resource Notes

The Standard version has minimal resource conflicts due to its conservative pin breakout. However, the following system-level allocations should be noted:

Table 3-6. Standard Version Reserved GPIO Summary

SoC Pin	System Function	Notes
GPIO0	BOOT Button	Active Low. Directly connected to the BOOT button. Available as a general-purpose input when the button is not pressed, but avoid using as an output to prevent boot-mode issues.
GPIO21	USER LED (LED_BUILTIN)	Active Low. The on-board user LED is hardwired to this pin. Using GPIO21 for other purposes will affect LED behavior.
GPIO20 / GPIO19	USB D+ / D-	Reserved for native USB communication. Not available for general use.
GPIO39 ~ GPIO42	JTAG (MTCK/MTDO/MTDI/MTMS)	Available on bottom-side pads. These GPIOs are shared with external four-wire JTAG; see Section 5.12 for USB Serial/JTAG.

D2/GPIO3 is the JTAG signal-source strapping pin. It is sampled only when EFUSE_STRAP_JTAG_SEL is burned. This eFuse is not burned by default.

3.5.2 Sense Version Conflicts

The Sense Expansion Board connects via the B2B connector and occupies a significant number of GPIOs for its integrated peripherals (camera, microphone, and MicroSD card). This creates three categories of conflict.

3.5.2.1 JTAG vs. Camera & Microphone

The camera SCCB lines and PDM microphone share GPIO39-42 with external four-wire JTAG. Allocate these pins to either the connected peripherals or the external JTAG interface. USB Serial/JTAG uses a separate interface; see Section 5.12.

Table 3-7. Sense Version - JTAG Conflicts

SoC Pin	JTAG Function	Sense Board Function	Conflict
GPIO39	MTCK	CAM_SCL (Camera I2C Clock)	GPIO39 is shared by camera control and external JTAG MTCK.
GPIO40	MTDO	CAM_SDA (Camera I2C Data)	GPIO40 is shared by camera control and external JTAG MTDO.
GPIO41	MTDI	PDM_DATA (Microphone) / J2 / D12	Three-way conflict: JTAG, Microphone, and D12 expansion pad.
GPIO42	MTMS	PDM_CLK (Microphone) / J1 / D11	Three-way conflict: JTAG, Microphone, and D11 expansion pad.

3.5.2.2 Microphone vs. Expansion Pads (D11 / D12)

The Sense board's two expansion pads (J1 and J2) reuse the same GPIOs as the PDM microphone. These functions cannot operate simultaneously.

Table 3-8. Sense Version - Microphone vs. Expansion Pad Conflicts

SoC Pin	Microphone Function	Expansion Pad	Resolution
GPIO42	PDM_CLK	J1 / D11	Cut solder jumper JP1 to disconnect the microphone clock and free GPIO42 for D11 use.
GPIO41	PDM_DATA	J2 / D12	Cut solder jumper JP2 to disconnect the microphone data and free GPIO41 for D12 use.

Cutting JP1 or JP2 will disconnect the PDM microphone from the corresponding GPIO, rendering the microphone non-functional. This modification is reversible - the solder jumper can be re-bridged with solder to restore the microphone connection when needed.

3.5.2.3 MicroSD Card - Shared SPI Bus & CS Pin

The MicroSD card slot on the Sense Expansion Board shares the standard SPI bus with the user-accessible header pins (D8, D9, D10). While SPI is inherently a multi-device bus protocol that supports sharing via individual Chip Select (CS) lines, the following hardware design

details must be considered:

Table 3-9. Sense Version - MicroSD SPI Bus Sharing

SoC Pin	Standard Header Pin	MicroSD Function	Hardware Notes
GPIO7	D8 / SCK	SD_SCK	22Ω series resistor (R2) on the expansion board between the header and SD card.
GPIO8	D9 / MISO	SD_MISO	22Ω series resistor (R1) on the expansion board.
GPIO9	D10 / MOSI	SD_MOSI	22Ω series resistor (R3) on the expansion board.
GPIO21	USER_LED	SD_CS (Default)	Active Low. Directly conflicts with the on-board USER LED (see note below).

1. **SPI Bus Sharing Is Possible**: Other SPI peripherals can share the SCK/MISO/MOSI lines with the SD card, provided each device has its own dedicated CS line and the SD card's CS is held HIGH (deselected) when communicating with other devices.
2. **Series Resistors**: The 22Ω series resistors (R1–R3) on the expansion board provide signal integrity and short-circuit protection for the SD-card branch. Because the SD-card branch remains connected to D8–D10, validate the maximum SPI clock when other SPI devices share these pins.
3. **Pull-Up Resistors**: The expansion board includes 4.7KΩ pull-up resistors on the SPI lines, enabled by solder jumper JP3. These are required for proper SD card initialization but may affect other SPI slaves on the shared bus.
4. **SD_CS Conflicts with USER LED**: By default, the SD card's Chip Select is routed to GPIO21 via a 0Ω resistor (R12). Since GPIO21 is also hardwired to the on-board USER LED, the LED will toggle during SD card operations. To resolve this, advanced users can relocate the 0Ω resistor from R12 to R11, rerouting SD_CS to D2 (GPIO3) instead. This frees GPIO21 for normal LED operation but occupies D2.

3.5.3 Plus Version Conflicts

The Plus version exposes nine additional GPIOs on D11-D19. Allocate each GPIO according to the external JTAG and peripheral functions used by the application. The general-purpose SPI controller names and pin routing are described in Section 5.4.

3.5.3.1 JTAG Conflicts

Table 3-10. Plus Version - JTAG Conflicts

SoC Pin	JTAG Function[9]	Plus Extended Pin	Conflict
GPIO39	MTCK	D12	GPIO39 is shared with external JTAG MTCK.
GPIO40	MTDO	D13	GPIO40 is shared with external JTAG MTDO.
GPIO41	MTDI	D14	GPIO41 is shared with external JTAG MTDI.
GPIO42	MTMS	D15	GPIO42 is shared with external JTAG MTMS.

[9] *Note: External four-wire JTAG requires the complete GPIO39-42 signal group. USB Serial/JTAG is available as a separate debugging interface when its USB pins are assigned to that function.*

3.5.3.2 Pin Name Mapping Conflicts (Sense vs. Plus)

Because the Sense and Plus versions route different physical GPIOs to the same Arduino-style Dx pin names, code using Dx identifiers is NOT portable between versions.

Table 3-11. Cross-Version Pin Name Mapping

Arduino Pin Name	Sense Version (GPIO)	Plus Version (GPIO)
D0 – D10	GPIO1–9, 43, 44	GPIO1–9, 43, 44
D11	GPIO42 (PDM_CLK)	GPIO38
D12	GPIO41 (PDM_DATA)	GPIO39
D13	-	GPIO40
D14	-	GPIO41
D15	-	GPIO42
D16 – D19	-	GPIO10, 13, 12, 11

GPIO42 is D11 on Sense but D15 on Plus. GPIO41 is D12 on Sense but D14 on Plus. When writing firmware intended for multiple board versions, always use the native GPIOxx identifiers instead of Dx labels. D11 and D12 are not defined in the Arduino board package for Standard and Sense.

3.5.4 Plus and Sense Peripheral Resource Comparison

The GPIO assignments in Table 3-12 compare the Plus extended pins with the Sense peripheral

signals. The Sense camera expansion board is supported with the matching Sense main board. The Plus B2B connector is not compatible with the plug-in camera sensor board, according to the product compatibility information.

Table 3-12. GPIO Resource Comparison Between Plus and Sense

Plus Pin	SoC Pin	Plus Function	Sense Board Function
D11	GPIO38	General I/O / I2S_SD	DVP_VSYNC (Camera)
D12	GPIO39	General I/O / I2S_SCK	CAM_SCL (Camera I2C)
D13	GPIO40	General I/O / I2S_WS	CAM_SDA (Camera I2C)
D14	GPIO41	General I/O / UART1_RX	PDM_DATA (Microphone)
D15	GPIO42	General I/O / UART1_TX	PDM_CLK (Microphone)
D16	GPIO10	ADC	XMCLK (Camera Master Clock)
D17	GPIO13	SPI1_SCK	DVP_PCLK (Camera Pixel Clock)
D18	GPIO12	SPI1_MISO	DVP_Y7 (Camera Data Bit 7)
D19	GPIO11	SPI1_MOSI	DVP_Y8 (Camera Data Bit 8)

4. Power Management

This chapter describes the power supply architecture, battery charging management, low-power operating modes, and power-on/reset timing of the XIAO ESP32-S3 series. Understanding the power subsystem is critical for designing battery-powered, energy-efficient, and reliable applications.

4.1 Power Architecture

4.1.1 Power System Block Diagram

The XIAO ESP32-S3 series supports USB and battery inputs. A power-path circuit selects the source for the DC-DC regulator, while the charger manages battery charging.

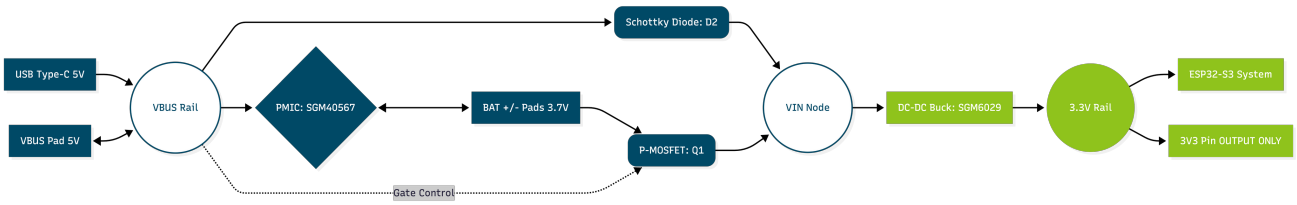


Figure 4-1. Power System Block Diagram of XIAO ESP32-S3 Series

4.1.2 Power Path Description

The board accepts a nominal 5V USB supply and a single-cell lithium battery with a nominal voltage of 3.7V. The power-path circuit selects the source according to the presence of USB power.

When USB is connected, VBUS supplies the system through the Schottky-diode path and supplies the battery charger. The P-channel MOSFET isolates the battery path from the system input. When USB is disconnected, the MOSFET enables the battery path to the DC-DC regulator.

The DC-DC buck converter accepts input from either source and generates a regulated 3.3V rail that powers the ESP32-S3 SoC, PSRAM, Flash, and all I/O. The 3.3V rail is also routed to the B2B connector to supply expansion board peripherals.

Table 4-1. Power Path Overview

Power Path	Source	Voltage	Description
Primary Input	USB Type-C (VBUS)	5V	Main power input. VBUS passes through the Schottky diode to the DC-DC regulator input. Simultaneously supplies the PMIC for battery charging.
Secondary Input	Lithium Battery (BAT± Pads)	3.7V (Nominal)	Battery power passes through the P-channel MOSFET to the regulator input when USB is disconnected. The charger controls battery charging.
System Rail	3.3V Regulated Output	3.3V	Generated by the DC-DC buck converter. Output only - do not apply external voltage.

The BAT± pads do not have reverse polarity protection. Connecting a battery with reversed polarity will permanently damage the PMIC and potentially the ESP32-S3 SoC. Always verify battery polarity before connection.

4.2 Supply Specifications

Table 4-2. Supply Reference Values and Board Measurements

Parameter	Version	Conditions	Value	Unit
USB Input Voltage	All	USB Type-C input	5.0	V
Battery input voltage	All	Single-cell Li-ion or Li-Po; nominal 3.7V	3.3-4.2	V
USB Input Current	Standard	System active, No charging[10]	51.82	mA
	Sense	System active, No charging[10]	55.85	mA
	Plus	System active, No charging[10]	50.15	mA
USB Input Current	Standard	System active + Charging	155.53	mA
	Sense	System active + Charging	164.33	mA
	Plus	System active + Charging	152.60	mA
USB Input Current	Standard	System Hibernation + Charging	103.59	mA
	Sense	System Hibernation + Charging	111.10	mA
	Plus	System Hibernation + Charging	102.12	mA
3.3V total load	All	USB supply + includes board current	1000	mA

Parameter	Version	Conditions	Value	Unit
capability		Battery supply + includes board current	650	mA
3.3V Output Voltage	All	DC-DC Output	3.29	V
VBUS load-test current	Plus	USB 5.00 V; pad-voltage drop 0.25 V; test under 10 s; temperature rise observed	2.3	A
	Sense		2.8	A

[10] *Note: USB input currents were measured with a 5.0V USB supply. The Sense current and load-test results in this table were obtained using an OV3660-equipped test unit. The operating and charging states are listed in the table. These results describe the recorded test configuration.*

Note: The VBUS load tests were performed for less than 10 s, with a 0.25 V drop at the VBUS pad and an observed temperature rise. These entries describe the recorded short-duration tests.

The 3V3 pin is a regulated output. The reported 3.3V load-test results include current consumed by the board. Calculate the current available to external peripherals after subtracting the current used by the main board and attached peripherals.

4.3 Power Supply Circuit Design

4.3.1 USB Power Supply

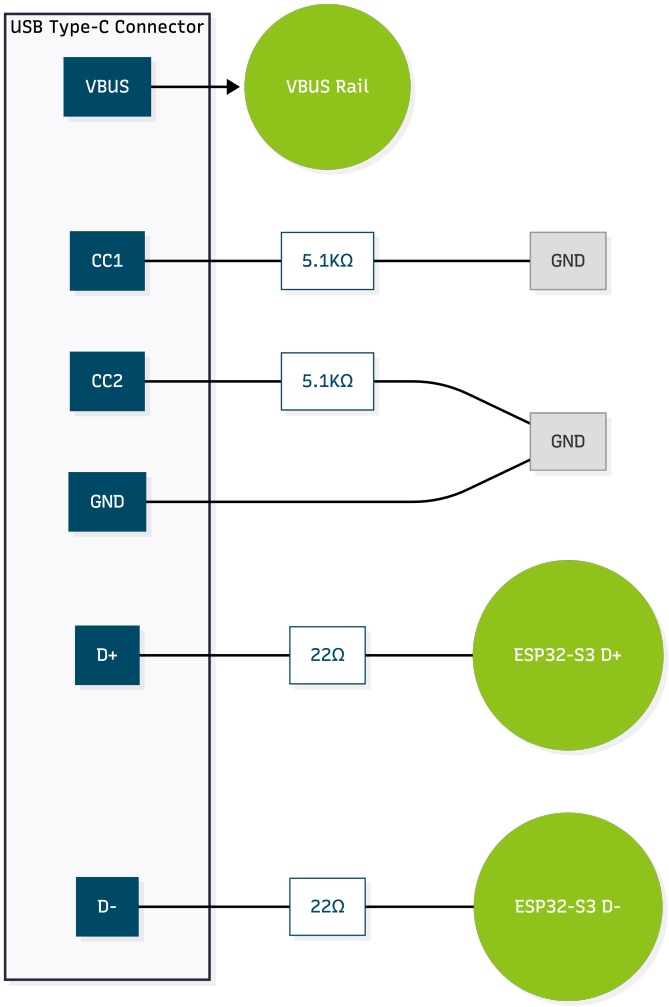


Figure 4-2. USB Type-C Interface Circuit

The USB Type-C connector is configured as a UFP (Upstream Facing Port) / Sink device with 5.1K**Ω** pull-down resistors on both CC lines. The board does not support USB Power Delivery negotiation and operates at the default 5V only. The USB data lines include 22**Ω** series resistors for signal integrity.

The VBUS pin on the header mirrors the USB 5V rail. When USB is connected, it provides 5V output for external peripherals. It can also accept an external regulated 5V input when USB is disconnected. Connect the external supply through a series Schottky diode (anode to the supply, cathode to the 5V pin) to prevent back-feeding the USB host. This is the only alternative power input besides USB Type-C and battery - do not use the 3V3 pin as a power input.

4.3.2 Battery Charging & Supply

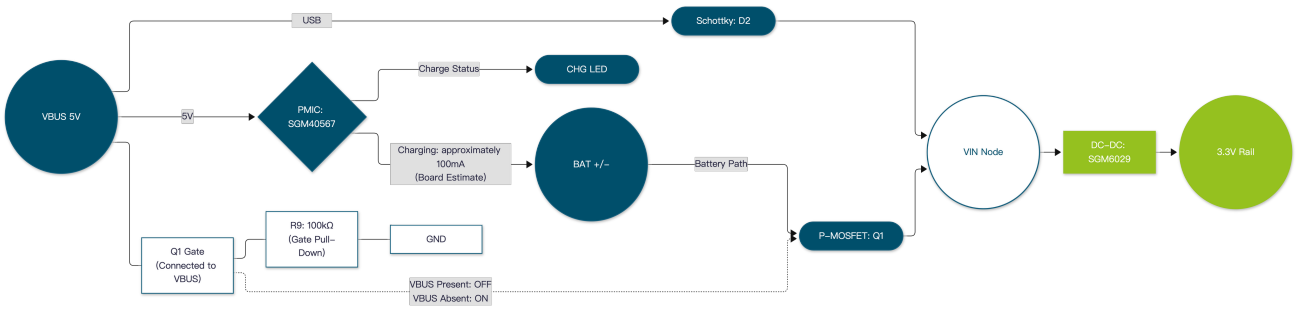


Figure 4-3. Battery Charging & Power Path Circuit

The board integrates an SGM40567-4.2XG/TR linear lithium battery charger that manages the complete CC/CV charging profile. The charge current is set by an external 220KΩ precision resistor on the IREF pin. The red CHG LED blinks while the battery is charging. After charging completes, it stays on for about 51 s and then turns off. With USB connected and no battery, it lights briefly and then turns off.

The power-path circuit uses an LP0404N3T5G P-channel MOSFET on the battery path and an LMBR4010BST5G Schottky diode on the USB path. The gate of Q1 is connected to VBUS. R9 (100kΩ) pulls the gate to GND when VBUS is absent, enabling the battery supply path. When USB power is present, VBUS drives the gate high and turns Q1 off.

Table 4-3. Battery Charging Specifications

Parameter	Specification	Unit	Notes
Charger IC	SGM40567-4.2XG/TR	-	-
Charge Voltage	4.2	V	-
Estimated board charging current	Approximately 100	mA	Estimated from USB input-current measurements during charging

Only use single-cell 3.7V Li-Ion or Li-Po batteries with built-in protection circuits. The BAT± pads have no on-board reverse polarity protection.

The values in this table are component specifications. Board-level load-test results for USB and battery supply are listed in Table 4-2.

Table 4-4. DC-DC Regulator Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Regulator IC	SGM6029CYG/TR	-	-	-	-
Input Voltage Range	-	1.95	-	5.5	V
Output Voltage	-	3.2	3.3	3.4	V
IC output-current rating	SGM6029C; VIN >= 2.3 V; component rating	-	-	1000	mA
Switching Frequency	SGM6029C Version	-	4.0	-	MHz
Quiescent Current	No load	-	2.3	-	µA

4.3.3 3V3 Pin Usage

The 3V3 pin is the regulated output of the on-board DC-DC converter. Power the board through USB Type-C, the VBUS input, or the BAT pads. For external peripherals powered from 3V3, calculate the available current using the supply-specific total load result in Table 4-2, after subtracting current consumed by the main board and attached peripherals.

The XIAO ESP32-S3 supports three power input methods: USB Type-C, lithium battery via BAT± pads, and external 5V via the VBUS header pin.

4.4 Power Consumption

4.4.1 Operating Mode Overview

The ESP32-S3 SoC provides multiple power management modes with progressive levels of power reduction.

Table 4-5. ESP32-S3 Power Modes Summary

Mode	CPU	Wi-Fi / BT	RTC	Main RAM	ULP	Typical Use Case
Active	Running	Available	On	On	Available	Normal operation
Modem-sleep	Running	Off	On	On	Available	CPU tasks without wireless
Light-sleep	Paused	Off	On	Retained	Available	Periodic polling, low-latency wakeup
Deep-sleep	Off	Off	On	Off	Available	Long-interval logging, standby
Hibernation	Off	Off	Partial	Off	Off	Ultra-long standby; RTC timer or

Mode	CPU	Wi-Fi / BT	RTC	Main RAM	ULP	Typical Use Case
						EXT1 wakeup

In Deep-sleep mode, main RAM content is lost. Only RTC memory (8KB slow + 8KB fast) is retained for variables declared with RTC_DATA_ATTR. Hibernation is Deep-sleep with the RTC peripherals and RTC memory powered down. The internal fast RC oscillator (RC_FAST_CLK, about 17.5 MHz) and the ULP co-processor are also powered down, leaving only the RTC timer and EXT1-capable RTC GPIOs functional.

4.4.2 Detailed Power Consumption Parameters

All measurements were taken at 25˚C with a 3.7V Li-Po battery supply and no external peripheral loads. All Sense current measurements in Section 4.4 were taken using an OV3660-equipped unit and are retained as historical reference data for that configuration. Current measurements for the OV5640-equipped Sense are not yet available.

Table 4-6. Measured Current by Operating Mode (Battery 3.7V)

Mode	Conditions	XIAO ESP32-S3	XIAO ESP32-S3 Sense (OV3660)	XIAO ESP32-S3 Plus
Wi-Fi TX	802.11b; maximum configured RF transmit power	167.72 mA	185.93 mA	168.76 mA
Wi-Fi RX	Wi-Fi receive/listen state	92.83 mA	99.11 mA	93.28 mA
BLE advertising	Continuous advertising	31.90 mA	36.99 mA	32.79 mA
Active	CPU 240 MHz; Wi-Fi and Bluetooth RF disabled	61.52 mA	66.75 mA	61.74 mA
Modem-sleep	CPU running; wireless RF disabled	35.08 mA	39.62 mA	38.41 mA
Light-sleep	CPU paused; Sense microphone and SD communication disabled	2.10 mA	2.98 mA	2.26 mA
Deep-sleep	RTC low-power operation; Sense microphone and SD communication disabled	18.39 µA	2.28 mA	19.40 µA
Hibernation	RTC timer retained; Sense microphone and SD communication disabled	17.47µA	2.28 mA	17.95 µA

Measurements were taken at 25˚C with a 3.7 V Li-Po battery supply and no external load. The

Standard measurements exclude the Sense expansion board, while the Sense measurements include the expansion board. The microphone and SD-card communication were disabled for the Sense Light-sleep, Deep-sleep, and Hibernation tests.

With a 3.7V battery supply, measured Deep-sleep current was 18.39μA for Standard, 2.28mA for the OV3660-equipped Sense with the expansion board attached, and 19.40μA for Plus. The Sense sleep measurements were taken with microphone and SD-card communication disabled.

4.4.3 XIAO ESP32-S3 Sense Power Consumption Notes

The following values describe the OV3660-equipped Sense test assembly and the measured current difference introduced by its complete expansion board.

Table 4-7. Sense Sleep Current and Expansion-Board Overhead (OV3660 Test Configuration)

Measurement	Result	Conditions
Sense Deep-sleep current	2.28 mA	3.7 V battery; expansion board attached; microphone and SD-card communication disabled
Sense Hibernation current	2.28 mA	3.7 V battery; expansion board attached; microphone and SD-card communication disabled
Aggregate expansion-board static-current difference	Approximately 2.26 mA	Reported Sense-minus-Standard static-current difference

Low-power measurements for Standard, Sense, and Plus are listed in Table 4-6. The attached Sense expansion board adds static current. Evaluate the complete assembly after changing peripheral activity, jumper settings, or connected accessories.

The Sense version is not recommended for applications requiring ultra-low-power deep-sleep over extended periods. For such use cases, the Standard or Plus version is preferred.

4.4.4 Sleep Wakeup Sources

Table 4-8. Sleep Wakeup Sources

Wakeup Source	Description	Available Pins on XIAO
EXT0	Single RTC GPIO level trigger (HIGH or LOW)	D0–D5, D8–D10
EXT1	Multi-pin RTC GPIO level trigger: any HIGH or any LOW	D0–D5, D8–D10
Timer	RTC timer interval; time specified in microseconds; resolution depends on RTC clock	Internal

Wakeup Source	Description	Available Pins on XIAO
Touch Pad	Capacitive touch detection	D0–D5, D8–D10
ULP Co-processor	Condition triggered by ULP program	Internal
GPIO (Light-sleep only)	Selected HIGH or LOW level on a configured GPIO	All GPIOs

The Plus version provides 4 additional RTC-capable wakeup pins on the extended pads:

Table 4-9. Plus Version - Additional RTC Wakeup Pins

Plus Pin	SoC Pin	RTC GPIO	Touch Channel
D16	GPIO10	RTC_GPIO10	Touch10
D17	GPIO13	RTC_GPIO13	Touch13
D18	GPIO12	RTC_GPIO12	Touch12
D19	GPIO11	RTC_GPIO11	Touch11

4.4.5 Low-Power Design Recommendations

Table 4-10. Low-Power Design Checklist

Category	Recommendation	Expected Impact
Wi-Fi	Enable power save mode (WIFI_PS_MIN_MODEM or WIFI_PS_MAX_MODEM). Use Modem-sleep or Light-sleep between transmissions.	Reduces average current between wireless transfers
BLE	Maximize advertising and connection intervals.	Proportional average current reduction
CPU Frequency	Reduce from 240 MHz to 160 or 80 MHz when full performance is not needed. Use 40 MHz only when Wi-Fi and Bluetooth are off.	Current depends on CPU frequency and workload
Unused GPIOs	Configure unused pins to a defined state appropriate for the external circuit.	Controls leakage paths associated with pin states
Peripherals	Disable unused peripherals in firmware.	Reduces quiescent current
Flash / PSRAM	Configure Flash and PSRAM power management for the selected ESP-IDF release.	Depends on the memory power configuration

Category	Recommendation	Expected Impact
USER LED	Drive GPIO21 HIGH before sleep to turn the active-low user LED off.	Removes current used by the user LED
Sense Peripherals	Configure microphone and SD-card activity for sleep and measure the complete assembly.	See measured assembly currents in Table 4-6
External Loads	Use GPIO-controlled switches to cut power to external sensors during sleep.	Eliminates external quiescent current

5. Peripherals and Interfaces

The Seeed Studio XIAO ESP32-S3 series is built upon the Espressif ESP32-S3R8 SoC, which features a highly flexible I/O MUX and GPIO Matrix. This architecture allows the hardware to remap internal peripheral signals to any physical pin. The following sections define the default interface assignments and the electrical specifications for integrated components.

5.1 USB Interface

5.1.1 Interface Specifications

The XIAO ESP32-S3 utilizes the native USB PHY of the ESP32-S3 SoC, eliminating the need for an external USB-to-Serial bridge. This direct connection supports multiple logical device classes simultaneously.

Table 5-1. USB Interface Specifications

Parameter	Specification
Interface Type	USB Type-C
USB Version	USB 2.0 Full Speed
Data Rate	Up to 12 Mbps
Native Functions	Bus Power, UART/CDC Communication, JTAG Debugging, DFU Firmware Download
Driver Class	CDC-ACM (Plug-and-play)

5.1.2 Reference Circuit

The USB data lines (D+/D-) are implemented with 22 Ω series resistors to achieve impedance matching and enhance signal integrity. The CC1 and CC2 lines utilize 5.1 kΩ pull-down resistors, identifying the board as a UFP (Upstream Facing Port) to the USB host. For applications requiring enhanced ESD protection beyond the SoC's internal capabilities, DNP footprints (C1/C2, 0201) are reserved between USB D+/D− and GND.

5.2 UART Interface

The XIAO ESP32-S3 provides multiple hardware Universal Asynchronous Receiver-Transmitter (UART) resources. While the primary system console and firmware logging are handled via the

native USB interface (logical Serial), the edge pins D6 and D7 expose hardware UART0 (Arduino Serial0). D6 (TX) has a 499 Ω series resistor (R6) on the main board. This allows for full-duplex asynchronous communication with external modules such as GNSS, sensors, or other microcontrollers.

5.2.1 Interface Specifications

The UART controller in the ESP32-S3 is highly flexible, featuring hardware-supported DMA for high-speed data throughput and independent FIFOs for both transmit and receive paths.

Table 5-2. UART Interface Specifications

Parameter	Specification
Default Baud Rate	115200 bps
Supported Baud Rate	300 bps to 5,000,000 bps
Data Bits	5, 6, 7, 8
Stop Bits	1, 1.5, 2
Parity	None, Even, Odd
Logic Level	3.3V CMOS

5.2.2 Pin Mapping (Default)

To maintain compatibility with the XIAO pinout standard, the hardware UART is mapped to the following pins. While these are the defaults in the Board Support Package (BSP), the GPIO Matrix allows remapping to other pins if required.

Table 5-3. UART Pin Mapping (Default)

Signal	XIAO Pin	SoC GPIO	Direction	Description
TX	D6	GPIO 43	Output	UART Transmit Data (499 Ω series resistor)
RX	D7	GPIO 44	Input	UART Receive Data

5.2.3 Application Circuitry

The UART interface operates strictly at 3.3V logic levels. Designers must adhere to the following guidelines for reliable integration:

- 3.3V Device Interconnect: For devices operating on the same 3.3V rail, a direct point-to-point connection is sufficient.
- 5V device interconnect: Use a suitable level shifter, or a voltage divider on the XIAO RX path, when connecting 5V logic. A 5V signal applied directly to D7 exceeds the GPIO

input-voltage rating.

- Signal Integrity: For high baud rates (> 1 Mbps), traces should be kept short and isolated from high-frequency switching nodes (like the DC-DC inductor) to minimize EMI.

5.3 I2C Interface

The XIAO ESP32-S3 series includes two hardware I2C (Inter-Integrated Circuit) controllers. By default, one controller is assigned to the edge headers to facilitate communication with a wide array of digital sensors, OLED displays, and port expanders.

5.3.1 Interface Specifications

The I2C interface utilizes an open-drain architecture, allowing multiple devices to share the same bus. The ESP32-S3 hardware supports advanced features such as clock stretching (for slow slaves) and multi-master arbitration.

Table 5-4. I2C Interface Specifications

Parameter	Specification
Supported Modes	Master and Slave
Speed Modes	Standard mode (100 kHz); Fast mode (400 kHz)
Addressing Mode	7-bit and 10-bit Addressing
FIFO Buffer	32 Bytes for both TX and RX
Logic Level	3.3V CMOS (Open-Drain compatible)
Internal Pull-ups	None (Hardware Level)[11]

[11] *Note: While the ESP32-S3 SoC provides weak internal software-enabled pull-ups (~45 kΩ), these are insufficient for I2C communication. Physical external resistors must be used for reliable operation.*

5.3.2 Pin Mapping (Default)

The default I2C mapping follows the XIAO pinout standard. These pins can be reconfigured to other GPIOs through the GPIO Matrix if the default pins are required for other functions.

Table 5-5. I2C Pin Mapping (Default)

Signal	XIAO Pin	SoC GPIO	Direction	Description
SDA	D4	GPIO 5	Bi-directional	I2C Data Line
SCL	D5	GPIO 6	Output	I2C Clock Line

5.3.3 External Pull-up Resistor Selection

Since the XIAO ESP32-S3 does not integrate on-board I2C pull-up resistors, the developer must provide them on the carrier board. The choice of resistance value is a trade-off between power consumption and signal rise time (bandwidth).

- **Standard/Fast Mode (100-400 kbps):** 4.7 kΩ to 10 kΩ resistors are recommended for general-purpose applications with short bus lengths.
- **Pull-up selection**: Select resistance according to the target 100 kHz or 400 kHz bus speed, total bus capacitance, rise time, and device sink-current capability.
- **Low Power Applications:** Higher values (10 kΩ+) reduce current consumption when the bus is active but limit the maximum reliable clock speed.

5.3.4 Bus Topology and Capacitance Limits

The I2C bus is physically limited by the total bus capacitance (C_b), which includes the traces of the PCB and the internal capacitance of every connected device.

- **Maximum Capacitance:** The total bus capacitance should not exceed 400 pF.
- **Device Limit:** While the 7-bit address space provides 112 usable addresses, the physical limit is typically 10-20 devices before signal integrity degrades due to cumulative capacitance.
- **Wiring Recommendation:** For high-speed I2C, avoid long jumper wires. Use a solid ground plane beneath the SDA/SCL traces to provide a clean return path and minimize crosstalk.

5.4 SPI Interface

The XIAO ESP32-S3 series provides high-performance synchronous serial communication via the SoC's GPSPI (General Purpose SPI) controllers. The series supports multiple hardware SPI instances, featuring integrated DMA (Direct Memory Access) to handle high-speed data transfers without significant CPU overhead.

5.4.1 Interface Specifications

The SPI controllers support various operational modes and data widths, making them suitable for high-speed displays, external memory, and precision sensors.

Table 5-6. SPI Interface Specifications

Parameter	Specification
Supported Modes	Master and Slave
Max Clock Speed	80 MHz (SoC limit) / 40 MHz (Recommended for stable PCB routing)
Transfer Length	Firmware-configurable; supports buffer transfers and DMA
SPI Modes	Mode 0, 1, 2, 3 (CPOL/CPHA configurable)
Bit Order	MSB First or LSB First
DMA Support	Hardware DMA with linked-list descriptors

5.4.2 Pin Mapping (Primary SPI - All Versions)

The primary SPI pin group is exposed on D8/SCK, D9/MISO, and D10/MOSI. On Sense, these pins are shared with the MicroSD interface. Select a general-purpose SPI controller and configure the pin routing in firmware.

Table 5-7. Primary SPI Pin Mapping (Standard Headers)

Signal Name	XIAO Pin	SoC GPIO	Direction	Function Description
SCK	D8	GPIO 7	Output	SPI Serial Clock
MISO	D9	GPIO 8	Input	Master In Slave Out
MOSI	D10	GPIO 9	Output	Master Out Slave In
CS	User Defined	-	Output	General Purpose Chip Select

5.4.3 Additional SPI Pin Group (Plus Version Only)

On the Plus version, the Arduino SPI1 pin group uses D17/GPIO13 for SPI1_SCK, D18/GPIO12 for SPI1_MISO, and D19/GPIO11 for SPI1_MOSI. Configure this pin routing in firmware. For independent operation, assign this group and the edge-header group to separate general-purpose SPI controllers.

Table 5-8. Additional SPI Pin Mapping (Plus Staggered Pads)

Signal Name	XIAO Pin	SoC GPIO	Direction	Function Description
SPI1_SCK	D17	GPIO 13	Output	SPI1 Serial Clock
SPI1_MISO	D18	GPIO 12	Input	SPI1 Master In Slave Out
SPI1_MOSI	D19	GPIO 11	Output	SPI1 Master Out Slave In
SPI1_CS0	User Defined	-	Output	Use any available GPIO as Software CS

5.4.4 Shared SPI Bus Considerations (Sense Version)

On the XIAO ESP32-S3 Sense, the primary SPI bus (D8-D10) is shared between the user-accessible headers and the integrated MicroSD card slot on the expansion board.

- Chip Select (CS): By default, the SD card's Chip Select is routed to GPIO 21 (shared with the USER LED). For independent operation, users can remap the CS to D2 (GPIO 3) by relocating the on-board 0 **Ω** resistor (R12 to R11).
- Bus Contention: When using additional SPI slaves on the edge headers (D8-D10), ensure that all Slave Select pins are held HIGH when the bus is idle to prevent interference with SD card operations.

5.4.5 Signal Integrity and Layout

For high-speed SPI operation (> 20 MHz), traces should be kept as short as possible. For the Plus version's extended pads, provide a continuous ground plane on the carrier board beneath the SPI traces to minimize crosstalk between the primary and secondary SPI buses.

5.5 ADC Interface

The XIAO ESP32-S3 series utilizes two 12-bit SAR ADCs. To ensure maximum stability and Wi-Fi compatibility, the hardware design prioritizes ADC1 for the primary analog pins.

5.5.1 Interface Specifications

The ADC channels support multiple attenuation levels, enabling a wide dynamic range. By default, the Arduino core uses ATTEN3 (12 dB, named 11 dB in earlier releases) for the maximum measurable input voltage.

Table 5-9. ADC Interface Specifications

Parameter	Specification
Resolution	12-bit (0 - 4095 levels)
Input Range	Depends on attenuation and calibration; see Section 6.3.2
Sample Rate	Up to 100kSPS (SoC datasheet specification)
Reference Voltage	Internal 1100 mV (Factory Calibrated)
Input Impedance	> 1 MΩ

5.5.2 ADC1 Channel Mapping (High Compatibility)

The standard analog header pins A0-A5 and A8-A10 are routed to ADC1. ADC1 is recommended for analog acquisition during wireless operation. The available pins and ADC channels are listed in Table 5-10.

Table 5-10. ADC1 Pin Mapping (Available on All Versions)

XIAO Pin	Arduino Name	SoC GPIO	ADC Channel	Function
D0	A0	GPIO 1	ADC1_CH0	General Analog Input
D1	A1	GPIO 2	ADC1_CH1	General Analog Input
D2	A2	GPIO 3	ADC1_CH2	General Analog Input
D3	A3	GPIO 4	ADC1_CH3	General Analog Input
D4	A4	GPIO 5	ADC1_CH4	General Analog Input
D5	A5	GPIO 6	ADC1_CH5	General Analog Input
D8	A8	GPIO 7	ADC1_CH6	General Analog Input
D9	A9	GPIO 8	ADC1_CH7	General Analog Input
D10	A10	GPIO 9	ADC1_CH8	General Analog Input

5.5.3 Plus Version ADC Expansion

The XIAO ESP32-S3 Plus variant breaks out 4 additional analog channels via its staggered pads. Note that D16 is routed to ADC1, while D17–D19 utilize ADC2.

Table 5-11. Extended ADC Mapping (Plus Staggered Pads)

XIAO Pin	SoC GPIO	ADC Controller	ADC Channel	Primary Function
D16	GPIO 10	ADC1	ADC1_CH9	General Analog Input
D17	GPIO 13	ADC2	ADC2_CH2	General Analog Input[12]
D18	GPIO 12	ADC2	ADC2_CH1	General Analog Input[12]
D19	GPIO 11	ADC2	ADC2_CH0	General Analog Input[12]

[12] *Note: ADC2 shares hardware resources with Wi-Fi. Follow the concurrency requirements of the selected ESP-IDF ADC driver. ADC1 is recommended for analog acquisition during wireless operation.*

5.5.4 Battery Monitoring (Plus Version Only)

GPIO10 (D16, named ADC_BAT in the Arduino variant) is available as ADC1_CH9. Battery-voltage measurement requires an external resistor divider between BAT+ and GND, with its midpoint connected to GPIO10. Select the divider ratio for the configured ADC input range.

5.5.5 Design Recommendations for Voltage Measurement

For precision voltage measurement, select attenuation and calibration for the required input range. The board-level ADC ranges are listed in Section 6.3.2. An input RC filter may reduce noise. Use a suitable voltage divider when the signal exceeds the selected ADC range or the GPIO input-voltage rating.

5.6 PWM Output (LEDC Controller)

The XIAO ESP32-S3 series utilizes the SoC's integrated LEDC (LED Control) peripheral to generate PWM waveforms. A key advantage of the ESP32-S3 architecture is that PWM signals can be internally routed to any available digital GPIO via the GPIO Matrix, providing maximum flexibility for carrier board design.

Table 5-12. PWM (LEDC) Interface Specifications

Parameter	Specification
Independent Channels	8 Channels
Assignable Pins	D0-D10 on all versions; Sense D11-D12 subject to microphone sharing; Plus D11-D19

Parameter	Specification
	subject to pin-function sharing
Timer Resolution	1-bit to 14-bit (Configurable)
Maximum Frequency	40 MHz (at 1-bit resolution)
Typical Functions	LED Dimming, Buzzer Control, Servo Driving, Clock Generation

The LEDC peripheral also features hardware-supported automatic fading (smooth transitions between duty cycles), which reduces CPU load during lighting effects.

5.7 Camera Interface (Sense Version Only)

The XIAO ESP32-S3 Sense incorporates a dedicated 8-bit Digital Video Port (DVP) interface, accessible via the 30-pin high-density B2B connector. The system is designed to leverage the ESP32-S3's internal Camera Slave controller, enabling hardware-accelerated image capture and processing.

5.7.1 Hardware Architecture

The camera subsystem uses a parallel data bus for high-bandwidth pixel transmission. The SoC provides the master clock (XMCLK) to the sensor, while the sensor provides the pixel clock (PCLK), horizontal reference (HREF), and vertical sync (VSYNC) to synchronize the data stream.

Table 5-13. Camera Interface Pin Mapping

Signal Name	SoC GPIO	Direction	Function
XMCLK	GPIO 10	Output	Master Clock (Typical: 20 MHz)
PCLK	GPIO 13	Input	Pixel Clock
VSYNC	GPIO 38	Input	Vertical Synchronization (Frame start)
HREF	GPIO 47	Input	Horizontal Reference (Line active)
DVP_Y2 – Y9	Various[13]	Input	8-bit Parallel Luminance/Data Bus
CAM_SCL	GPIO 39	Output	SCCB (I2C) Control Clock
CAM_SDA	GPIO 40	Bi-dir	SCCB (I2C) Control Data

[13] *Note: Refer to Table 2-4 for the complete mapping of DVP_Y2-Y9 to the ESP32-S3 GPIOs.*

5.7.2 Integrated Sensor Specifications (OV5640)

The standard Sense OV5640 camera module provides 5MP imaging with a fixed-focus F2.2 lens, a 68° field of view, and a specified minimum shooting distance of 20cm. It includes integrated image signal processing (ISP).

Table 5-14. Standard Sense OV5640 Camera Specifications

Parameter	Specification
Standard Sensor	OmniVision OV5640 (OmniBSI CMOS)
Resolution	5 Megapixels (2592×1944)
Output Formats	RAW RGB; RGB565/555/444; YUV422/420; YCbCr422; JPEG
Hardware Encoder	Integrated JPEG Compression
Maximum Frame Rate	See Table 2-3 for sensor-level theoretical frame-rate specifications
Optical FOV	68°
Aperture	F2.2
Focus Type	Fixed Focus (FF)
Minimum Shooting Distance	20cm
Dimensions	8 × 8 × 4.5 mm
Shutter Type	Rolling Shutter

5.8 Digital Microphone Interface (Sense Version Only)

The Sense expansion board provides a digital PDM microphone connected to GPIO42 for the clock and GPIO41 for data. The ESP32-S3 I2S peripheral receives the PDM signal for audio processing.

The ESP32-S3's I2S peripheral is configured in PDM mode to interface directly with the sensor. This hardware-level conversion from PDM bitstream to PCM (Pulse Code Modulation) audio significantly reduces CPU overhead for audio processing tasks.

Table 5-15. Digital Microphone Specifications

Parameter	Specification
Sensor Model	MSM261DGT006 (PDM Output)
Signal-to-Noise Ratio	65 dB
Clock Input	GPIO 42 (PDM_CLK)
Data Output	GPIO 41 (PDM_DATA)

5.9 MicroSD Card Interface (Sense Version Only)

To support local data logging and model storage for AI applications, the expansion board includes a push-pull MicroSD card slot.

5.9.1 Bus Configuration and Sharing

The MicroSD card uses SPI mode and shares SCK, MISO, and MOSI with the XIAO edge-header pins D8, D9, and D10.

Table 5-16. MicroSD Card Interface Specifications

Parameter	Specification
Interface Protocol	SPI mode
Supported File System	FAT32
Maximum Capacity	32 GB (SDHC Support)
Shared Pins	D8 (SCK), D9 (MISO), D10 (MOSI)
Default Chip Select	GPIO 21 (Shared with USER LED)

5.9.2 Hardware Customization (CS Remapping)

By default, the MicroSD Chip Select (CS) is tied to GPIO 21, which is also connected to the on-board USER LED. This causes the LED to toggle during SD card activity. Advanced users can decouple these functions by modifying the on-board 0 Ω resistor configuration:

- Default: Resistor on pad R12 (CS routed to GPIO 21).
- Optional: Relocate resistor to pad R11 (CS routed to D2 / GPIO 3).

5.9.3 Signal Integrity

The interface includes on-board 4.7 kΩ pull-up resistors (enabled via jumper JP3) on the SPI lines. These resistors ensure stable bus initialization and prevent signal floating when no card is inserted.

5.10 I2S Audio Interface (Plus Only)

The XIAO ESP32-S3 Plus utilizes its staggered expansion pads to provide a dedicated hardware I2S (Inter-IC Sound) interface for high-fidelity audio peripherals. This interface supports standard protocols including Philips and PCM, managed by hardware DMA to ensure low CPU overhead during audio streaming.

Table 5-17. I2S Interface Pin Mapping (Serial Audio)

Signal Name	XIAO Pin	SoC GPIO	Direction	Primary Function
I2S_SD	D11	GPIO 38	Bi-dir	Serial Data Line
I2S_SCK	D12	GPIO 39	Output	Continuous Serial Clock (BCLK)
I2S_WS	D13	GPIO 40	Output	Word Select (LRCLK)

5.11 PDM Microphone Interface (Plus Only)

Unlike the Sense version's integrated microphone, the Plus variant breaks out the PDM (Pulse Density Modulation) signals to physical pads. This allows for the integration of external digital microphone arrays or customized audio capture solutions for AI voice recognition.

Table 5-18. PDM Interface Pin Mapping

Signal Name	XIAO Pin	SoC GPIO	Direction	Function Description
PDM_DATA	D14	GPIO 41	Input	PDM Digital Audio Bitstream
PDM_CLK	D15	GPIO 42	Output	PDM Clock Output

5.12 Debugging and Test Points

The series supports external JTAG through GPIO39-42 and the USB Serial/JTAG interface. On Plus, the external JTAG signals are accessible through the extended pads and rear test pads. Refer to Chapter 7 for pad dimensions and Section 3.5 for peripheral sharing.

Table 5-19. JTAG Pad Assignment

JTAG Signal	SoC GPIO	XIAO Pad (Plus)	Rear Test Point	Function
MTCK	GPIO 39	D12	MTCK	JTAG Clock
MTMS	GPIO 42	D15	MTMS	JTAG Mode Select
MTDI	GPIO 41	D14	MTDI	JTAG Data In
MTDO	GPIO 40	D13	MTDO	JTAG Data Out

5.12.1 Reliability and Layout Guidelines

When developing custom carrier boards or test fixtures using pogo-pin arrays, debug traces should be routed directly from the SoC output to the contact point to minimize signal reflections and impedance discontinuities. For high-frequency lines such as TCK (JTAG Clock), "via stitching"—placing adjacent ground vias alongside the signal transitions—is recommended to provide a continuous return path and mitigate electromagnetic interference (EMI).

5.13 Low-Power Wakeup and RTC Resources

Low-power wakeup depends on the selected sleep mode, enabled wakeup sources, and RTC power-domain configuration. Table 5-20 lists the RTC-capable pins available on the board. Configure the wakeup source and power-down options for the application.

Table 5-20. RTC-Capable GPIOs and Wakeup Mapping

XIAO Pin	SoC GPIO	RTC Index	Touch Channel	Wakeup Support
D0	GPIO 1	RTC_GPIO 1	TOUCH 1	EXT0 / EXT1 / Touch
D1	GPIO 2	RTC_GPIO 2	TOUCH 2	EXT0 / EXT1 / Touch
D2	GPIO 3	RTC_GPIO 3	TOUCH 3	EXT0 / EXT1 / Touch
D3	GPIO 4	RTC_GPIO 4	TOUCH 4	EXT0 / EXT1 / Touch
D4	GPIO 5	RTC_GPIO 5	TOUCH 5	EXT0 / EXT1 / Touch
D5	GPIO 6	RTC_GPIO 6	TOUCH 6	EXT0 / EXT1 / Touch
D8	GPIO 7	RTC_GPIO 7	TOUCH 7	EXT0 / EXT1 / Touch
D9	GPIO 8	RTC_GPIO 8	TOUCH 8	EXT0 / EXT1 / Touch
D10	GPIO 9	RTC_GPIO 9	TOUCH 9	EXT0 / EXT1 / Touch

XIAO Pin	SoC GPIO	RTC Index	Touch Channel	Wakeup Support
D16	GPIO 10	RTC_GPIO 10	TOUCH 10	EXT0 / EXT1 / Touch (Plus Only)
D19	GPIO 11	RTC_GPIO 11	TOUCH 11	EXT0 / EXT1 / Touch (Plus Only)
D18	GPIO 12	RTC_GPIO 12	TOUCH 12	EXT0 / EXT1 / Touch (Plus Only)
D17	GPIO 13	RTC_GPIO 13	TOUCH 13	EXT0 / EXT1 / Touch (Plus Only)

Digital domain pins D6, D7, D11, D12, D13, D14, and D15 do not possess RTC capabilities. These pins cannot be used for EXT0/EXT1 wakeup or capacitive touch detection during Deep-sleep. When the system enters a low-power state, these pins enter a high-impedance mode and lose any previously set logic states unless explicitly configured for state-retention.

5.13.1 Hardware Wakeup Modes (EXT0 and EXT1)

EXT0 uses one RTC GPIO to trigger wakeup at a selected HIGH or LOW level. EXT1 uses a group of RTC GPIOs and triggers when any selected pin is HIGH or when any selected pin is LOW. Configure the trigger level and supported RTC pins for the ESP32-S3 target.

5.13.2 ULP Co-processor and Capacitive Touch

During Deep-sleep, the main Xtensa cores are powered off. The ULP coprocessor and touch controller can support low-power monitoring or wakeup when enabled with the required RTC power domains. Select the wakeup source and power configuration for the application before entering sleep.

5.14 On-board Connectors

The XIAO ESP32-S3 series utilizes industry-standard miniature connectors to provide external antenna support and high-density peripheral expansion. These components are selected for their balance of low-profile design and high-frequency signal integrity.

5.14.1 RF Interconnect (U.FL)

The RF front-end is terminated at a standard U.FL-R-SMT-1 (Hirose compatible) connector, designed for 2.4 GHz Wi-Fi and Bluetooth LE antennas. The internal transmission line from the SoC to this connector is impedance-matched to 50 Ω to ensure maximum power transfer and minimal signal reflection.

Mechanical Life and Maintenance:

The U.FL connector is a micro-miniature component with a rated mating lifetime of

approximately 30 cycles. Due to the fragile nature of the center contact, frequent disconnection is strongly discouraged. For production maintenance, the use of a specialized U.FL extraction tool is recommended to apply vertical force and prevent mechanical deformation of the outer ground ring.

5.14.2 High-Density B2B Expansion Connector

To facilitate the advanced sensing capabilities of the Sense and Plus variants, the mainboard incorporates a 30-pin Board-to-Board (B2B) interconnect utilizing the Hirose DF40C series. This high-reliability, low-profile system is engineered for stable signal transmission in compact AIoT devices.

Table 5-21. B2B Connector Mechanical Specifications

Parameter	Specification
Manufacturer / Series	Hirose DF40C
Total Pin Count	30-Pin
Current Rating	0.3 A per pin

The B2B interface is a precision-engineered component. To ensure a reliable electrical connection and prevent hardware damage, precise parallel alignment is required before applying pressure. Downward force should be applied evenly across the connector surface until a tactile "click" is felt, indicating that the locking mechanism is fully engaged. Developers must avoid mating the connector at an angle or by pressing on one side only; uneven force during assembly can cause permanent bending or shearing of the pin contacts, rendering the expansion interface unusable.

6. Electrical Characteristics

This chapter specifies the electrical operating limits, DC and AC characteristics, power consumption, and RF performance of the XIAO ESP32-S3 series. The "typical" values in the tables are representative measurements taken at an ambient temperature of 25°C with 5.0V USB power or 3.7V lithium-battery power. The operating ranges defined by "minimum" and "maximum" values are derived either from the Espressif ESP32-S3 SoC datasheet or from verification testing performed by Seeed Studio on EVT samples.

6.1 Absolute Maximum Ratings

Stresses applied to the device beyond the limits listed below may cause permanent damage. Prolonged operation under absolute maximum rating conditions may affect device reliability, and correct operation is not guaranteed under such conditions.

Table 6-1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
USB input voltage	V_{USB}	-0.3	+6.0	V	via Type-C port
Battery input voltage	V_{BAT}	-0.3	+4.5	V	via BAT± pads
GPIO input voltage	V_{IN}	-0.3	+3.6	V	not 5V-tolerant
Storage temperature	T_{STG}	-40	+125	°C	-
ESD (Human Body Model)	V_{ESD_HBM}	-	±2000	V	JEDEC JS-001
ESD (Charged Device Model)	V_{ESD_CDM}	-	±500	V	JEDEC JS-002

The BAT+ pad does not include reverse-polarity protection; applying a reverse voltage to this pad will permanently damage the on-board PMIC. The system designer must ensure correct polarity at the battery input.

6.2 Recommended Operating Conditions

Table 6-2 lists the recommended battery and environmental operating conditions. The 3.7 V battery value is nominal. Supply reference values and measured board results are listed separately in Table 4-2. Absolute maximum ratings are provided in Section 6.1.

The board accepts a nominal 5.0 V input through USB Type-C or the VBUS pin and a single-cell Li-ion or Li-Po battery through the BAT pads. The recommended battery range is 3.3 V to 4.2 V,

with a nominal voltage of 3.7 V. When USB and the battery are connected, the power-path circuit supplies the system from USB and the charger charges the battery. Measured 3.3 V output voltage is listed in Table 4-2.

Table 6-2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Battery input voltage	V_{BAT}	3.3	-	4.2	V
Operating temperature	T_A	-20	+25	+65	℃
Operating humidity (NC)	RH	10	-	90	%

6.3 DC Electrical Characteristics

6.3.1 GPIO Characteristics

The GPIO input threshold and output level specifications are taken from the Espressif ESP32-S3 SoC datasheet. The drive-capability data were measured on EVT samples of the XIAO ESP32-S3 and XIAO ESP32-S3 Plus using a KIKUSUI electronic load.

Table 6-3 GPIO DC Characteristics (V_{IO} = 3.3V, T_A = 25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	-	0.75 V_{IO}	-	V_{IO} + 0.3	V
Input low voltage	V_{IL}	-	-0.3	-	0.25 V_{IO}	V
Output high voltage	V_{OH}	I_{OH} = -8mA	2.64	-	-	V
Output low voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
GPIO sink/source current (Standard Version)	I_{IO}	3.3V rail droop ⩽ 5%	-	8	9	mA
GPIO sink/source current (Plus Version)	I_{IO}	3.3V rail droop ⩽ 5%	-	6	7	mA
GPIO max. source current	I_{IO_max}	V_{OH} ⩾ 2.64V	-	26	-	mA
Input leakage current	I_{LK}	V_{IN} = 0 or V_{IO}	-	-	±1	μA
Internal pull-up	R_{PU}	-	-	45	-	kΩ
Internal pull-down	R_{PD}	-	-	45	-	kΩ

The per-pin drive capability is constrained by the SoC electrical specification. In bench testing,

the 3.3V rail droops by less than 5% when a single pin sinks or sources approximately 9mA. If the output voltage is allowed to fall to the minimum VOH of 2.64V, the source current can reach approximately 26mA. Select GPIO drive strength and load current according to the required output voltage and the ESP32-S3 DC characteristics.

6.3.2 ADC Characteristics

Table 6-4 ADC Characteristics (V_{DD} = 3.3V, T_A = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Resolution	-	-	-	12	-	bit
Input voltage range	V_{IN}	0dB attenuation	0	-	0.95	V
Input voltage range	V_{IN}	2.5dB attenuation	0	-	1.25	V
Input voltage range	V_{IN}	6dB attenuation	0	-	1.75	V
Input voltage range	V_{IN}	11dB attenuation (default)	0	-	2.5	V
Absolute accuracy	-	0.1V ~ 3.0V input	-	±20	±50	mV

Absolute accuracy was measured on XIAO ESP32-S3 EVT samples using a calibrated bench multimeter as the reference, with test points at 0.1V, 0.2V, 0.5V, 1.0V, 2.0V, and 3.0V. The ±50mV figure represents the worst-case error across all test points on both samples. For high-precision analog acquisition, an external reference source or two-point calibration is recommended.

6.4 RF Characteristics

6.4.1 Wi-Fi Transmit Characteristics

Table 6-5 Wi-Fi Transmit Power (measured at the antenna port after spectrum-analyzer calibration)

Version	Protocol	Data Rate	Min.	Typ.	Unit
Standard	802.11b	1 Mbps	16.6	19.97	dBm
Plus	802.11b	1 Mbps	15	-	dBm

The operating frequency range is defined by the ESP32-S3 specification. The measured sample frequency offset is listed separately below.

- Frequency range: 2412 ~ 2484 MHz
- Measured frequency offset: 31.94 kHz

6.4.2 Wi-Fi Receive Characteristics

The receive sensitivities listed below are taken from the Espressif ESP32-S3 SoC datasheet. Field-measured line-of-sight communication range is provided in Section 6.4.4.

Table 6-6 Wi-Fi Receive Sensitivity

Protocol	Data Rate	Sensitivity	Unit
802.11b	1 Mbps	-98.4	dBm
802.11b	11 Mbps	-88.6	dBm
802.11g	6 Mbps	-93.2	dBm
802.11g	54 Mbps	-76.5	dBm
802.11n (HT20)	MCS0	-92.6	dBm
802.11n (HT20)	MCS7	-74.2	dBm

6.4.3 Bluetooth LE Characteristics

The ESP32-S3 supports Bluetooth 5.0 Low Energy, including the 2M PHY for higher throughput and the Coded PHY (S=2 and S=8) for extended range. The transmit-power figure listed below was measured at the U.FL connector of a Standard-version EVT sample using a calibrated spectrum analyzer; other parameters are taken from the Espressif ESP32-S3 SoC datasheet.

Table 6-7 Bluetooth LE RF Characteristics

Parameter	Value	Unit
Transmit power (default setting)	19.73	dBm
Frequency range	2402 ~ 2480	MHz
Supported PHYs	1M / 2M / Coded (125K, 500K)	—
Receive sensitivity (1M PHY)	-97.5 (typ.)	dBm

6.4.4 Communication Range

The following ranges were measured in an open, line-of-sight outdoor environment with a smartphone acting as the peer device and the DUT powered from a 5V USB power bank.

Table 6-8 Typical Communication Range

Link Type	Version	Typical Range	Remarks
Wi-Fi (AP mode)	Standard	⩾ 98m	line-of-sight
Wi-Fi (AP mode)	Plus	⩾ 100m	packet loss appears beyond 140 m
Bluetooth LE	Standard	⩾ 110m	Android phone, nRF Connect
Bluetooth LE	Plus	⩾ 140m	Android phone, nRF Connect

Communication range depends on antenna orientation, obstacles, multipath propagation, and peer-device sensitivity. Evaluate the range in the final installation environment.

6.4.5 Antenna Configuration

The XIAO ESP32-S3 series does not use a PCB trace antenna. The RF front end is routed through a 50Ω impedance-controlled transmission line to an on-board U.FL coaxial connector, with radiation provided by an external flexible FPC antenna. This FPC antenna is shipped with the module and must be attached to the U.FL connector before use; otherwise the module cannot transmit or receive RF signals correctly.

Table 6-9 Supplied FPC Antenna Specification

Parameter	Value
Connector type	U.FL / IPEX MHF1
Operating frequency	2400–2500 MHz
Characteristic impedance	50 Ω
VSWR	< 2:1
Polarization	linear
Cable length	80 mm

If the application imposes specific requirements on the radiation pattern or mechanical form factor, any antenna that meets the electrical specifications above and uses a U.FL / IPEX MHF1 interface may be substituted. The mechanical mating cycle rating of the U.FL connector is approximately 30 insertions, so frequent mating and unmating during production test or end-user operation should be avoided. Refer to Section 5.14.1 for additional guidance.

6.5 Thermal Characteristics

The thermal performance of the module is determined jointly by the power dissipation of the ESP32-S3 SoC, the ambient temperature, and the heat-dissipation design of the PCB and enclosure. The following data were collected on an EVT sample of the XIAO ESP32-S3 Sense running the ESP32 WebCamera firmware, streaming continuously over Wi-Fi at SVGA (800×600) resolution for more than one hour.

Table 6-10 Reference Steady-State Temperatures of the Tested Sense EVT Sample

Configuration	Rear Thermal-Pad Temperature
No heatsink	77.9°C
With adhesive-backed heatsink	53.5°C

Conditions: TA=25°C, USB Type-C 5V supply, OMEGA CL3515R thermocouple attached to the rear thermal pad.

During this test the module operated stably for more than one hour with no visible frame drops and no Wi-Fi disconnections, reaching its steady-state peak temperature within one hour. For applications that require sustained high-load operation (such as continuous video streaming, edge AI inference, or long-term operation at a 240MHz core clock), attaching a thermally conductive silicone pad or a small aluminum heatsink to the rear thermal pad is recommended. Test results show that this measure reduces the steady-state rear-pad temperature by approximately 24°C, improving operating reliability and duty-cycle capability in enclosed or poorly ventilated housings.

7. Mechanical Dimensions

This chapter provides the mechanical dimensions and PCB footprint information for the XIAO ESP32-S3 Series. The XIAO ESP32-S3, XIAO ESP32-S3 Sense, and XIAO ESP32-S3 Plus share the same main board outline. The Sense version includes an expansion board that mates with the B2B connector on the top side of the main board.

All dimensions are given in millimeters unless otherwise specified.

7.1 Outline Dimensions

The main board measures 21.0mm × 17.8mm and has a nominal height of 5.0mm for all three versions. The XIAO ESP32-S3 Sense assembly has a nominal total height of 15.0mm with its expansion board and camera installed. These heights exclude pin headers, external cables, and optional heatsinks. Figure 7-1 shows the main-board outlines and overall height envelopes.

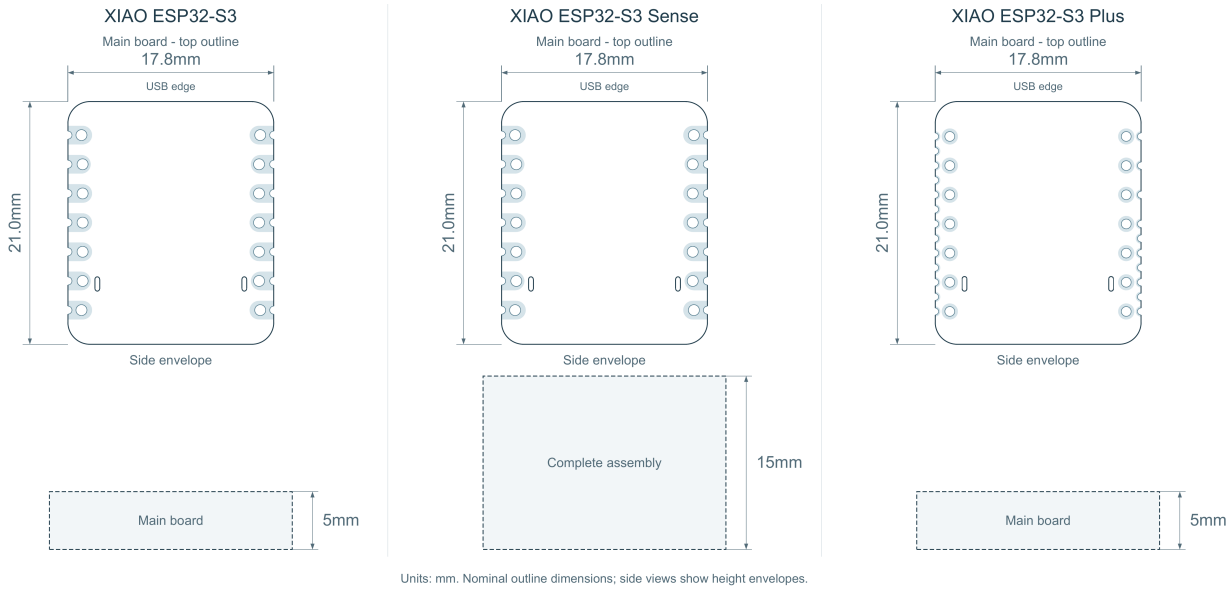


Figure 7-1. XIAO ESP32-S3 Series Outline Dimensions

Table 7-1. Mechanical Dimension Comparison

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus	Unit
Main board length	21.0	21.0	21.0	mm
Main board width	17.8	17.8	17.8	mm
Main board height	5.0	5.0	5.0	mm

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus	Unit
Total height	5.0	15.0	5.0	mm
Weight without antenna	2.17	4.00	2.17	g
Weight with antenna	2.64	4.47	2.64	g

7.2 Mechanical Specifications

The following table defines the principal mechanical parameters used for enclosure design, carrier board design, and assembly process evaluation.

Table 7-2. Mechanical Specifications

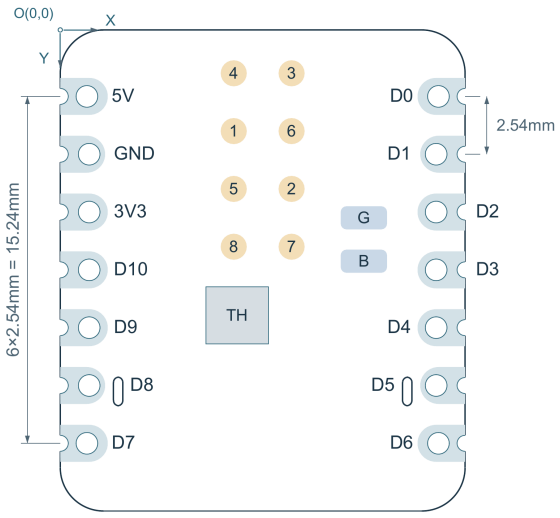
Parameter	Symbol	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus	Tolerance	Unit
Main board length	L	21.0	21.0	21.0	±0.10	mm
Main board width	W	17.8	17.8	17.8	±0.10	mm
Main board height	H1	5.0	5.0	5.0	±0.20	mm
Total height with expansion board	H2	-	15.0	-	±0.30	mm
Expansion board length (without camera)	L_EXT	-	15.3	-	±0.10	mm
Expansion board width	W_EXT	-	17.8	-	±0.10	mm

7.3 Pin Pitch and Pad Dimensions

The standard edge pads have a 2.54mm pitch. The Plus version adds extended castellated pads between the standard positions. Where an extended pad is present, the center spacing along the board length between that pad and the adjacent standard pad is 1.27mm. The additional Plus pads require the dedicated Plus carrier-board footprint.

A. XIAO ESP32-S3 (Standard / Sense main board)

PCB file: V1.5; official Standard / Sense project packages
Bottom view (mirrored); USB edge at top



Header drill: Ø0.95mm; castellation drill: Ø0.70mm
Hole-row spacing: inner 5 rows 15.24mm; end rows 15.44mm

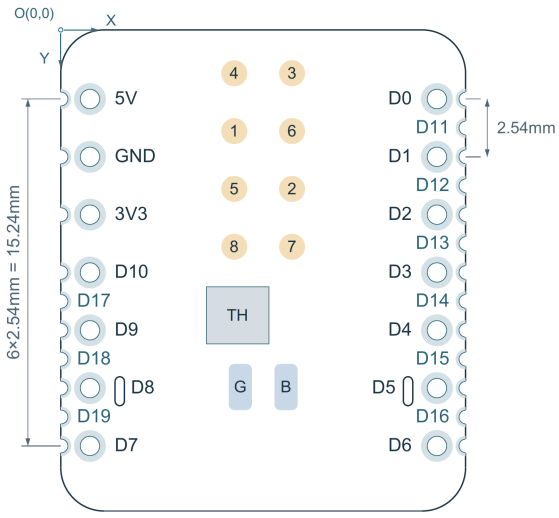
Bottom pad coordinates (mm)

Pad	X	Y	Pad geometry
BAT+ (B)	13.335	10.160	2.032×1.016
GND (G)	13.335	8.255	2.032×1.016
TH	7.770	12.540	2.750×2.500
TP1	7.620	4.445	Ø1.143
TP2	10.160	6.985	Ø1.143
TP3	10.160	1.905	Ø1.143
TP4	7.620	1.905	Ø1.143
TP5	7.620	6.985	Ø1.143
TP6	10.160	4.445	Ø1.143
TP7	10.160	9.525	Ø1.143
TP8	7.620	9.525	Ø1.143

Source: XIAO ESP32S3_V1.5.kicad_pcb

B. XIAO ESP32-S3 Plus - V1.1

PCB file: V1.1
Bottom view (mirrored); USB edge at top



Header drill: Ø0.85mm; castellation drill: Ø0.60mm
Header-row spacing: 15.24mm; staggered edge pitch: 1.27mm

Bottom pad coordinates (mm)

Pad	X	Y	Pad geometry
BAT+ (B)	9.894	15.688	1.016×2.032
GND (G)	7.888	15.688	1.016×2.032
TH	7.770	12.540	2.750×2.500
TP1	7.620	4.445	Ø1.143
TP2	10.160	6.985	Ø1.143
TP3	10.160	1.905	Ø1.143
TP4	7.620	1.905	Ø1.143
TP5	7.620	6.985	Ø1.143
TP6	10.160	4.445	Ø1.143
TP7	10.160	9.525	Ø1.143
TP8	7.620	9.525	Ø1.143

Source: XIAO ESP32S3 Plus_V1.1_250724.kicad_pcb

Units: mm. Origin: upper-left corner of the CAD outline bounding box; X increases to the right and Y downward.
B = BAT+; G = BAT-/GND; TH = thermal-pad mask opening. Rectangles: W×H; circles: diameter.
Nominal CAD pad geometry. A: identical PCB data in the official Standard and Sense project packages.

Figure 7-2. Edge Pad and Bottom Pad Dimensions

Table 7-3. Pin and Pad Dimensions

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus	Tolerance	Unit
Standard edge pad pitch	2.54	2.54	2.54	±0.05	mm
Plus inner castellated pad pitch	-	-	1.27	±0.05	mm
Standard castellated pad size	2.15 x 1.75	2.15 x 1.75	1.95 x 1.40	±0.05	mm
Plus inner castellated pad size	-	-	0.68 x 0.90	±0.05	mm

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus	Tolerance	Unit
Standard castellated half-hole diameter	Φ0.70	Φ0.70	Φ0.60	±0.05	mm
Header through-hole diameter	Φ0.95	Φ0.95	Φ0.85	-	mm
Header-hole row spacing	15.24 / 15.44[14]	15.24 / 15.44[14]	15.24	±0.10	mm
Distance between standard pad rows	15.20	15.20	15.20	±0.10	mm
Bottom test pad size	Φ1.14	Φ1.14	Φ1.14	±0.10	mm
BAT pad size	2.03 x 1.01	2.03 x 1.01	2.03 x 1.01	±0.10	mm

[14] *Note: Standard/Sense: 15.24mm at the inner five rows; 15.44mm at the two end rows. These CAD references use the published Standard/Sense V1.5 PCB file and Plus V1.1 PCB file.*

Table 7-3 summarizes nominal module-pad dimensions and PCB reference geometry. The official, version-specific footprint defines the carrier-board copper geometry used for assembly.

Standard edge pad pitch is the center-to-center spacing along the board length between adjacent standard pads, such as D0 and D1. It is 2.54mm for all versions.

Plus staggered edge pad pitch is the center spacing along the board length between an extended pad and the adjacent standard pad. It is 1.27mm where an extended pad is present. Successive extended-pad positions on the same edge are spaced at 2.54mm.

The nominal standard castellated pad sizes are 2.15mm×1.75mm for the Standard and Sense versions and 1.95mm×1.40mm for Plus. The nominal Plus extended pad size is 0.68mm×0.90mm. The copper geometry may consist of multiple shapes; use the corresponding official carrier-board footprint for the complete land pattern.

Castellated half-hole diameter refers to the hole intersected by the board edge. Header through-hole diameter refers to the separate complete hole used for a pin header. Header-hole row spacing is measured across the board between the centers of the complete header holes.

The bottom test pads have a nominal diameter of 1.14mm. BAT pad size is 2.032mm×1.016mm, specified as long side × short side. Pad positions and orientation are version dependent; use Figure 7-2 and Table 7-9 for the battery-pad references.

7.4 Recommended PCB Footprint

The XIAO ESP32-S3 Series supports pin-header mounting and SMD mounting through its castellated pads. For SMD carrier-board design, use XIAO-ESP32-S3-SMD for the Standard and Sense versions and XIAO-ESP32-S3-Plus-SMD for the Plus version from the official Seeed XIAO KiCad footprint library.

Table 7-4 lists carrier-board pad dimensions, while Figure 7-2 shows the module-side pad layout. Use the complete version-specific land pattern, including pad positions, rotations, and solder-mask openings.

Table 7-4. Recommended PCB Footprint Parameters

Parameter	Applicable Version	Recommended Value	Unit
Standard edge pad pitch	All versions	2.54	mm
Carrier pad size for standard castellated positions	Standard / Sense	2.75 x 2.00	mm
Carrier pad size for standard castellated positions	Plus	2.032 x 0.95	mm
Carrier pad size for Plus extended castellated positions	Plus	1.232 x 0.95	mm
Carrier pad size for bottom test pads	All versions	∅1.70	mm
Carrier pad size for BAT pads	All versions	2.50 x 1.10	mm
Carrier pad size for thermal pad	Standard / Sense	2.75 x 2.50	mm
Carrier pad size for thermal pad	Plus	2.80 x 2.50	mm
Stencil thickness	All versions	0.12 to 0.15	mm

The values in Table 7-4 specify copper lands on the carrier board. Standard and Sense SMD lands differ from the narrower lands used at the standard positions of the Plus footprint.

Include the Plus extended-pad lands when the additional GPIO connections are required. Connect bottom test and BAT lands according to the intended signals and board version. Preserve electrical isolation from other exposed module metal.

Use a 0.12mm to 0.15mm stencil as the reference range. Adjust aperture geometry and assembly settings for the solder paste, reflow profile, and assembly process.

7.5 Component Location and Mechanical Clearance

This section defines the mechanical clearance requirements for the main components that may affect enclosure design, carrier-board layout, and product assembly. These dimensions include the USB Type-C connector, BOOT and RESET buttons, FPC antenna, U.FL connector, bottom-side exposed pads, and battery pads.

The dimensions in this section are intended for mechanical integration. Electrical layout, RF keep-out, EMC protection, grounding, and thermal design recommendations are described in Chapter 8.

7.5.1 USB Type-C Connector Clearance

The USB Type-C connector is mounted at one end of the main board and extends beyond the PCB outline. When the module is installed in an enclosure, the opening shall provide sufficient clearance for the connector shell and the USB cable plug. The enclosure design shall also reserve insertion space in front of the connector to allow normal cable mating and removal.

Table 7-5. USB Type-C Connector Mechanical Parameters

Parameter	Symbol	Value	Tolerance	Unit
USB-C connector protrusion from board edge	L_USB	1.80	±0.10	mm
USB-C connector body width	W_USB_BODY	8.98	±0.10	mm
USB-C connector body length	L_USB_BODY	7.30	±0.10	mm
Recommended enclosure opening width	W_USB_OPEN	11.00	-	mm
Recommended enclosure opening height	H_USB_OPEN	8.00	-	mm
Recommended plug insertion clearance	L_USB_CLR	15.00	-	mm

The USB-C connector protrusion is measured from the main board edge to the outermost front edge of the connector shell. The enclosure opening dimensions shall be larger than the connector shell dimensions to account for enclosure tolerance, connector placement tolerance, and USB cable plug variation.

The 8.98mm body dimension is transverse to the USB mating direction, parallel to the PCB width. The 7.30mm body dimension is along the USB mating direction. The recommended enclosure opening is 11.00mm wide and 8.00mm high, with 15.00mm reserved in front of the

connector for plug insertion.

7.5.2 BOOT and RESET Button Position

The BOOT and RESET buttons are located on the top side of the main board. If the module is assembled inside an enclosure and manual access is required, the enclosure shall provide access holes or mechanical actuators aligned with the button center positions.

Coordinates in Table 7-6 are measured in the main-board top view with the USB edge at the top. The origin is the upper-left corner of the CAD outline bounding box; X increases to the right and Y increases downward. The coordinates refer to the centers of the button bodies. K2 is BOOT and K1 is RESET.

Table 7-6. BOOT and RESET Button Mechanical Parameters

Parameter	BOOT Button	RESET Button	Tolerance	Unit
Button center X position	14.732	3.048	±0.10	mm
Button center Y position	1.651	1.651	±0.10	mm
Button body length	1.60	1.60	±0.10	mm
Button body width	2.60	2.60	±0.10	mm
Recommended button access diameter	Ø3.50	Ø3.50	-	mm

The button access opening shall provide sufficient clearance for the button travel direction. The enclosure or actuator shall not continuously press the button after assembly.

7.5.3 FPC Antenna and U.FL Connector Location

The XIAO ESP32-S3 Series uses an external 2.4GHz FPC antenna connected through the on-board U.FL connector. Table 7-7 specifies the A-02 antenna assembly with an 80mm cable. U.FL placement coordinates refer to the ANT1 footprint origin in the main-board top view with the USB edge at the top. The origin is the upper-left corner of the CAD outline bounding box; X increases to the right and Y increases downward.

Table 7-7. FPC Antenna and U.FL Mechanical Parameters

Parameter	Symbol	Value	Tolerance	Unit
FPC antenna length[15]	L_ANT	37.40	±0.20	mm
FPC antenna width[15]	W_ANT	17.50	±0.20	mm

Parameter	Symbol	Value	Tolerance	Unit
Antenna cable length	L_CABLE	80.00	±0.10	mm
U.FL footprint origin X position	X_UFL	4.039	±0.10	mm
U.FL footprint origin Y position	Y_UFL	19.406	±0.10	mm
Recommended cable bending clearance	R_CABLE	5.00	-	mm

[15]*Note: The FPC antenna length and width refer to the antenna body only and do not include the coaxial cable.*

The FPC antenna shall not be mechanically pressed by the enclosure, battery, display, or other internal components. Sufficient clearance shall be reserved around the U.FL connector and cable bending area to avoid mechanical stress on the RF connector.

7.5.4 Bottom-Side Pad Clearance

The bottom side of the main board has no mounted components in the PCB reference designs covered here. It contains exposed test pads, battery pads, a thermal-pad opening, and connector anchoring or soldered metal features. Provide electrical insulation from nearby conductive surfaces.

Where bottom-side lands are intentionally connected to a carrier board, use the version-specific pad layout and carrier-board footprint in Sections 7.3 and 7.4. Maintain isolation from all other exposed module metal, including connector anchor joints and edge-pad metallization.

Table 7-8. Bottom-Side Clearance Parameters

Parameter	Symbol	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus	Tolerance	Unit
Bottom exposed pad keep-out length	L_BOT_KO	13.21	13.21	16.00	±0.10	mm
Bottom exposed pad keep-out width	W_BOT_KO	8.24	8.24	5.00	±0.10	mm
Exposed thermal-pad mask opening length (Y)	L_TH	2.50	2.50	2.50	±0.10	mm
Exposed thermal-pad mask opening width (X)	W_TH	2.75	2.75	2.75	±0.10	mm

The bottom exposed-pad keep-out dimensions are reference rectangles positioned to enclose

the test pads, battery pads, and thermal-pad opening shown in Figure 7-2. L_TH and W_TH specify the exposed thermal-pad solder-mask opening along the Y and X axes, respectively. Provide insulation from conductive carrier-board or enclosure features throughout the affected area.

Set the bottom-side clearance for the solder-joint height, mounting method, assembly tolerances, and mechanical loading. Non-conductive surfaces may approach the exposed-pad areas when electrical insulation, thermal requirements, and mechanical stress are accommodated.

The ESP32-S3 may generate heat during sustained high-load operation. A thermally conductive interface or heatsink may be coupled to the bottom-side thermal pad, with electrical isolation from surrounding exposed conductors where required. Reserve clearance for the selected thermal solution. Seeed offers an optional 10mm×10mm heatsink accessory.

7.5.5 Battery Pad Location Difference

The BAT+ and BAT-/GND pads are located on the bottom side of the main board. The copper pad size is 2.032mm×1.016mm, specified as long side × short side. The Plus pads are rotated by 90° and have different positions from the Standard and Sense reference design.

Coordinates in Table 7-9 use the mirrored bottom view in Figure 7-2 with the USB edge at the top. The origin is the upper-left corner of the CAD outline bounding box; X increases to the right and Y increases downward. BAT+ is the VBAT net and BAT- is GND.

Table 7-9. Battery Pad Location Parameters

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus	Tolerance	Unit
BAT+ pad center X position	13.335	13.335	9.894	±0.10	mm
BAT+ pad center Y position	10.160	10.160	15.688	±0.10	mm
BAT- pad center X position	13.335	13.335	7.888	±0.10	mm
BAT- pad center Y position	8.255	8.255	15.688	±0.10	mm
BAT pad copper size (long side x short side)	2.032 × 1.016	2.032 × 1.016	2.032 × 1.016	±0.10	mm

For carrier boards designed to support multiple XIAO ESP32-S3 variants, the BAT pad alignment shall be checked separately for the XIAO ESP32-S3 Plus. A shared battery pad footprint shall only be used when the pad overlap and soldering reliability are verified for all intended versions.

7.6 Sense Version Mechanical Dimensions

The XIAO ESP32-S3 Sense consists of the main board and the Sense expansion board. The expansion board contains the camera connector, microphone, and MicroSD card slot. Mechanical integration shall reserve clearance for the camera module, lens, camera FPC, MicroSD card insertion direction, microphone acoustic port, and antenna cable routing.

Table 7-10. XIAO ESP32-S3 Sense Specific Dimensions

Parameter	Symbol	Value	Tolerance	Unit
Total assembly height	H2	15.0	±0.30	mm
Expansion board length (without camera)	L_EXT	15.30	±0.10	mm
Expansion board width	W_EXT	17.80	±0.10	mm
Fully inserted MicroSD card protrusion[16]	L_SD_PROTRUSION	9.53	±0.30	mm

The nominal overall assembly height is shown in Figure 7-1. Table 7-10 lists the expansion-board dimensions and the protrusion of a fully inserted MicroSD card.

[16] *Note: L_SD_PROTRUSION is measured from the outer edge of the Sense expansion board to the exposed end of a fully inserted MicroSD card. Reserve additional space for card insertion, removal, and finger access.*

7.7 Plus Version Mechanical Dimensions

The XIAO ESP32-S3 Plus has the same nominal main-board outline as the Standard version and adds extended castellated pads between the standard edge-pad positions. Figure 7-2 shows the Plus pad layout. Where an extended pad is present, its center is offset by 1.27mm along the board length from the adjacent standard pad. Use the dedicated Plus carrier-board footprint when these additional GPIO connections are required.

Table 7-11. XIAO ESP32-S3 Plus Specific Dimensions

Parameter	Value	Tolerance	Unit
Main board length	21.0	±0.10	mm
Main board width	17.8	±0.10	mm
Main board height	5.0	±0.20	mm
Nominal Plus extended castellated pad size	0.68 x 0.90	±0.05	mm

Parameter	Value	Tolerance	Unit
Plus staggered edge pad pitch	1.27	±0.05	mm

8. Hardware Design Guidelines

This chapter provides hardware design recommendations for integrating the XIAO ESP32-S3 Series into user systems. The guidelines cover schematic design, PCB layout, EMC considerations, and thermal design. They are intended to support reliable carrier-board development, product integration, and volume production.

The XIAO ESP32-S3 Series is a compact wireless microcontroller development board. When it is used as a module on a carrier board, the user design shall consider power integrity, signal compatibility, RF performance, thermal dissipation, and mechanical clearance at the system level.

8.1 Schematic Design Recommendations

The schematic design shall ensure that all external circuits connected to the XIAO ESP32-S3 Series remain within the electrical limits of the board. Special attention shall be given to power input, GPIO voltage levels, battery connection, and high-speed or noise-sensitive interfaces.

8.1.1 Power Design

The XIAO ESP32-S3 Series supports power input through USB Type-C, the VBUS pin, or the BAT pads. The 3V3 pin is a regulated output from the on-board DC-DC converter and shall not be used as an external power input.

When powering the board through the VBUS pin, the external supply shall comply with the VBUS input voltage range in Table 6-2 and connect through a series Schottky diode (see Section 4.3.1). The power path shall provide sufficient current capability for the XIAO board, connected peripherals, RF transmission peaks, and battery charging when applicable. Long power traces or cables may cause voltage drop during RF transmission peaks; therefore, the carrier-board power path should be kept short and low impedance.

When using the BAT pads, only a single-cell Li-ion or Li-Po battery shall be connected. Battery polarity shall be verified before connection, as reverse battery connection may damage the charging and power management circuitry. If the product requires a removable battery connector, the connector pinout and mechanical keying should be designed to prevent reverse insertion.

For peripherals powered from the 3V3 pin, calculate the available external current from the supply-specific total load capability in Table 4-2 after subtracting the current used by the main

board and attached peripherals. Use a separate regulated supply for loads that exceed the available budget.

For battery-powered products, the carrier board should avoid leakage paths on GPIOs, pull-up resistors, level shifters, sensors, and external modules when the system is in sleep mode. External circuits connected to wake-up pins shall be designed so that they do not dominate the deep-sleep current.

8.1.2 GPIO Design

All GPIO signals on the XIAO ESP32-S3 Series use 3.3 V logic. External circuits connected to GPIO pins shall not drive signals above 3.3 V. If the external device uses 5 V logic, a level shifter or other voltage-limiting circuit shall be used.

GPIOs used during boot, reset, USB communication, LED control, JTAG, camera, microphone, MicroSD card, or other internal functions shall be checked against the pin assignment and conflict descriptions in Chapter 3. Some GPIOs have version-specific mappings, especially the extended pins on the XIAO ESP32-S3 Sense and XIAO ESP32-S3 Plus. Firmware intended to support multiple versions should use native GPIO numbers instead of relying only on Arduino-style Dx naming.

GPIO0 is connected to the BOOT function. External circuits connected to GPIO0 shall not force an unintended boot mode during reset. GPIO19 carries USB D- and GPIO20 carries USB D+. Reserve these pins for native USB communication when that interface is used. GPIO39-42 are shared with external four-wire JTAG. For debugging while these pins serve other peripherals, use the USB Serial/JTAG interface described in Section 5.12.

When using GPIO10 (D16) to measure battery voltage, provide an external resistor divider and keep the divided voltage within the configured ADC range. Reserve this pin for the measurement circuit while battery monitoring is enabled.

For input signals routed off-board, series resistors, pull-up or pull-down resistors, and ESD protection may be added according to the system environment. For output signals driving cables, LEDs, relays, or external modules, the GPIO drive strength and current limit shall be considered. Inductive loads shall not be driven directly from GPIO pins.

8.1.3 Communication Interface Design

The default communication interfaces of the XIAO ESP32-S3 Series include UART, I2C, SPI, USB, and version-specific interfaces such as camera, microphone, MicroSD, and additional Plus extended GPIO functions. Although the ESP32-S3 GPIO matrix allows flexible signal routing,

the default pin assignments should be followed where possible to maintain compatibility with existing software examples and board support packages.

For I2C interfaces, external pull-up resistors shall be selected according to the bus voltage, bus speed, and total bus capacitance. If multiple I2C modules already contain pull-up resistors, the equivalent pull-up resistance shall be checked to avoid excessive bus current or distorted signal edges.

For SPI interfaces, the SCK, MOSI, and MISO traces should be routed with short trace length and a continuous ground reference. If multiple SPI devices share the same bus, each device shall have an independent chip select signal.

On the Sense expansion board, the MicroSD card shares the standard SPI bus lines with D8/SCK, D9/MISO, and D10/MOSI. The MicroSD chip-select signal is configured by the on-board 0 **Ω** resistor option. In the default configuration, SD_CS is routed to IO21/USER_LED. If the chip-select signal is remapped to D2/GPIO3, the corresponding resistor configuration shall be changed. When using the MicroSD card and the user LED or additional SPI devices in the same design, the chip-select assignment shall be checked against the actual hardware configuration.

For UART interfaces, TX and RX shall be crossed correctly between the XIAO board and the external device. If the external device uses a different voltage domain, level shifting shall be used. Long UART cables should include ESD protection and, where necessary, additional filtering or differential communication should be considered.

For USB, the on-board USB Type-C connector includes the required CC pull-down resistors for sink-device operation and series resistors on the USB data lines. When the on-board USB Type-C connector is used, no additional USB front-end circuitry is required on the carrier board.

If the USB D+ and D− signals are routed from the module to an external connector on the carrier board, the traces should be routed as a short, closely coupled differential pair with minimal stubs. ESD protection should be placed close to the external connector. Additional series resistance should be evaluated carefully to avoid over-damping the signal, as series resistors are already present on the module USB path.

8.2 PCB Layout Guidelines

The carrier-board layout shall provide stable power delivery, reliable signal routing, and sufficient RF and thermal clearance. The compact size of the XIAO ESP32-S3 Series makes layout density high, so special attention shall be given to antenna placement, ground continuity, connector clearance, and exposed bottom pads.

8.2.1 General Layout Rules

Place the XIAO module so that the USB Type-C connector, BOOT and RESET buttons, antenna cable, and any required bottom-side pads remain accessible according to the mechanical dimensions in Chapter 7. Avoid placing tall components near the USB connector, U.FL connector, antenna cable path, buttons, and Sense camera or MicroSD card clearance area.

The carrier board should provide a continuous ground reference for signal routing and power return. In the area below the XIAO module, any copper plane, vias, or metal features shall be covered by solder mask or insulated from the bottom-side exposed pads of the module. Direct contact between the carrier board copper and the bottom-side test pads, battery pads, or thermal pads shall be avoided unless it is intentionally designed as part of the carrier-board footprint.

High-speed or noise-sensitive signals should be routed over continuous ground and should avoid crossing splits in the ground plane. Power traces shall be sized according to the expected load current and should be kept short between the power source, XIAO module, and external peripherals.

Decoupling capacitors for external devices shall be placed close to the load. If the carrier board includes sensors, displays, audio devices, relays, motors, or wireless modules, their supply domains should be reviewed to prevent noise coupling into the XIAO power rail.

8.2.2 Antenna Area Design

The XIAO ESP32-S3 Series uses an external 2.4 GHz FPC antenna connected through the on-board U.FL connector. The antenna placement has a direct effect on Wi-Fi and Bluetooth performance. The FPC antenna shall be placed away from metal structures, batteries, displays, motors, large copper areas, and conductive enclosure parts.

The antenna should be positioned near the product enclosure edge or in a non-metallic region with clear space around the radiating area. The coaxial cable shall not be sharply bent, pinched, or placed under mechanical stress. The cable bending clearance (R_CABLE) in Table 7-7 shall be followed during enclosure and assembly design.

The carrier board should avoid routing high-speed digital signals, switching power traces, or high-current traces near the antenna cable and U.FL connector. If the product enclosure contains metal, the antenna location shall be verified through RF testing in the final assembled product.

8.2.3 Power Layout

Power traces from VBUS, battery input, or external regulators shall be routed with low impedance. The current path for high-current external peripherals shall not pass through narrow signal traces or shared return paths that may disturb the XIAO power rail.

If the carrier board supplies power to external loads, the power distribution network should separate noisy loads from sensitive circuits where possible. Switching regulators, motors, relays, and LED drivers should be placed away from the antenna, crystal-sensitive areas, analog inputs, and camera or microphone signals.

Ground return paths shall be short and continuous. For systems with both digital and analog circuits, the analog measurement path should be routed away from switching power nodes and high-current loops. Battery measurement circuits should use appropriate resistor values to reduce leakage current while maintaining ADC measurement accuracy.

8.3 EMC Design Recommendations

The XIAO ESP32-S3 Series is intended for integration into user systems, and the final EMC performance depends on the complete product design. The carrier board, enclosure, cables, power supply, and connected peripherals all affect electromagnetic compatibility.

8.3.1 Filtering Design

For interfaces exposed through the carrier board or external cables, ESD protection and filtering should be added where appropriate. This is especially important for external USB connectors, UART connectors, GPIO headers, sensor cables, button lines, and external power inputs.

For power inputs, input capacitance and filtering should be placed close to the entry point or connector. If the product is powered from long cables, transient protection may be required. For noisy external loads, additional filtering or separate regulation may be used to prevent conducted noise from entering the XIAO power rail.

For communication lines, series resistors may be used to slow excessive signal edges and reduce ringing, especially on SPI clock lines or long GPIO traces. Filter components shall be selected so that they do not violate the timing or signal integrity requirements of the interface.

8.3.2 Grounding Design

A continuous ground reference is important for signal integrity, RF performance, and EMC behavior. The carrier board should provide a low-impedance ground plane for signal return and power return, while avoiding unintended electrical contact with exposed bottom pads.

Ground connections for USB shielding, ESD devices, power return, and external connectors should be routed to a stable ground reference. ESD protection devices shall have a short and direct path to ground to reduce discharge impedance. Long, narrow, or fragmented ground paths reduce the effectiveness of ESD and EMC protection.

For designs with metal enclosures, the relationship between signal ground, chassis ground, and shield connection shall be defined at the system level. Direct contact between the XIAO bottom-side exposed pads and the enclosure shall be avoided unless it is intentionally designed and verified.

8.4 Thermal Design

Thermal behavior depends on operating mode, RF activity, CPU load, enclosure design, ambient temperature, and external heat sources. The ESP32-S3 SoC may generate noticeable heat during high-load operation, especially when Wi-Fi transmission, camera processing, continuous computation, or high peripheral activity is enabled.

8.4.1 Power Consumption and Temperature Rise

Temperature rise is related to average power consumption and heat dissipation conditions. Operation in open air generally allows better heat dissipation than operation inside a sealed enclosure. Continuous Wi-Fi transmission, high CPU frequency, camera streaming, and frequent flash or MicroSD activity may increase the board temperature.

When the XIAO ESP32-S3 Sense is used with the camera, microphone, and MicroSD card, the total system power consumption may be higher than the main board alone. Enclosure design shall account for the additional heat generated by the expansion board and nearby components.

If the product operates at elevated ambient temperature or in a sealed enclosure, the thermal performance shall be evaluated under the maximum expected workload. The final product shall ensure that component temperature remains within the specified operating limits.

8.4.2 Heat Dissipation Recommendations

For applications requiring sustained high-performance operation, sufficient air space should be reserved around the ESP32-S3 package. Avoid placing insulating foam, plastic ribs, batteries, displays, or other heat-sensitive components directly above the SoC unless thermal performance has been verified.

A heatsink may be used when additional thermal dissipation is required. Seeed provides an optional 10mm×10mm heatsink accessory for the bottom-side thermal pad. Reserve sufficient bottom-side clearance for the heatsink and its thermal interface, with electrical isolation from surrounding exposed conductors where required.

For carrier-board designs, thermal pads or copper areas may be used to improve heat spreading where mechanically and electrically appropriate. Thermal enhancement structures shall not create unintended electrical contact with the bottom-side exposed pads. In sealed or high-temperature products, thermal validation shall be performed using the final enclosure and actual application workload.

9. Packaging, Storage and Production

This chapter describes the packaging contents, storage conditions, soldering recommendations, and production handling guidelines for the XIAO ESP32-S3 Series. The information is intended for product inspection, warehouse storage, manual assembly, carrier-board mounting, and production process evaluation.

9.1 Packaging Specifications

The XIAO ESP32-S3 Series is shipped with different accessory configurations depending on the product version. The package contents shall be checked against the product label and order SKU before production use.

9.1.1 Standard Package Contents

Table 9-1 lists the single-unit retail package contents for Un-Soldered SKUs 113991114, 113991115, and 102010671. Package contents for Pre-Soldered, multi-unit, and tape-and-reel SKUs are listed in Table 2-1.

Table 9-1. Single-Unit Retail Package Contents (Un-Soldered SKUs)

Item	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
Main board	1 pc	1 pc	1 pc
Plug-in Expansion Board	-	1 pc	-
Aluminum heatsink for XIAO	-	2 pcs	-
7-pin header	2 pcs	2 pcs	2 pcs
FPC antenna	1 pc	1 pc	1 pc

The Sense kit includes the expansion board and heatsinks listed in the table. For each delivery, match the package contents to the ordered SKU in Table 2-1.

9.1.2 Packaging Dimensions

The packaging dimensions depend on the SKU, regional warehouse configuration, and packaging option. For single-unit retail packaging, the package includes the board and its standard accessories. For tape-and-reel packaging, the mechanical packing format shall follow the corresponding production packaging specification.

For cylindrical retail packages, the package dimension is expressed as diameter × height.

Table 9-2. Packaging Dimensions

Packaging Type	Applicable Version	Package Dimensions	Quantity per Package	Unit
Retail package	XIAO ESP32-S3	Ø42.18 × 24.86	1	mm
Retail package	XIAO ESP32-S3 Sense	Ø42.4 × 35.26	1	mm
Retail package	XIAO ESP32-S3 Plus	Ø42.18 × 24.86	1	mm

Table 9-3. Tape-and-Reel Packaging Parameters

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Plus	Unit
Tape width	44.00	44.00	mm
Pocket pitch	24.00	24.00	mm
Pocket length	18.68	18.68	mm
Pocket width	21.96	21.96	mm
Pocket depth	5.00	5.00	mm
Feed hole pitch	4.00	4.00	mm
Maximum quantity per reel	800	800	pcs
Supplied accessories	Not included	Not included	-

Tape-and-reel packaging is available for selected SKUs. The tape-and-reel package contains the XIAO module only and does not include the FPC antenna or 7-pin headers. The supplied tape length depends on the ordered quantity. Therefore, the package dimension is defined by the carrier tape parameters rather than the final cut length or shipping carton size.

9.2 Storage Conditions

The XIAO ESP32-S3 Series shall be stored in a clean, dry, and temperature-controlled environment. The product contains ESD-sensitive semiconductor devices and exposed metal pads, so moisture, dust, electrostatic discharge, and mechanical stress shall be controlled during storage and handling.

9.2.1 Recommended Storage Conditions

Table 9-4 defines the recommended storage conditions for unopened products.

Table 9-4. Recommended Storage Conditions

Parameter	Recommended Condition
Storage temperature	10 ˚C to 30 ˚C
Relative humidity	30% RH to 60% RH
Storage environment	Clean, dry, non-corrosive atmosphere
ESD handling	ESD-protected area and packaging
Mechanical stress	Avoid compression, bending, or impact

Products should be kept in the original packaging before use. Do not store the boards in environments with corrosive gas, high humidity, direct sunlight, or large temperature cycling. When handling unpacked boards, operators shall use proper ESD protection.

9.2.2 Handling After Opening

After opening the package, the board shall be handled by the PCB edge where possible. Direct contact with the RF connector, USB connector contacts, castellated pads, bottom-side pads, camera connector, and other exposed metal areas should be avoided.

If the board is used for SMT assembly or long-term storage after opening, the production team shall evaluate the moisture exposure time and storage condition according to the assembly process requirements. Boards that have been exposed to high humidity or long storage time shall be inspected before soldering.

9.2.3 Baking Conditions

If moisture exposure exceeds the process control limit, or if the boards show signs of moisture risk before reflow soldering, baking shall be performed according to the internal production process or the requirements of the assembly factory.

Table 9-5. Baking Conditions

Condition	Recommendation
Baking trigger	Long exposure after opening, high humidity exposure, or process requirement
Baking temperature	Follow assembly factory process
Baking duration	Follow assembly factory process
Packaging removal	Remove moisture-sensitive or heat-sensitive packaging before baking
Post-baking handling	Use within the allowed process window after baking

The board contains connectors, buttons, antenna connector, plastic parts, and other

temperature-sensitive materials. Baking temperature and duration shall be selected to avoid mechanical deformation, connector damage, label damage, or accessory degradation.

9.3 Production Soldering

The XIAO ESP32-S3 Series supports manual soldering and carrier-board surface-mount assembly depending on the selected integration method. The soldering process shall be selected according to the mechanical design, footprint design, and production volume.

9.3.1 Manual Soldering

Manual soldering is suitable for pin headers, wires, battery pads, and prototype assembly. The soldering iron temperature and contact time shall be controlled to avoid pad lifting, connector deformation, or thermal damage to nearby components.

For castellated edge pads, solder shall fully wet both the carrier-board pad and the castellated pad. Excessive solder volume may cause bridging between adjacent pads, especially on the XIAO ESP32-S3 Plus inner castellated pads. Flux residue shall be cleaned according to the production process when required.

When soldering the BAT+ and BAT- pads manually, polarity shall be checked before connection. Reverse battery connection may permanently damage the power management circuitry.

9.3.2 Reflow Soldering

For carrier-board integration using the castellated pads or bottom-side pads, the XIAO module may be mounted by reflow soldering when the footprint, stencil, solder paste, and temperature profile are properly validated.

The reflow process shall be compatible with the assembled XIAO module, including the USB Type-C connector, buttons, U.FL connector, plastic parts, and bottom-side exposed pads. The module shall be placed accurately on the carrier-board footprint to ensure reliable solder joints on the standard castellated pads and, for the Plus version, the inner castellated pads.

If the XIAO module is reflowed onto a carrier board, the FPC antenna, camera module, loose accessories, and any removable cables shall not be installed during reflow. They shall be assembled after the soldering process unless the accessory supplier and production process explicitly allow reflow exposure.

9.3.3 Reflow Soldering Parameters

The reflow profile shall follow the solder paste specification and the assembly factory's qualified process. The parameters in Table 9-6 provide a general lead-free reflow reference and shall be validated before production.

Table 9-6. Reflow Soldering Reference Parameters

Parameter	Reference Condition
Solder paste type	Lead-free solder paste
Preheat ramp rate	Follow solder paste specification
Soak temperature range	Follow solder paste specification
Time above liquidus	Follow solder paste specification
Peak temperature	Follow solder paste and component limits
Cooling rate	Follow solder paste specification
Number of reflow cycles	Validate according to production process

The peak temperature and thermal exposure shall not exceed the limits of the assembled components on the module. Production reflow parameters shall be verified using actual carrier boards, module placement, stencil design, and thermal profiling.

9.4 Production Precautions

The XIAO ESP32-S3 Series contains RF, power management, USB, battery charging, and exposed-pad structures. The following precautions shall be considered during production, testing, and final assembly.

Before assembly, verify the board version, SKU, accessory configuration, and orientation. The XIAO ESP32-S3, XIAO ESP32-S3 Sense, and XIAO ESP32-S3 Plus share the same main board outline, but the pad layout, bottom-side battery pad position, and version-specific peripherals may differ.

During SMT or carrier-board assembly, the footprint shall match the selected version. The XIAO ESP32-S3 Plus uses smaller inner castellated pads between the standard edge pads. These pads require accurate placement and solder process control. Carrier boards designed for multiple versions shall verify BAT pad alignment and bottom-side exposed-pad compatibility before production.

The FPC antenna and U.FL connector shall be handled carefully. Do not pull, twist, or sharply bend the antenna cable during assembly. The antenna shall be installed after soldering and cleaning processes that may expose the cable or FPC body to heat, solvent, or mechanical damage.

For the Sense version, the camera module, MicroSD card slot, microphone area, and expansion board shall be protected from mechanical stress and contamination. The camera lens and FPC cable shall not be pressed during enclosure assembly. If a MicroSD card is installed before shipment, the card retention and insertion clearance shall be checked.

For products using batteries, polarity, connector orientation, insulation, and strain relief shall be verified before power-on. Battery wires shall not be pinched by the enclosure or routed through sharp mechanical features.

After production assembly, visual inspection should confirm solder wetting, absence of bridging, correct antenna connection, clean USB connector, button operation, and proper mechanical clearance. Functional testing should include power-on, USB communication, wireless connection, and version-specific peripherals where applicable.

10. Certifications and Compliance

This chapter lists the certification, compliance, customs classification, and environmental compliance information for the XIAO ESP32-S3 Series. Certification information may vary by product version, SKU, shipping region, or document revision. The latest official certification documents shall be used as the final reference.

10.1 Certification Information

The XIAO ESP32-S3 Series complies with the certification and documentation requirements listed in Table 10-1. The XIAO ESP32-S3 standard version, XIAO ESP32-S3 Sense, and XIAO ESP32-S3 Plus may have different certification document coverage.

Table 10-1. Certification and Compliance Information

Item	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
CE	Supported	Supported	Supported
EU Declaration of Conformity	Supported	Supported	Supported
FCC	Supported	Supported	Supported
RoHS	Supported	Supported	Supported
REACH	Supported	Supported	Supported
TELEC	Supported	Supported	Supported
UK Declaration of Conformity	Supported	Supported	Supported
Country of origin	China	China	China

The certification marks and declaration documents apply to the product configuration as shipped by Seeed Studio. Any modification to the RF circuit, antenna, power system, enclosure, or external wiring may affect the compliance status of the final product.

Table 10-2. Customs Classification Information

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
HS Code	8517180050	8517180050	8543709990
US HS Code	8517180050	8517180050	8517180050
EU HS Code	8543709099	8543709099	8543709099

Parameter	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
Country of Origin	China	China	China

10.2 Compliance Documents and Marks

The certification marks shown for the XIAO ESP32-S3 Series indicate the regulatory and environmental documentation available for each product version. The marks may appear on the product page, product label, package, or official documentation depending on the SKU and region.

Table 10-3. Compliance Documents and Marks by Version

Compliance Document / Mark	XIAO ESP32-S3	XIAO ESP32-S3 Sense	XIAO ESP32-S3 Plus
CE Mark	✓	✓	✓
EU DoC	✓	✓	✓
FCC Mark	✓	✓	✓
RoHS Declaration	✓	✓	✓
REACH Declaration	✓	✓	✓
TELEC Mark	✓	✓	✓
UK DoC	✓	✓	✓

The table identifies compliance documents and marks listed for each version. Match the certificate, declaration, or test report to the ordered SKU and supplied product configuration before final-product integration.

10.3 Compliance Statements

The XIAO ESP32-S3 Series is intended for use as a development board or embedded module in user systems. When the board is integrated into a final product, the system integrator is responsible for evaluating the final product against all applicable regulatory requirements in the target market.

10.3.1 FCC Statement

The XIAO ESP32-S3 Series has FCC certification support as indicated by the product certification information. The certification applies to the product configuration as supplied by Seeed Studio.

If the board is integrated into another product, the final product may require additional compliance evaluation. Changes to the antenna, RF layout, shielding, enclosure, power supply, or external cables may affect RF emissions and compliance status. The final product shall be tested and labeled according to applicable FCC requirements.

10.3.2 CE Statement

The XIAO ESP32-S3 Series has CE compliance support and EU Declaration of Conformity documentation as indicated by the product certification information. The CE-related documentation applies to the product configuration as supplied by Seeed Studio.

When the board is integrated into a final system, the system integrator shall ensure that the final product complies with applicable EU directives and standards. The final enclosure, cable configuration, power supply, antenna placement, and connected peripherals may affect EMC, RF, safety, and environmental compliance.

10.3.3 UK Compliance Statement

The XIAO ESP32-S3 Series has UK compliance documentation according to the product certification information. The UK Declaration of Conformity applies to the product configuration supplied by Seeed Studio.

When the board is integrated into a final system, the system integrator shall ensure that the final product complies with all applicable UK regulatory requirements. The final enclosure, power supply, antenna installation, cable configuration, connected peripherals, and intended operating environment may affect EMC, RF, safety, and environmental compliance.

For products placed on the UK market, the latest official UK Declaration of Conformity and applicable labeling requirements shall be verified before shipment.

10.4 Environmental Compliance

The XIAO ESP32-S3 Series supports environmental compliance documentation according to the certification information listed in this chapter.

The RoHS declaration confirms compliance with restrictions on hazardous substances for each product version. A REACH declaration is available for the XIAO ESP32-S3, XIAO ESP32-S3 Sense, and XIAO ESP32-S3 Plus.

The product shall be handled, stored, used, and disposed of in accordance with local environmental regulations. Batteries, external accessories, packaging materials, and final products using the XIAO ESP32-S3 Series may be subject to additional environmental or

recycling requirements depending on the target market.

Appendix A. Reference Documents

This appendix lists the reference documents used for hardware design, software development, production integration, and compliance verification of the XIAO ESP32-S3 Series.

Table A-1. Reference Documents and Open-Source Materials

Document	Description	Link
Espressif ESP32-S3 Series Datasheet	Electrical characteristics, RF characteristics, GPIO functions, boot configuration, power modes, and SoC-level specifications	https://documentation.espressif.com/esp32-s3_datasheet_en.pdf
Espressif ESP32-S3 Technical Reference Manual	Detailed register-level and peripheral descriptions for firmware development	https://documentation.espressif.com/esp32-s3_technical_reference_manual_en.pdf
Seeed Studio Product Page and Wiki	Ordering information, getting-started guide, software examples, and accessory information	https://wiki.seeedstudio.com/xiao_esp32s3_getting_started/
Seeed Studio XIAO ESP32S3 Schematic	Standard version v1.2 schematic	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_SCH_v1.2.pdf
Seeed Studio XIAO ESP32S3 Eagle Libraries	Standard version v1.1 Eagle schematic and PCB source files	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_v1.1_SCH&PCB_230327.zip
Seeed Studio XIAO ESP32S3 Dimension in DXF	Mechanical dimension drawing for the XIAO ESP32-S3 standard version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_v1.1_Dimensioning.dxf
Seeed Studio XIAO ESP32S3 Eagle Footprint	Eagle footprint library for the XIAO ESP32-S3 standard version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/Seeed-Studio-XIAO-ESP32S3-footprint-eagle.lbr
Seeed Studio XIAO ESP32S3 Factory Firmware	Factory firmware package for the XIAO ESP32-S3 standard version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO-ESP32S3-firmware.zip
Seeed Studio XIAO ESP32S3 Pinout	Pinout reference spreadsheet for the XIAO ESP32-S3 standard version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-

Document	Description	Link
Sheet		ESP32S3/res/XIAO_ESP32S3_Sense_Pinout.xlsx
Seeed Studio XIAO ESP32S3 3D Model	3D model for the XIAO ESP32-S3 standard version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/seeed-studio-xiao-esp32s3-3d_model.zip
Seeed Studio XIAO ESP32S3 Sense Schematic	Schematic reference for the XIAO ESP32-S3 Sense expansion board	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_ExpBoard_v1.0_SCH.pdf
Seeed Studio XIAO ESP32S3 Sense KiCAD Libraries	KiCad library files for the XIAO ESP32-S3 Sense version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/Seeeduino-xiao-ESP32S3-KiCAD-Library.zip
Seeed Studio XIAO ESP32S3 Sense Eagle Libraries	Eagle schematic and PCB source files for the XIAO ESP32-S3 Sense expansion board	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_ExpBoard_v1.0_SCH&PCB_230324.zip
Seeed Studio XIAO ESP32S3 Sense Dimension in DXF (Top)	Top-side mechanical drawing for the XIAO ESP32-S3 Sense expansion board	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_ExpBoard_v1.0_top.dxf
Seeed Studio XIAO ESP32S3 Sense Dimension in DXF (Bottom)	Bottom-side mechanical drawing for the XIAO ESP32-S3 Sense expansion board	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_ExpBoard_v1.0_bot.dxf
Seeed Studio XIAO ESP32S3 Sense Factory Firmware	Factory firmware package for the XIAO ESP32-S3 Sense version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAOESP32S3-Sense-firmware.zip
Seeed Studio XIAO ESP32S3 Sense Pinout Sheet	Pinout reference spreadsheet for the XIAO ESP32-S3 Sense version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_Sense_Pinout.xlsx
XIAO ESP32S3 Sense Housing Design (Top)	Top housing design file for XIAO ESP32-S3 Sense mechanical reference	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO-ESP32S3-Sense-housing-design(top).stp
XIAO ESP32S3	Bottom housing design file for XIAO	https://files.seeedstudio.com/wiki/SeeedSt

Document	Description	Link
Sense Housing Design (Bottom)	ESP32-S3 Sense mechanical reference	udio-XIAO-ESP32S3/res/XIAO-ESP32S3-Sense-housing-design(bottom).stp
Seeed Studio XIAO ESP32S3 Sense 3D Model	3D model for the XIAO ESP32-S3 Sense version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/seeed-studio-xiao-esp32s3-sense-3d_model.zip
Seeed Studio XIAO ESP32S3 Plus Schematic	Schematic and PCB source package for the XIAO ESP32-S3 Plus version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_ESP32S3_Plus_V1.0_SCH_PCB.zip
Seeed Studio XIAO ESP32S3 Plus KiCAD Libraries	KiCad library files for the XIAO ESP32-S3 Plus version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/Seeed_Studio_XIAO_ESP32S3_Plus_KiCAD_Library.zip
Seeed Studio XIAO ESP32S3 Plus Dimension in DXF (Top)	Top-side mechanical drawing for the XIAO ESP32-S3 Plus version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/TOP.dxf
Seeed Studio XIAO ESP32S3 Plus Dimension in DXF (Bottom)	Bottom-side mechanical drawing for the XIAO ESP32-S3 Plus version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/BOTTOM.dxf
Seeed Studio XIAO ESP32S3 Plus Pinout Sheet	Pinout reference spreadsheet for the XIAO ESP32-S3 Plus version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/Seeed_Studio_XIAO_ESP32S3_Plus_Pinout.xlsx
Seeed Studio XIAO ESP32S3 Plus KiCAD File	KiCad schematic and PCB source files for the XIAO ESP32-S3 Plus version	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/Seeed_Studio_XIAO_ESP32S3_Plus_V1.0_SCH%26PCB_KICAD.zip
Seeed Studio XIAO Plus Base with Bottom Pad Lead Out	Reference baseboard design with bottom pads routed out for XIAO ESP32-S3 Plus	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-ESP32S3/res/XIAO_Plus_Base_with_botton_pad_lead_out_V1.0.zip
Seeed Studio XIAO Plus Base without	Reference baseboard design without bottom pad lead-out for XIAO ESP32-S3	https://files.seeedstudio.com/wiki/SeeedStudio-XIAO-

Document	Description	Link
Bottom Pad Lead Out	Plus	ESP32S3/res/XIAO_Plus_Base_without_button_pad_lead_out_V1.0.zip

Select schematics, PCB files, footprints, and mechanical drawings that match the product SKU and hardware revision used in the design. Verify the revision of each reference file before production integration.

Appendix B. Terms and Abbreviations

This appendix defines the common terms, signal names, and abbreviations used in this document.

Table B-1. Terms and Abbreviations

Term	Description
ADC	Analog-to-Digital Converter
BAT	Battery input pads for single-cell Li-ion / Li-Po battery connection
BLE	Bluetooth Low Energy
B2B	Board-to-Board connector
CE	European conformity marking
DVP	Digital Video Port, used by the camera interface
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
FPC	Flexible Printed Circuit
GPIO	General-Purpose Input / Output
I2C	Inter-Integrated Circuit serial bus
I2S	Inter-IC Sound interface
JTAG	Joint Test Action Group debug interface
LGA	Land Grid Array style surface-mount usage
MicroSD	Micro Secure Digital memory card
PDM	Pulse-Density Modulation, used by the digital microphone interface
PMIC	Power Management Integrated Circuit
PSRAM	Pseudo Static Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances

Term	Description
RTC	Real-Time Clock domain of the ESP32-S3
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
U.FL	Miniature RF coaxial connector used for the external FPC antenna
UART	Universal Asynchronous Receiver / Transmitter
USB	Universal Serial Bus
VBUS	USB 5 V power rail or 5 V input/output pin
3V3	Regulated 3.3 V power rail

Table B-2. Signal Naming Conventions

Name	Description
Dx	Arduino-style digital pin name
Ax	Arduino-style analog input name
GPIOx	Native ESP32-S3 GPIO number
IOx	Alternative short form of native GPIO naming
D+ / D−	USB differential data signals
SCK	SPI serial clock
MOSI	SPI master-out slave-in signal
MISO	SPI master-in slave-out signal
CS	SPI chip-select signal
SDA	I2C data signal
SCL	I2C clock signal
TX	UART transmit signal
RX	UART receive signal

Name	Description
EN	Enable / reset control signal
BOOT	Boot-mode selection button or GPIO0 function