REF Schematic for RK3576

Main Functions Introduction

1) PMIC: 1 x RK806S-5 + DiscretePower
2) RAM: 1 x LPDDR4X 32bit
   Option: 1 x LPDDR4 32bit
   Option: 1 x LPDDR5 32bit
3) ROM: 1 x eMMC5.1 + 1 x UFS
   Option: 1 x SPI Flash(FSPI0)
4) Support: 1 x Micro SD Card3.0
   Option: 1 x SPI Flash(FSPI1)
5) Support: 1 x USB TYPEC with Displayport Alt Mode
   Option: 1 x USB2.0
   Option: 1 x USB3.2 Gen1x1 HOST
6) Support: 3 x USB2.0 HOST(USB2.0 HUB) + 1 x USB3.2 Gen1x1 HOST(USB2.0 from HUB)
   Option: 1 x USB3.2 Gen1x1 HOST
7) Support: 1 x a/b/g/n/ac/ax 2T2R SDIO WIFI6 + UART/PCM BT
   Option: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
   Option: 1 x a/b/g/n/ac/ax 2T2R SDIO WIFI + UART/PCM BT
   Option: 1 x a/b/g/n/ac 1T1R SDIO WIFI + UART/PCM BT
8) Support: 1 x PCIe Slot_36P
   Option: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
   Option: 1 x MiniPCIe Slot_with 4G
   Option: 1 x SATA Slot
9) Support: 3 x CAM MIPI CSI RX
   Option: 1 x 4Lanes MIPI DPHY RX Camera + 1 x HDMI RX to MIPI CSI
10) Support: 1 x LCM MIPI DSI TX
   Option: 1 x MIPI to LVDS
11) Support: 1 x HDMI2.1 TX (Up to 4Kx2K@120Hz)
   Option: 1 x LCM eDP TX
12) Support: 2 x 10/100/1000M Ethernet
   Option: 1 x 10/100M Ethernet + 1 x 10/100/1000M Ethernet
13) Support: 1 x Headphone + 2 x SPK + 1 x Analog MIC
   Option: 4 x PDM-DMIC
14) Support: 1 x SPDIF TX + 1 x SPDIF RX
15) Support: 1 x IR Receiver
16) Support: 1 x G-Sensor
17) Support: Array Key(MENU,VOL+,VOL-,ESC)
18) Support: 7 x SARADC + 1 x SARADC only for boot
19) Support: 1 x Debug UART Connector

Note:

The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic.
If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

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Page 28	28.VO-HDMI TX	Default
Page 29	29.WIFI/BT-SDIO+UART_1T1R	Default
Page 30	30.RGMII0 Gigabit Ethernet	Default
Page 31	31.RGMII1 Gigabit Ethernet	Default
Page 32	32.RJ45*2	Default
Page 33	33.Audio-CODEC(ES8311)	Default
Page 34	34.Key-PowerON/Reset/V+/V-/etc	Default
Page 35	35.IIC TO IO/40PIN-CM5	Default
Page 36	36.HW_ID	Default
Page 37	37.LED&FAN	Default
Page 38	38.Mini PICe	Default

Notes

NOTE 1:
Component parameter description
1. NC stands for component not mounted temporarily
2. If Value or option is NC, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Generate Bill of Materials

Header:

Item\tQuantity\tReference\tASSY\tValue\tPCB Footprint\tPN\tPart Type\tManufacturer\tManufacturer Part Number\tDescription\tStatus

Combined property string:

{Item}\t{Quantity}\t{Reference}\t{ASSY}\t{Value}\t{PCB Footprint}\t{PN}\t{Part Type}\t{Manufacturer}\t{Manufacturer Part Number}\t{Description}\t{Status}

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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2025-10-31		1. First version;	

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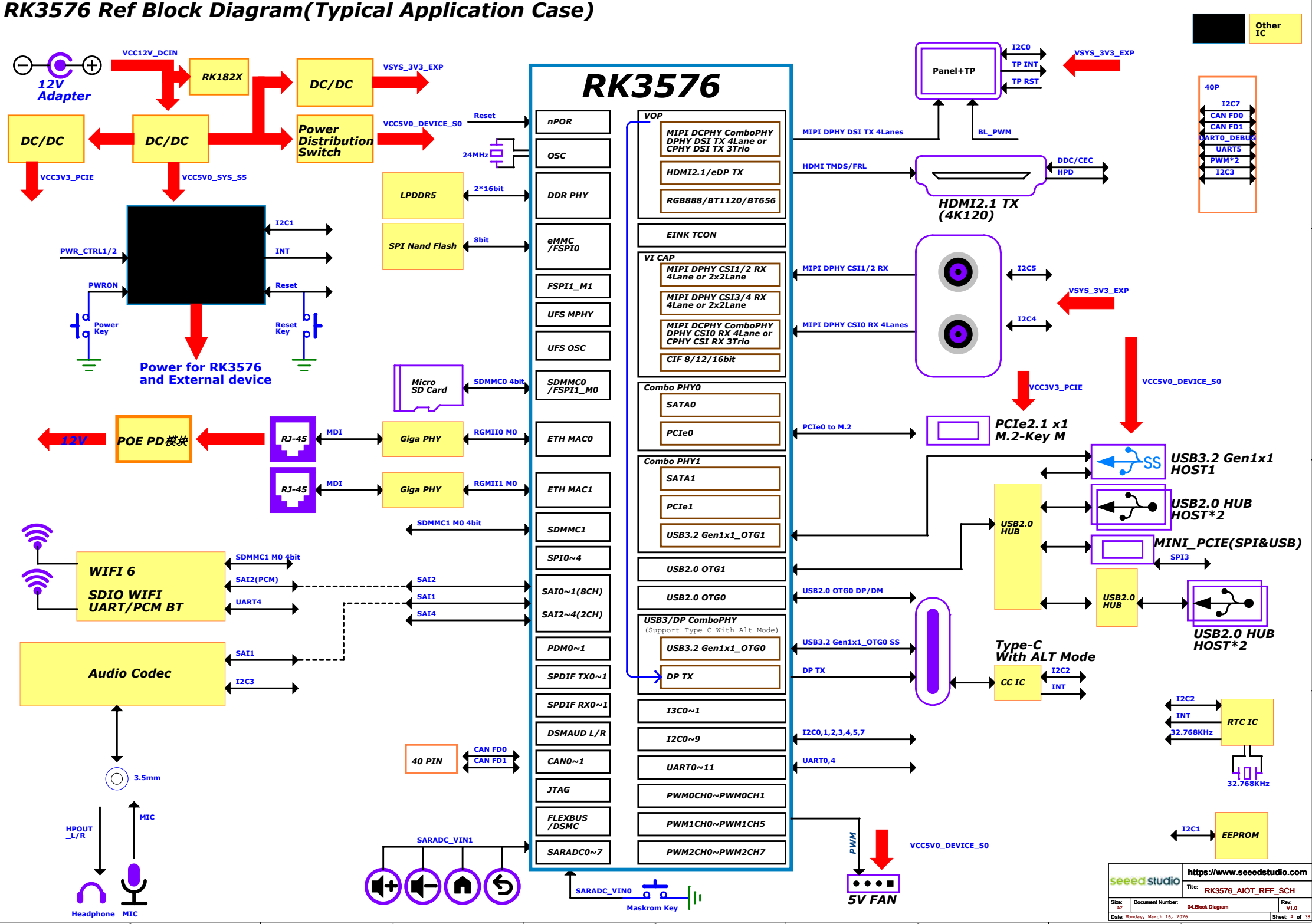
RK3576 Ref Block Diagram(Typical Application Case)



Default Power Tree

Note: Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

9-19V Adapter

VCC12V_DCIN

DC/DC MP9928GL-Z 5V@10000mA

VCC5V0_SYS_S5 Seq:0

Note: With PCIe/SATA, the current is estimated according to the actual number of PCIe/SATA

Power Distribution Switch SY6288E1AAC 5V@3000mA

VCC5V0_DEVICE_S0 Seq:3A
- RPI 40PIN 5V Max:
- FAN 5V Max:
- TYPEC 5V Max:
- USB2_HOST 5V Max:
- HDMI TX 5V Max:
- Work LED Max:

DC/DC TPS62A06DRLR 3.3V@6000mA

VSYS_3V3_EXP Seq:6A
- MIPI DSI LCM 3.3V Max:
- MIPI CSI0&CSI1 3.3V Max:
- RPI 40PIN 3.3V Max:
- USE LED 3.3V Max:

DC/DC TPS62A06DRLR 3.3V@6000mA

VCC3V3_PCIE Seq:3A
- M.2 PCIE M-KEY 3.3V Max:
- MINI PCIE(SPI&USB) Max:

RK806S-5

		Power on Sequence		
VCC1	BUCK1 6.5A max	Seq:2	VDD_CPU_BIG_S0 Max:4A	VDD_CPU_BIG_SOC
VCC2	BUCK2 5.0A max	Seq:2	VDD_NPU_S0 Max:4A	VDD_NPU_SOC
VCC3	BUCK3 5.0A max	Seq:2	VDD_CPU_LIT_S0 Max:2A	VDD_CPU_LIT_SOC
VCC4	BUCK4 5.0A max	Seq:5	VCC_3V3_S3 Max:	LOAD SWITCH VCC_3V3_S0
VCC5	BUCK5 3A max	Seq:2	VDD_GPU_SOC Max:3A	VDD_GPU_SOC
VCC6	BUCK6 3A max	Seq:7	VDDQ_DDR_S0 Max:	LPDDR5 VDDQ Max: DDRPHY_CK_VDDQ_SOC Max: DDRPHY_VDDQ_SOC Max:
VCC7	BUCK7 3A max	Seq:2	VDD_LOGIC_S0 Max:2A	VDD_LOGIC_SOC VDD_LOGIC_MEM_SOC
VCC8	BUCK8 3A max	Seq:3	VCC_1V8_S3 Max:	LOAD SWITCH 3 x LDO 3 x LDO 3 x LDO LOAD SWITCH CC IC 3V3 Max: eMMC_3V3 Max: TP 3V3 Max: WIFI BAT Max: IR 3V3 Max: Debug Uart 3V3 Max: PMUIO1_VCC_SOC Max:
VCC9	BUCK9 3A max	Seq:4	VDD2_DDR_S3 Max:	LPDDR5 VDD2H Max: DDRPHY_CKE_VDDQ_SOC Max:
VCC10	BUCK10 3A max	Seq:2	VDD_DDR_S0 Max:2A	DDRPHY_DVDD_SOC
VCC_2V0_PLDO_S3	PLDO1 500mA max	Seq:3	VCCA_1V8_S0	NMOS VCC_1V8_S0 eMMC_1V8 PMOS LPDDR4/4X VDD1 Max: LPDDR5 VDD1 Max: WIFI VCCIO Max: PMUIO0_VCC1V8_SOC Max: VCCIO0_VCC1V8_SOC Max: VCCIO3_VCC_SOC Max:
VCC11	PLDO2 300mA max	Seq:5	VCCA1V8_PLDO2_S0	SARADC_AVDD1V8_SOC Max:
	PLDO3 300mA max	Seq:4	VDDA_1V2_S0	VCCIO7_VCC_SOC Max: MIPI_DCPHY_AVDD1V2_SOC Max:
VCC12	PLDO4 500mA max	Seq:5	VCCA_3V3_S0	CODEC VCCA3V3 Max:
	PLDO5 300mA max	Seq:5	VCCIO_SD_S0	VCCIO1_VCC_SOC Max:
VCCA	PLDO6 300mA max	Seq:3	VCCA1V8_PLDO6_S3	VCCA1V8_PLDO6_S3 Max:
VCC_1V1_NLDO_S3	NLDO1 300mA max	Seq:2	VDD_0V75_S3	PMU_LOGIC_DVDD0V75_SOC Max:
	NLDO2 300mA max	Seq:2	VDDA_DDR_PLL_S0	DDRPHY_PLL_DVDD_SOC Max:
	NLDO3 500mA max	Seq:2	VDDA_HDMI_S0	HDMI_TX/eDP_TX_AVDDD0V75_SOC Max: HDMI_TX/eDP_TX_AVDDC0V75_SOC Max:
VCC_1V1_NLDO_S3	NLDO4 500mA max	Seq:2	VDDA_0V85_S0	ESD & Ferrite bead
	NLDO5 300mA max	Seq:2	VDDA_0V75_S0	PLL_DVDD0V75_SOC Max: OTP_DVDD0V75_SOC Max: USB2_OTG_DVDD0V75_SOC Max: MIPI_DCPHY_AVDD_SOC Max: MIPI_CSI1/2_RX_AVDD0V75_SOC Max: MIPI_CSI3/4_RX_AVDD0V75_SOC Max:
	EXT DC/DC ,2A (VCC_3V3_S3 EN)	Seq:1	VDD2L_0V9_DDR_S3 Max:	LPDDR5 VDD2L Max:
	EXT DC/DC ,2A (PMIC_EXT_EN_OUT EN)	Seq:1	VCC_2V0_PLDO_S3 Max:	
	EXT DC/DC ,2A (PMIC_EXT_EN_OUT EN)	Seq:1	VCC_1V1_NLDO_S3 Max:	
	EXT DC/DC ,2A (VCC_3V3_S0 EN)	Seq:5B	VCC_UFS_S0 Max:	VCC_UFS_S0(Opt) Max:
	EXT LDO	Seq:0A	VCC3V3_RTC_S5 Max:	RTC_3V3 Max:

- LOAD SWITCH VCC_3V3_S0
  - CODEC ES8311 3V3 Max:
  - USB2 HUB Max:
  - VCC_UFS_S0 Max:
  - RGMII PHY0/1 3V3 Max:
  - RGMII PHY1 VCCIO Max:
  - SPDIF TX/RX Max:
  - G-Sensor 3V3 Max:
  - VCCIO2_VCC_SOC Max:
  - VCCIO4_VCC_SOC Max:
  - VCCIO6_VCC_SOC Max:
  - USB2_OTG_AVDD3V3_SOC Max:
- LOAD SWITCH
  - SD Card 3V3 Max:
  - CAM 1V2 Max:
  - CAM 2V8 Max:
  - CAM 1V8 Max:
  - LCD 3V3 Max:
- NMOS VCC_1V8_S0
  - VCCIO5_VCC_SOC Max:
- eMMC_1V8 / PMOS
  - UFS_VCCQ2_1V8_S0 Max:
- ESD & Ferrite bead
  - OSC_AVDD1V8_SOC Max:
  - PLL_AVDD1V8_SOC Max:
  - DDRPHY_PLL_AVDD1V8_SOC Max:
  - UFS_AVDD1V8_SOC Max:
  - OSC_UFS_AVDD_SOC Max:
- USB3_OTG0/DP_TX_AVDD1V8_SOC Max:
- USB2_OTG_AVDD1V8_SOC Max:
- MIPI_D/C_PHY_AVDD1V8_SOC Max:
- MIPI_CSI1/2_AVDD1V8_SOC Max:
- MIPI_CSI3/4_AVDD1V8_SOC Max:
- HDMI_TX/eDP_TX_AVDDIO1V8_SOC Max:
- HDMI_TX/eDP_TX_AVDDCMN1V8_SOC Max:
- PCIE0_SATA0_AVDD1V8_SOC Max:
- PCIE1_SATA1_USB3_OTG1_AVDD1V8_SOC Max:
- UFS_AVDD0V85_SOC Max:
- USB3_OTG0/DP_TX_AVDD0V85_SOC Max:
- USB3_OTG0/DP_TX_DVDD0V85_SOC Max:
- PCIE0_SATA0_AVDD0V85_SOC Max:
- PCIE1_SATA1_USB3_OTG1_AVDD0V85_SOC Max:

Note:
The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

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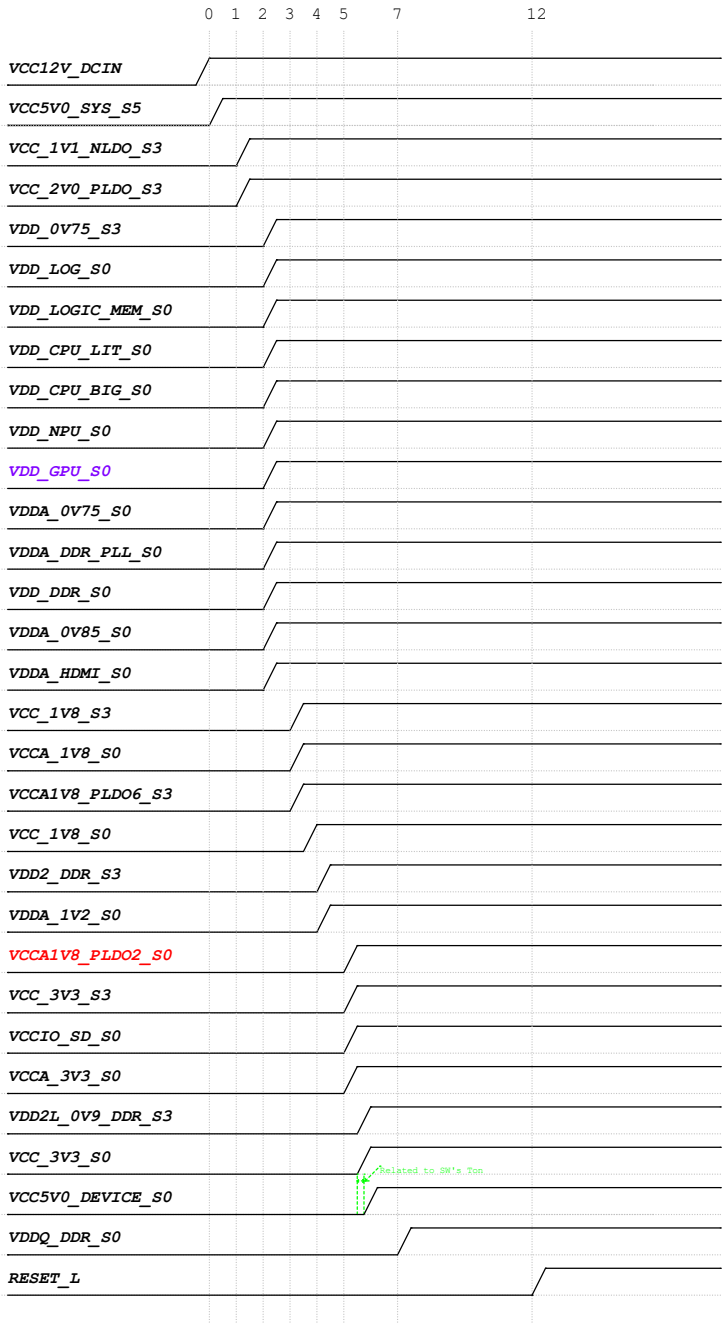
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA_HDMI_S0	Slot:2	0.75V	ON	0.8375V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

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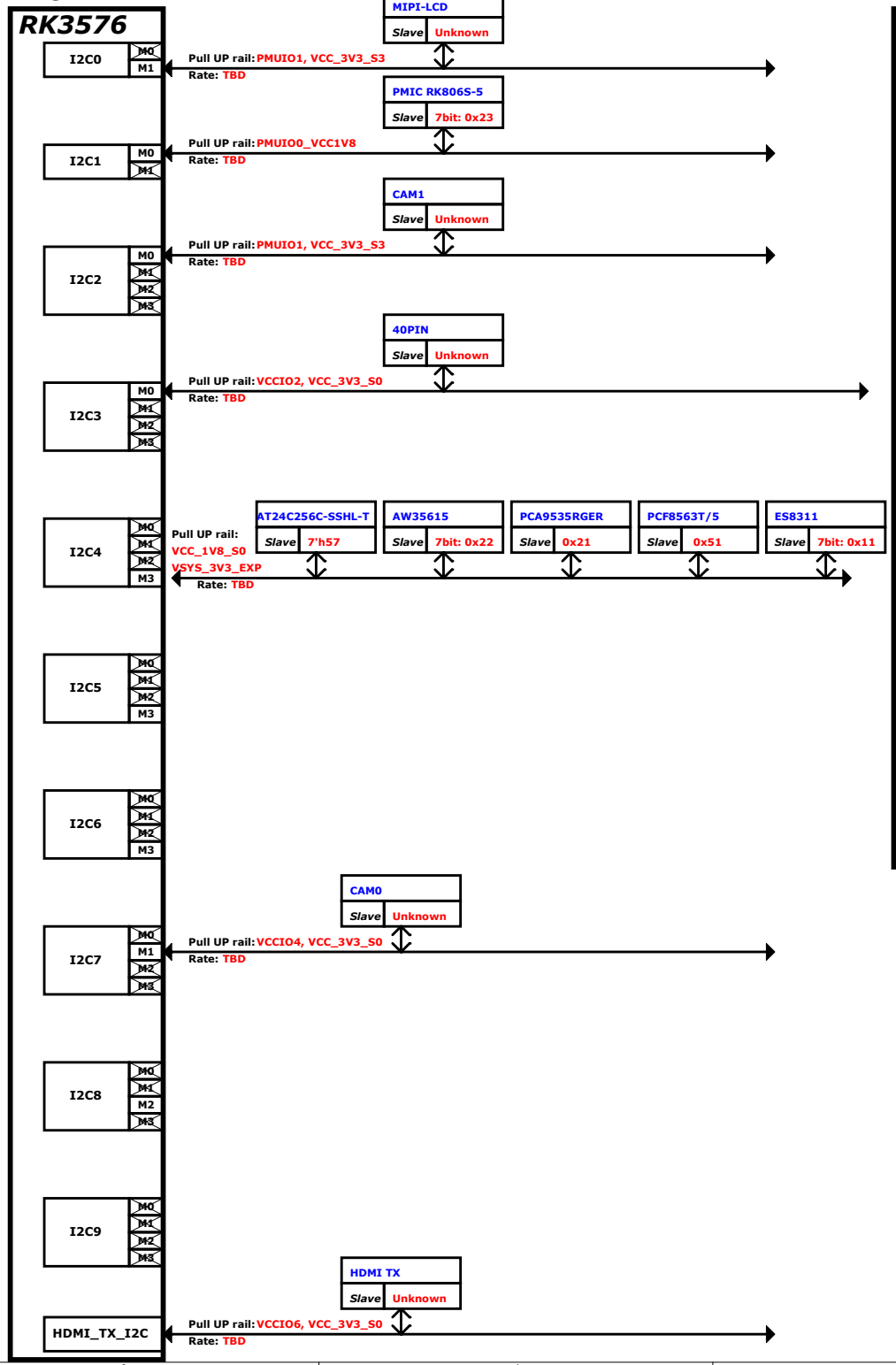
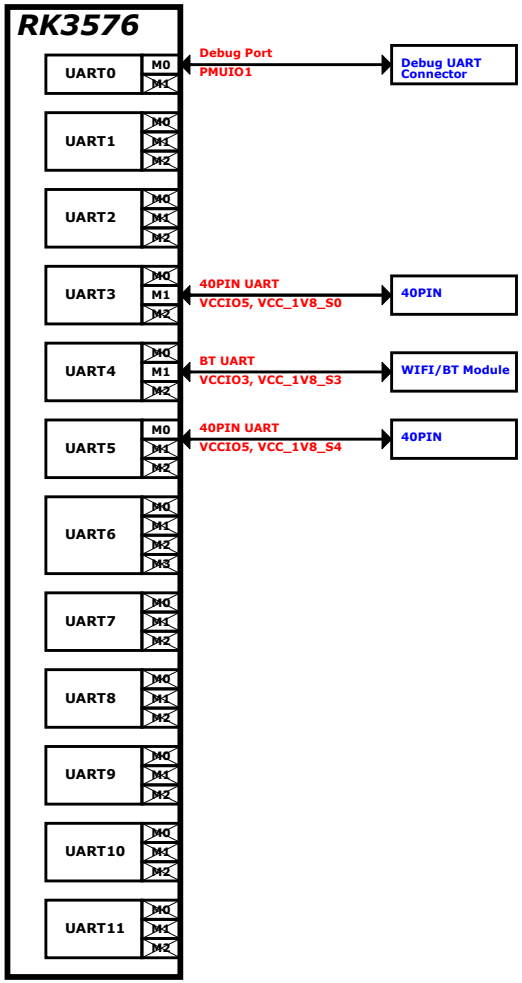
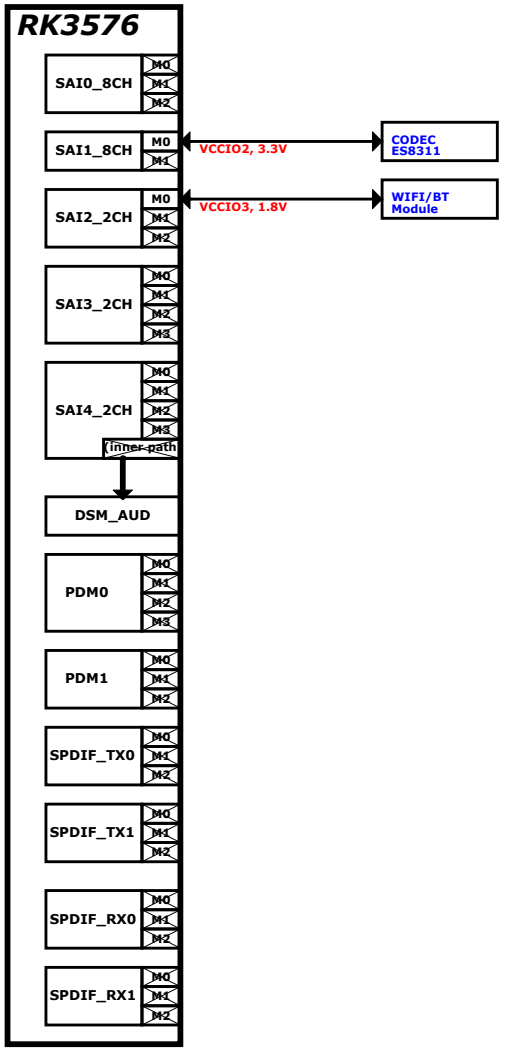
I2C MAP



UART MAP



Audio MAP



Note:

M0 Unselected IOmux path

M1 IOmux path in use

At the same time, only one path can be selected.

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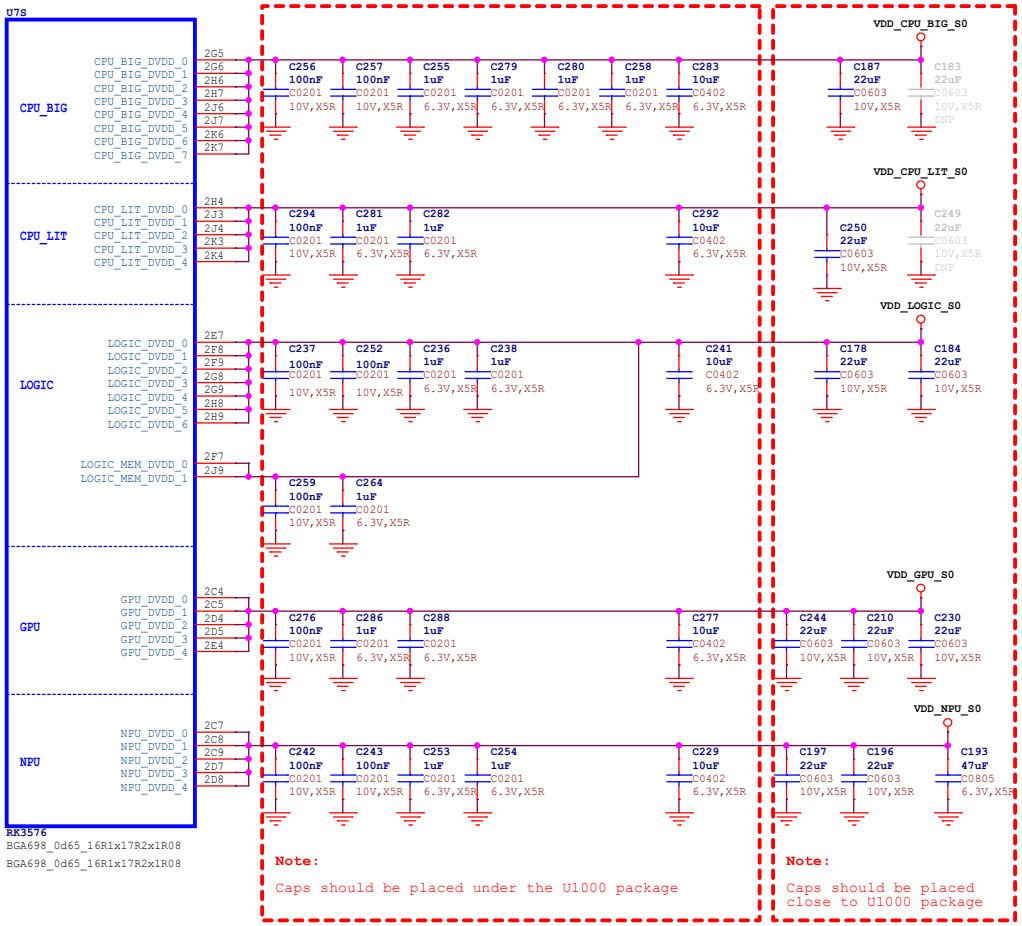
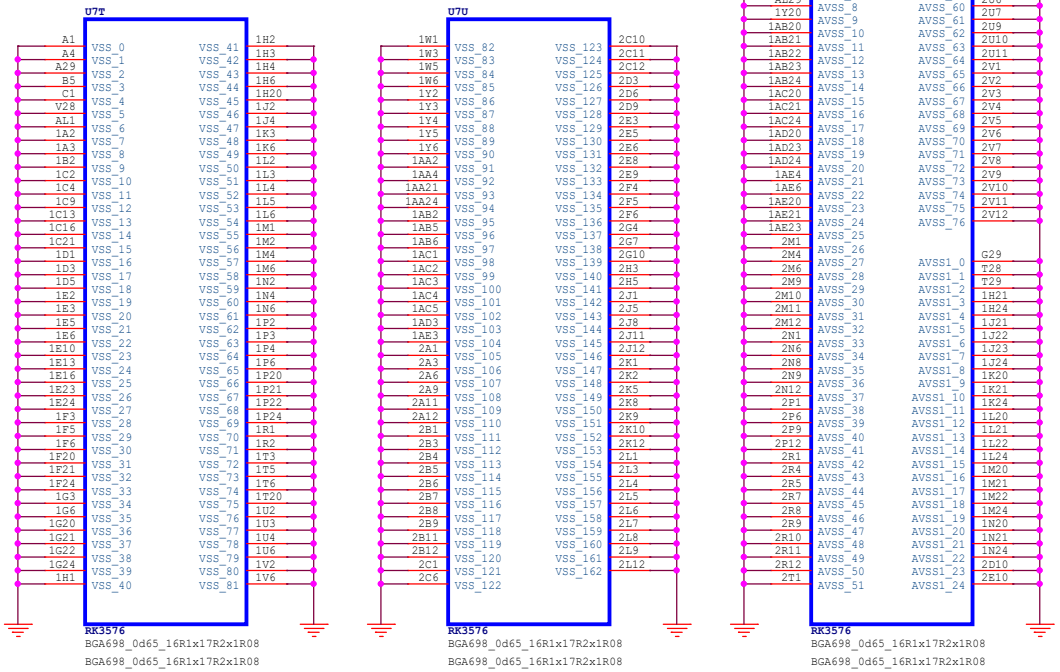
RK3576_S (Power)



RK3576_T/U/V (GND)



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RK3576_E (PMUIO0/1)

Note:
Adjust CL1 and CL2 according to the crystal specification
The the load capacitance CL is recommended by the
crystal vendors to obtain target clock frequency.
CL=(CL1*CL2/(CL1+CL2)))+PCB strays Total CL<=12pF

U7E

OSC

R37 22R 5% R0201 — XOUT24M U29 — OSC_XOUT
Y1
R44 510K 1% R0402
XIN24M U28 — OSC_XIN
C24 15pF C0402 50V,NPO
24MHz X4-SMD-3_2X2_5X1_0MM 20ppm,12pF
C23 15pF 50V,NPO C0402

VCC_1V8_PLL_S0 — R318 0R 1% R0201 — 2J10 — OSC_AVDD1V8
C219 100nF C0201 10V,X5R

VCCA1V8_PLDO6_S3 — R329 0R 1%R0201 DNP
Option:
Reserved for USB wake-up

Note:
When the following functions are required,
OSC_AVDD1V8 must remain powered.
1. PMU MCU is required;
2. USB wake-up function;
3. IR wake-up function.

PLL

VDDA_0V75_S0 — R316 0R 5% R0402 — 2G11 — PLL_DVDD0V75
Option:
Ferrite Bead
C207 100nF C0201 10V,X5R

VCC_1V8_PLL_S0 — 2H12 — PLL_AVDD1V8
C204 100nF C0201 10V,X5R

2G12 — PLL_AVSS

PMUIO0 Domain
Operating Voltage=1.8V

NPOR — W28 — C189 100nF C0201 10V,X5R — RESET_L [19,34]
Note: Closed to Pin W28
R54 0R 1% R0201 — RESET_L
TVSS — 2H10

--	--	--	AUPLL_CLK_IN_M0	REF_CLK0_OUT	GPIO0_A0_d
--	TSADC_CTRL_ORG	TSADC_CTRL_M0	--	--	GPIO0_A1_z
I2C6_SCL_M0	CLK0_32K_OUT	CLK_32K_IN	--	--	GPIO0_A2_d
--	TSADC_CTRL_M1	PWR_CTRL1	--	--	GPIO0_A3_d
--	--	PWR_CTRL2	--	--	GPIO0_A4_d
I2C6_SDA_M0	--	PWR_CTRL3	--	--	GPIO0_A5_d
--	--	PMIC_INT	--	--	GPIO0_A6_u
--	--	SPI2_CSN1_M0	--	SDMMC0_DETN	GPIO0_A7_u

V29 — GPIO0_A0 [38]
1R24 — TSADC_CTRL_M0
1U23 — 32KOUT_RTC2SOC [20]
Y28 — PMIC_PWR_CTRL1 [19]
1T24 — PMIC_PWR_CTRL2 [19,20]
Y29 — RTC_INT_L [20]
1T21 — PMIC_INT_L [19]
1U21 — SDMMC0_DET_L [24]
C203 1nF 16V,X7R C0201
1U22 — WIFI_WAKE_HOST_H [29]
1P23 — BT_WAKE_HOST_H [29]
1T22 — I2C1_SCL_M0_RK806 [19]
1T23 — I2C1_SDA_M0_RK806 [19]

I2C0_SCL_M0	--	SPI2_CSN0_M0	AUPLL_CLK_IN_M1	--	GPIO0_B0_z
I2C0_SDA_M0	--	SPI2_MISO_M0	--	--	GPIO0_B1_z
I2C1_SCL_M0	--	SPI2_CLK_M0	--	--	GPIO0_B2_z
I2C1_SDA_M0	--	SPI2_MOSI_M0	--	--	GPIO0_B3_z

PMUIO0_VCC1V8 — 2K11 — C218 100nF C0201 10V,X5R — VCC_1V8_S3

VCC_1V8_S3
R287 10K 1% R0201 — RESET_L
R299 100K 1% R0402 — SDMMC0_DET_L
R107 2.2K 1% R0201 — I2C1_SDA_M0_RK806
R101 2.2K 1% R0201 — I2C1_SCL_M0_RK806

PMUIO1 Domain
Operating Voltage=1.8V/3.3V

--	PWM1_CH0_M0	--	UART4_TX_M2	I2C1_SCL_M1	--	REF_CLK1_OUT	GPIO0_B4_d
--	PWM1_CH1_M0	--	UART4_RX_M2	I2C1_SDA_M1	--	--	GPIO0_B5_d
--	PWM1_CH2_M0	--	EDP_TX_HPDIN_M1	HDMI_TX_HPDIN_M1	--	SDMMC1_DETN_M2	SDMMC0_PWREN	GPIO0_B6_d
--	PWM1_CH4_M0	NPU_AVS	UART1_TX_M0	I2C2_SCL_M0	--	--	--	GPIO0_B7_d
--	PWM1_CH3_M0	CPULIT_AVS	UART1_RX_M0	I2C2_SDA_M0	--	--	--	GPIO0_C0_d
--	--	I3C0_SCL_M0	UART8_TX_M2	I2C0_SCL_M1	--	--	--	GPIO0_C1_d
--	--	I3C0_SDA_M0	UART8_RX_M2	I2C0_SDA_M1	--	--	--	GPIO0_C2_d
--	PWM0_CH1_M0	SPI0_CSN1_M0	--	HDMI_TX_CEC_M1	PDM0_CLK1_M0	--	--	GPIO0_C3_d
--	PWM0_CH0_M0	--	UART10_TX_M2	--	PDM0_CLK0_M0	--	SAI0_MCLK_M1	GPIO0_C4_d
--	--	I3C0_SDA_PU_M0	UART10_RX_M2	DP_HPDIN_M1	--	--	SAI0_SDO0_M1	GPIO0_C5_d
--	--	SPI0_CSN0_M0	--	I2C3_SCL_M1	--	--	SAI0_SCLK_M1	GPIO0_C6_d
--	--	SPI0_CLK_M0	--	I2C3_SDA_M1	--	--	SAI0_LRCK_M1	GPIO0_C7_d

AD28 — USBCC_INT_L [21]
AD29 — PCIE_PWREN_H_GPIO0B5 [18]
1Y24 — SDMMC0_PWREN_H [24]
1W24 — I2C2_SCL_M0_CC_RTC [27]
AB29 — I2C2_SDA_M0_CC_RTC [27]
AB28 — I2C0_SCL_M1_TP [27]
1Y24 — I2C0_SDA_M1_TP [27]
1W21 — USB_HUB_RST [22]
1W22 — GPIO0_C4_3V3 [35]
1AA22 — GPIO0_C5_3V3 [35]
1Y21 — GPIO0_C6_3V3 [35]
1Y23 — GPIO0_C7_3V3 [35]

R41 2.2K 1% R0201 — I2C2_SCL_M0_CC_RTC
R40 2.2K 1% R0201 — I2C2_SDA_M0_CC_RTC

--	--	SPI0_MOSI_M0	--	--	PDM0_SDI1_M0	SAI0_SDI1_M1	GPIO0_D0_d
--	--	SPI0_MISO_M0	--	--	PDM0_SDI2_M0	SAI0_SDI2_M1	GPIO0_D1_d
UART1_CTSN_M0	PWM1_CH5_M0	CPUBIG_AVS	--	I2C4_SCL_M0	PDM0_SDI3_M0	SAI0_SDO2_M1	SAI0_SDI3_M1	GPIO0_D2_d
UART1_RTSN_M0	PWM2_CH0_M0	GPU_AVS	--	I2C4_SDA_M0	PDM0_SDI3_M0	SAI0_SDO1_M1	SAI0_SDI3_M1	GPIO0_D3_d
--	--	--	JTAG_TCK_M1	UART0_TX_M0	--	--	--	GPIO0_D4_u
--	--	--	JTAG_TMS_M1	UART0_RX_M0	--	--	--	GPIO0_D5_u

1W23 — LTE_LED_WWAN# [38]
AC28 — WIFI_PWREN_L [29]
1Y22 — PCIE0_WAKEn_M0 [26]
1AA23 — GPIO0_D3_3V3 [35]
1U24 — UART0_TX_M0_DEBUG [35]
AA28 — UART0_RX_M0_DEBUG [35]

R39 2.2K 1% R0201 — I2C0_SCL_M1_TP
R38 2.2K 1% R0201 — I2C0_SDA_M1_TP

PMUIO1_VCC — 1U20 — C206 100nF C0201 10V,X5R — VCC_3V3_S3
PMU_LOGIC_DVDD0V75_0 — 2L2
PMU_LOGIC_DVDD0V75_1 — 2L10 — C311 100nF C0201 10V,X5R — C232 100nF C0201 10V,X5R — VDD_0V75_S3

PMUIO0/PMUIO1/VCCIO7 Domain Logic Power
Operating Voltage=0.75V

RK3576
BGA698_0d65_16R1x17R2x1R08
BGA698_0d65_16R1x17R2x1R08

RK3576_R (SARADC)

U7R

SARADC
12-bit 1MS/s

SARADC_IN0_BOOT	A25	SARADC_VIN0_BOOT	C194 1nF 16V,X7R C0201
Recovery/ SARADC_IN1	1A22	SARADC_VIN1_KEY/RECOVERY	C195 1nF 16V,X7R C0201
SARADC_IN2	1B19	SARADC_VIN2_HW_ID	C215 1nF 16V,X7R C0201
SARADC_IN3	1C19	SARADC_VIN3_HP_HOOK	C211 1nF 16V,X7R C0201
SARADC_IN4	1E18	SARADC_VIN4	C222 1nF 16V,X7R C0201
SARADC_IN5	1D19	SARADC_VIN5	C214 1nF 16V,X7R C0201
SARADC_IN6	1D21	SARADC_VIN6	C205 1nF 16V,X7R C0201
SARADC_IN7	1E19	SARADC_VIN7	C213 1nF 16V,X7R C0201

Note:This cap should be placed close to RK3576
Option:
If SARADC_IN4~7 is not used, the filtering capacitor can also be omitted

SARADC_AVDD1V8 — 2A10 — VCCA1V8_PLDO2_S0
C225 100nF C0201 10V,X5R
Internally connected to OTP_AVDD1V8.

TSADC
TSADC_TEST_OUT_TS — 2F10

OTP
OTP_DVDD0V75 — 2H11
C224 100nF C0201 10V,X5R
VDD_LOGIC_S0

Note:
For new projects, it is recommended to modify the power supply for OTP_DVDD0V75 to VDD_LOGIC_S0.
Using VDD_0V75_S0 as the power supply for OTP_DVDD0V75 in existing projects is also risk-free.

RK3576
BGA698_0d65_16R1x17R2x1R08
BGA698_0d65_16R1x17R2x1R08

VCCA1V8_PLDO2_S0
R302 10K 1% R0201 — SARADC_VIN0_BOOT
R295 6.8K 1% R0402

Note:
Closed to RK3576
Stay away from strong interference signals

BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	10K	1.13K	416	FSPI0->USB
Config3	10K	2.49K	816	FSPI1_M0->EMMC->USB
Config4	10K	4.3K	1231	FSPI1_M1->EMMC->USB
Config5	10K	6.8K	1658	FSPI0->UFS->USB
Config6	10K	10K	2048	FSPI1_M0->UFS->USB
Config7	10K	14.7K	2437	UFS->USB
Config8	10K	23.2K	2862	UFS->SDMMC0->USB
Config9	10K	40.2K	3279	RFU
Config10	10K	88.7K	3680	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

Note:
Must be mounted
VCCA1V8_PLDO2_S0
R303 10K 1% R0201 — SARADC_VIN1_KEY/RECOVERY

SARADC_VIN0_BOOT [34]
SARADC_VIN1_KEY/RECOVERY [34]
SARADC_VIN2_HW_ID [36]
SARADC_VIN3_HP_HOOK [33]

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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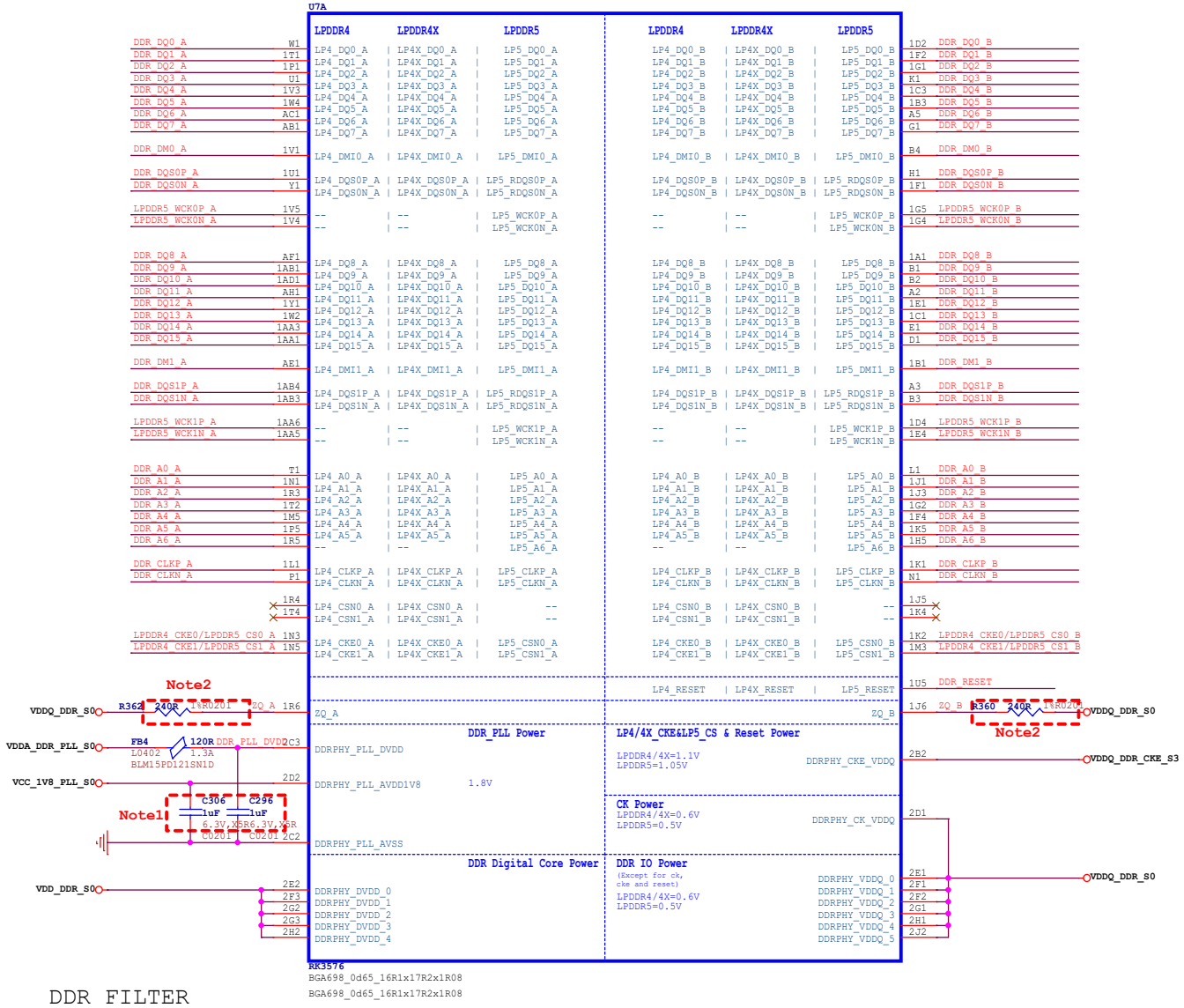
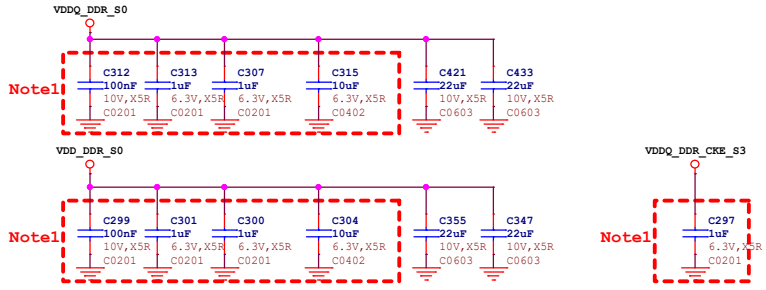
RK3576_A(DDRPHY)



DDR FILTER

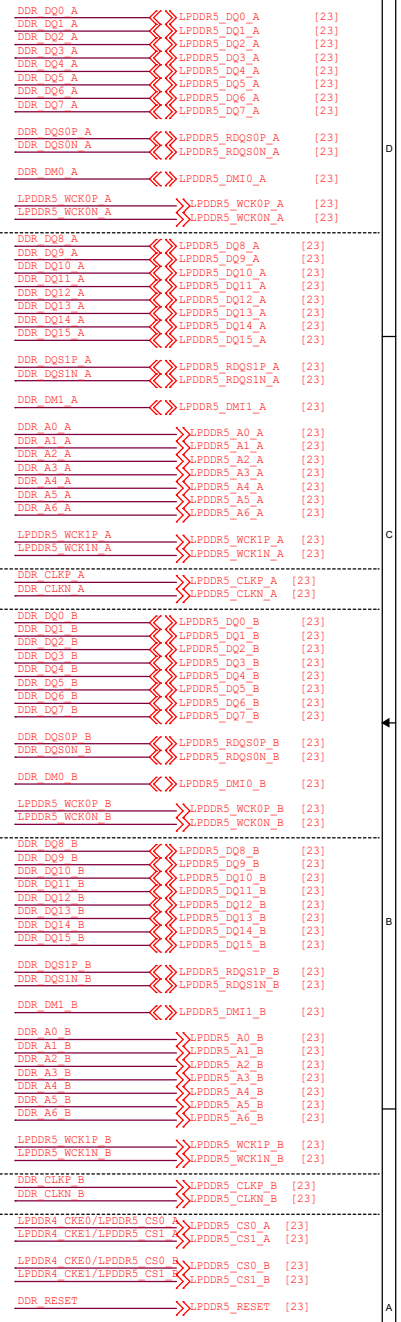


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR5



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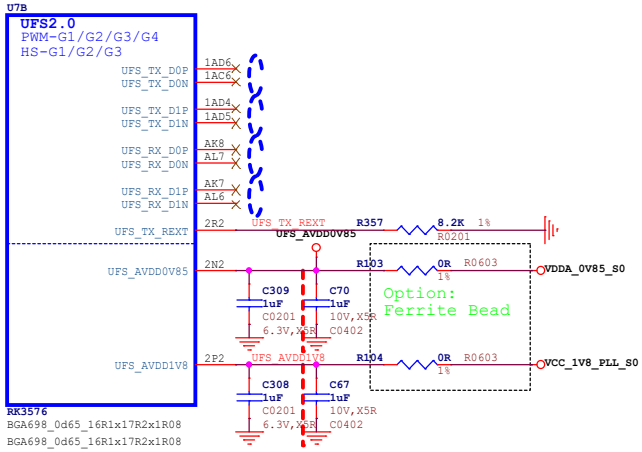
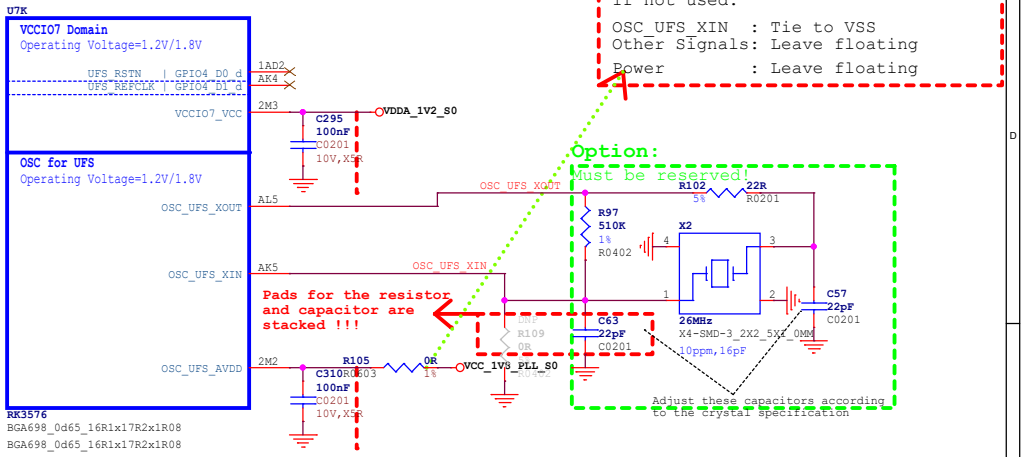
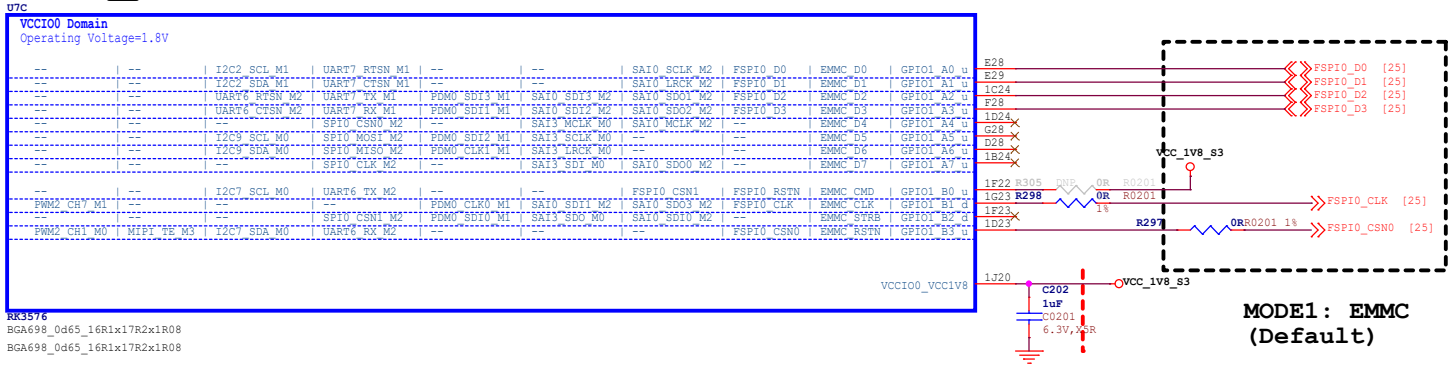
RK3576_B (UFS2.0)





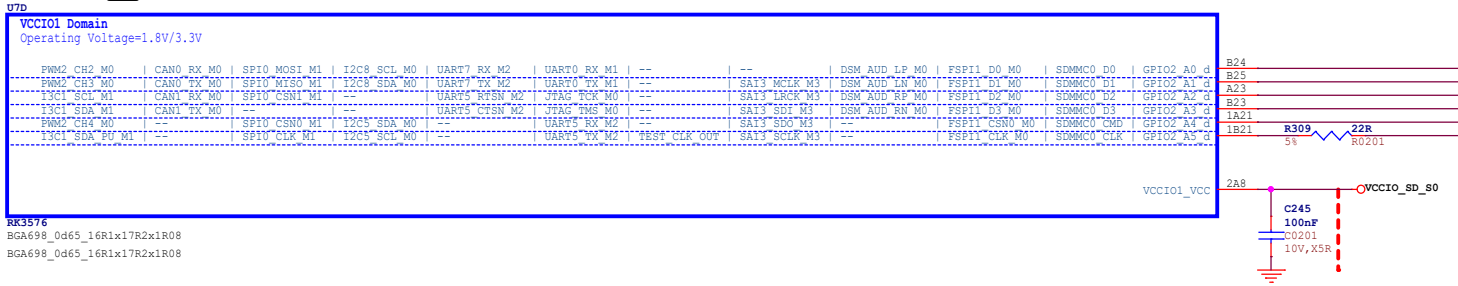
Note:
If not used:
OSC_UFS_XIN : Tie to VSS
Other Signals: Leave floating
Power : Leave floating

RK3576_C (VCCIO0)



MODE1: EMMC (Default)

RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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RK3576_L (USB3/DP)

Note:
If not used:
Signal: Leave floating
Power : Leave floating

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

U7L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

-- | DP_TX_AUXP
-- | DP_TX_AUXN
USB3_OTG0_SSRX1P | DP_TX_D0P
USB3_OTG0_SSRX1N | DP_TX_D0N
USB3_OTG0_SSTX1P | DP_TX_D1P
USB3_OTG0_SSTX1N | DP_TX_D1N
USB3_OTG0_SSRX2P | DP_TX_D2P
USB3_OTG0_SSRX2N | DP_TX_D2N
USB3_OTG0_SSTX2P | DP_TX_D3P
USB3_OTG0_SSTX2N | DP_TX_D3N
USB3_OTG0_REXT | DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85
USB3_OTG0_DP_TX_DVDD0V85
USB3_OTG0_DP_TX_AVDD1V8

RK3576
BGA698_0d65_16R1x17R2x1R08
BGA698_0d65_16R1x17R2x1R08

Support: Type-C With Displayport Alternate Mode

Diff 100 Ohm ±10%
2T2 DP_TX_AUXP [21]
2T3 DP_TX_AUXN [21]

Diff 95 Ohm ±10%
AK10 USB3_OTG0_SSRX1P [21]
AL10 USB3_OTG0_SSRX1N [21]
AL11 USB3_OTG0_SSTX1P [21]
AK11 USB3_OTG0_SSTX1N [21]
AK12 USB3_OTG0_SSRX2P [21]
AL12 USB3_OTG0_SSRX2N [21]
AL13 USB3_OTG0_SSTX2P [21]
AK13 USB3_OTG0_SSTX2N [21]

2T7 USB3_OTG0_DP_TX_REXT R337 1% 8.2K R0201
2M5 2N5 VDDA_0V85_S0
C278 1uF 6.3V,X5R C0201
DNP C58 1uF 10V,X5R C0402
2N4 VCCA_1V8_S0
C289 1uF 6.3V,X5R C0201
DNP C69 1uF 10V,X5R C0402

VCCA_1V8_S0
R348 DNP 10K 1% R0201
[12] USB2_OTG0_ID
R340 DNP 1% 100R R0201
DNP R347 10K 1% R0201

MODE1: TypeC with ALT (Default)

RK3576_M (USB2)

Note:
The USB20_VBUSDET pin internal has a pull-down resistance (40K ohm) to ground. The resistance creates a voltage with the external series 30K ohm resistor. The VBUSDET pin voltage range <=3.3V.

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

U7M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP
USB2_OTG0_DM
USB2_OTG0_ID
40K
USB2_OTG0_VBUSDET
USB2_OTG0_REXT

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP
USB2_OTG1_DM
USB2_OTG1_ID
40K
USB2_OTG1_VBUSDET
USB2_OTG1_REXT
USB2_OTG_DVDD0V75
USB2_OTG_AVDD1V8
USB2_OTG_AVDD3V3

RK3576
BGA698_0d65_16R1x17R2x1R08
BGA698_0d65_16R1x17R2x1R08

Diff 90 Ohm ±10%
AK9 USB2_OTG0_DP [21]
AL9 USB2_OTG0_DM [21]
2R6 Note: There is an internal pull-up resistor connected to 1.8V
USB2_OTG0_ID [12]
2P3 USB2_OTG0_VBUSDET [21]
2R3 USB2_OTG0_REXT R352 200R 1%R0201
C293 100nF 25V,X7R C0402

Diff 90 Ohm ±10%
2T4 USB2_HOST1_DP [22]
2T5 USB2_HOST1_DM [22]
2T9
2T10

2U8 USB2_OTG1_REXT R333 200R 1%R0201
2P5 USB2_OTG_DVDD0V75 R108 0R 1%R0201 VDDA_0V75_S0
R111 0R DNP 1%R0201 VDD_0V75_S3
C291 100nF 10V,X5R C0201
2P4 USB2_OTG_AVDD1V8 R113 0R 1%R0201 VCCA_1V8_S0
R115 0R DNP 1%R0201 VCC_1V8_S3
C290 100nF 10V,X5R C0201
DNP C68 1uF 10V,X5R C0402
2P7 USB2_OTG_AVDD3V3 R330 0R 1%R0201 VCC_3V3_S0
R323 0RDNP 1%R0201 VCC_3V3_S3
C251 100nF 10V,X5R C0201

Note:
USB2_OTG0:
DP/DM :Must be used for download
ID :According to demand,if not used,leave floating
VBUSDET:Must be used for download
REXT :200ohm 1% resistor must be connected externally
Power :Must supply power
USB2_OTG1:
If not used:
DP/DM :Leave floating
ID :Leave floating
VBUSDET:Leave floating
REXT :Leave floating

Note!!!
The USB2 PHY1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

Option:
USB Wake up

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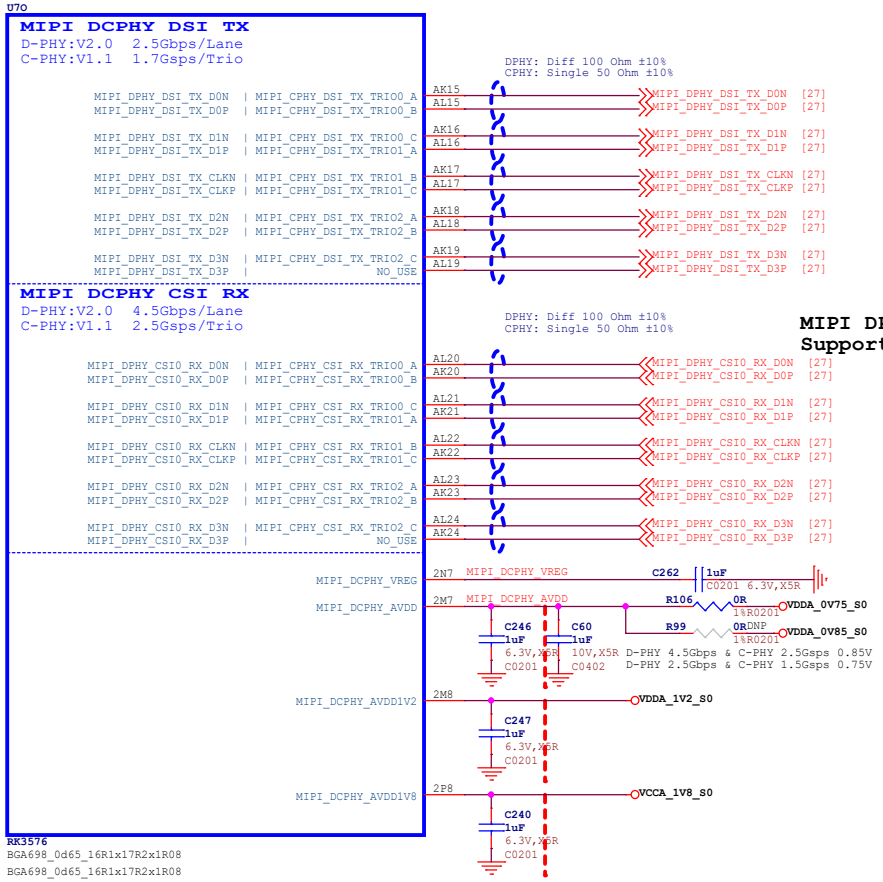
RK3576_O(MIPI DCPHY)



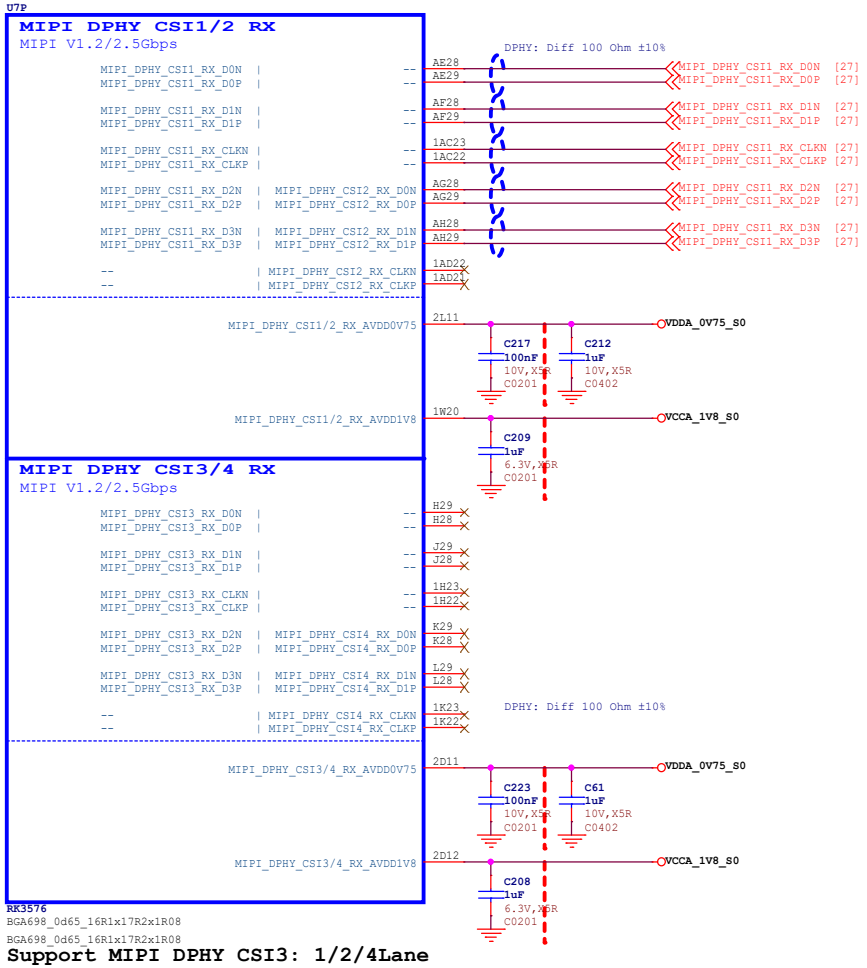
MIPI DPHY CSI0:
Support 1/2/4Lane

Note:
If not used:
Signal: Leave floating
Power : Leave floating

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

Support MIPI DPHY CSI1: 1/2/4Lane
Support MIPI DPHY CSI2: 1/2Lane
Support: MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane



Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI3 2Lane + MIPI DPHY CSI4 2Lane

Note:
If not used:
Signal: Leave floating
Power : Leave floating or tie to VSS

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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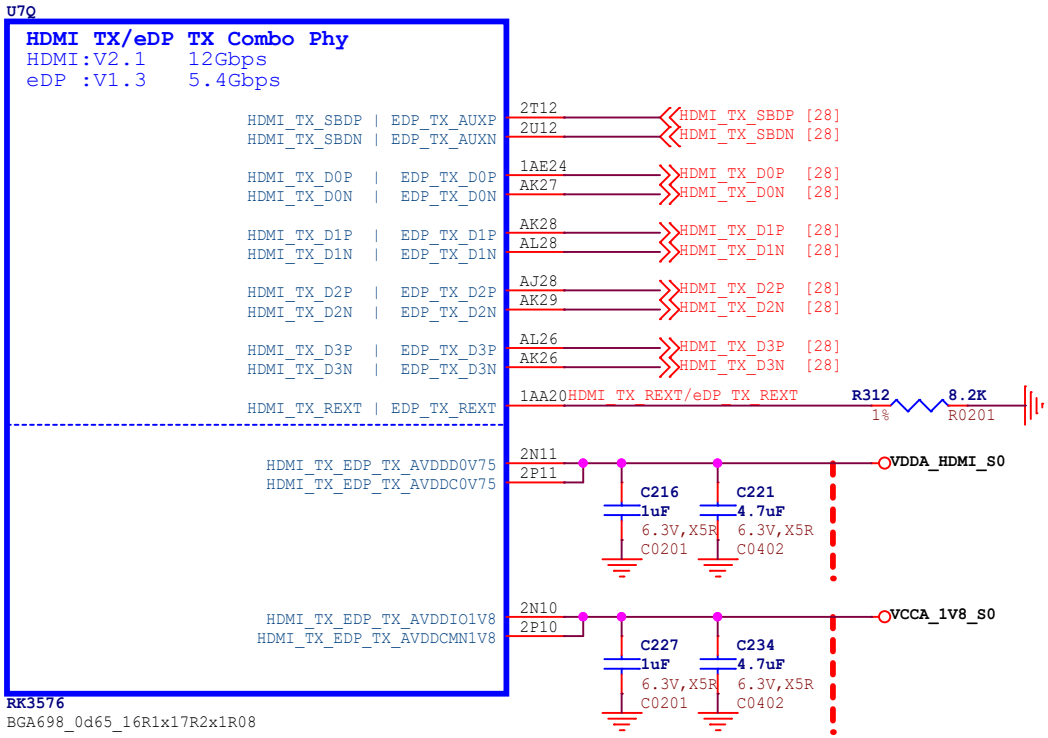
RK3576_Q(HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz



Note:
If not used:
Signal: Leave floating
Power : Leave floating or tie to VSS

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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	Title: RK3576_AIOT_REF_SCH	
Size: A4	Document Number: 14.RK3576-HDMI/eDP	Rev: V1.0
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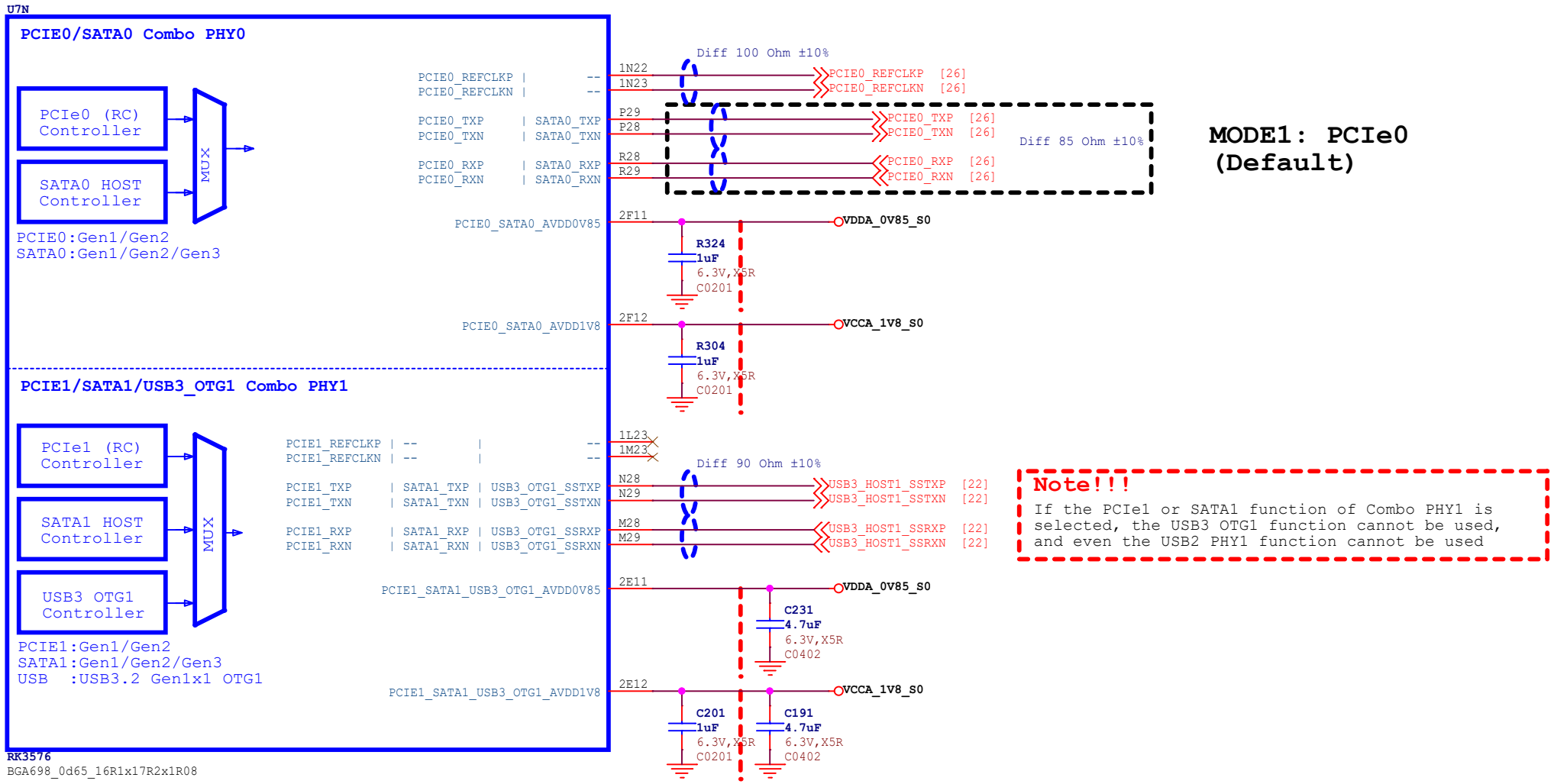
RK3576_N(PCIe/SATA/USB3)



MODE1: PCIe0 (Default)

Note!!!
If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 PHY1 function cannot be used

Note:
If not used:
Signal: Leave floating
Power : Tie to VSS

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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	Title: RK3576_AIOT_REF_SCH	
Size: A4	Document Number: 15.RK3576-PCIe/SATA/USB3	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 15 of 38

RK3576_F(VCCIO2)

U7F

VCCIO2 Domain

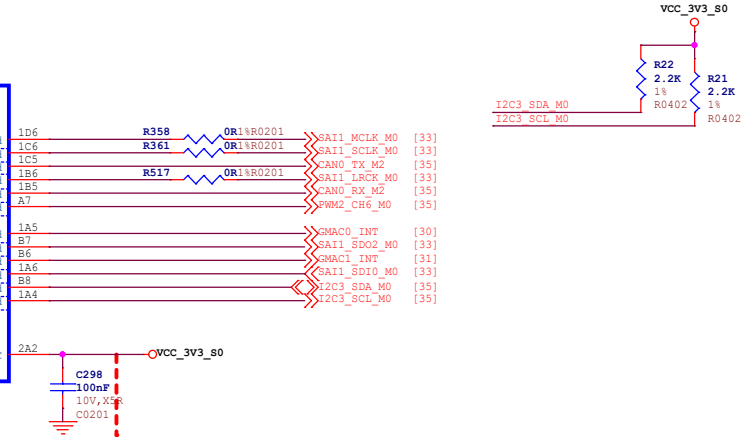
Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d
PWM2_CH4_M1	--	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	--	SAI1_SCLK_M0	GPIO4_A3_d
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	--	GPIO4_A4_d
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	--	SAI1_LRCK_M0	GPIO4_A5_d
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	--	GPIO4_A6_d
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	SAI1_SDO0_M0	GPIO4_A7_d
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d
PWM2_CH7_M0	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d
CAN1_RX_M2	--	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d

RK3576

BGA698_0d65_16R1x17R2x1R08

BGA698_0d65_16R1x17R2x1R08



RK3576_G(VCCIO3)

U7G

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

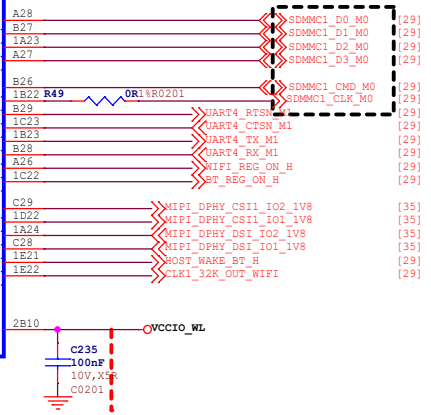
PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d
PWM1_CH1_M1	--	SPI1_MOSI_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d
--	--	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d
--	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_TXCLK_M1	GPIO1_C1_d
PWM1_CH4_M1	--	SPI2_CSN1_M1	I2C6_SCL_M1	UART4_RTSN_M1	--	--	FSPI1_CSN1_M1	FSPI1_RSTN_M1	SDMMC1_PWREN_M0	ETH1_RXCTL_M1	GPIO1_C2_d
--	--	SPI2_CSN0_M1	I2C6_SDA_M1	UART4_CTSN_M1	--	--	--	FSPI1_CSN0_M1	SDMMC1_DETN_M0	ETH1_RXSTRIG_M1	GPIO1_C3_d
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	FSPI1_D0_M1	--	ETH1_RXD0_M1	GPIO1_C4_d
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	FSPI1_D1_M1	--	ETH1_RXD1_M1	GPIO1_C5_d
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	FSPI1_D2_M1	--	ETH1_RXCTL_M1	GPIO1_C6_d
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	FSPI1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	--	--	ETH1_RXD1_M1	GPIO1_D0_d
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	--	--	ETH1_RXCTL_M1	GPIO1_D1_d
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	--	--	ETH1_MDC_M1	GPIO1_D2_d
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	--	--	ETH1_MDIO_M1	GPIO1_D3_d
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	--	--	ETH1_MCLK_M1	GPIO1_D4_d
CLK1_32K_OUT	SATA_MPSWIT	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d

RK3576

BGA698_0d65_16R1x17R2x1R08

BGA698_0d65_16R1x17R2x1R08

MODE1: SDIO WI-FI



RK3576_J(VCCIO6)

U7J

VCCIO6 Domain

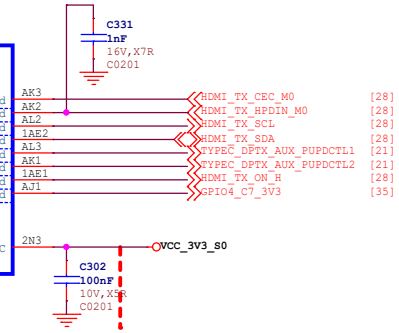
Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	--	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d
PWM0_CH1_M1	UART11_RX_M2	EDP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RF_M1	GPIO4_C2_d
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d
PWM2_CH6_M1	UART6_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d
PWM2_CH5_M1	UART6_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	--	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d

RK3576

BGA698_0d65_16R1x17R2x1R08

BGA698_0d65_16R1x17R2x1R08



Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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	Title: RK3576_AIOT_REF_SCH	
Size: A3	Document Number: 16.RK3576-GPIO VCCIO2/3/6	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 16 of 38

RK3576_H(VCCIO4)

U7H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d	
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d	
--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d	
--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d	
--	--	PCIE0_CLKREQn_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d	
--	--	PCIE1_CLKREQn_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d	
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART7_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d	
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART7_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d	
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d	
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d	
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d	
PWM1_CH1_M2	--	--	SPI1_CSN1_M1	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d	
PWM1_CH2_M2	--	--	SPI1_MOSI_M1	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d	
PWM0_CH0_M2	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_TXD2_M0	VI_CIF_D2	GPIO2_C3_d	
PWM1_CH3_M2	--	--	SPI1_CSN0_M1	UART11_TX_M1	PDM1_SDO_M0	SAI2_SDO_M1	--	ETH1_TXD3_M0	VI_CIF_D1	GPIO2_C4_d	
PWM1_CH4_M2	--	--	SPI1_CLK_M1	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_RXCLK_M0	VI_CIF_D0	GPIO2_C5_d	
PWM0_CH4_M2	--	I2C5_SCL_M2	--	UART4_CTSN_M0	--	SAI4_SCLK_M3	--	ETH1_TXD0_M0	--	GPIO2_C6_d	
PWM0_CH5_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI4_LRCK_M3	--	ETH1_TXD1_M0	--	GPIO2_C7_d	
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d	
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d	
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLKU_OUT_M1	GPIO2_D2_d	
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d	
PWM2_CH4_M2	--	I2C9_SDA_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	ISP_PRELIGHT_TRIG_M0	GPIO2_D4_d	
PWM2_CH5_M2	--	I2C9_SCL_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	ISP_FLASH_TRIGOUT_M0	GPIO2_D5_d	
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH_CLK1_25M_OUT_M0	CAM_CLK1_OUT_M1	GPIO2_D6_d	
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI3_SDO3_M0	ETH_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLK2_OUT_M1	GPIO2_D7_d	
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d	
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d	
--	MIPI_TE_M1	CAN1_TX_M3	SPI3_MISO_M0	UART3_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d	
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART3_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLKI	GPIO3_A3_d	

RK3576

BGA698_0d65_16R1x17R2x1R08

BGA698_0d65_16R1x17R2x1R08

B22 — HP_CTL_H [33]
B20 — VSYS_3V3_EXP_EN [18]

B19 — GPIO2_B1_3V3 [35]
1A18 — PCIE0_PERSTn [26]
1A17 — PCIE0_CLKREQn_M0 [26]
1B16 — GMAC0_RSTn [30]
A19 — GMAC1_RSTn [31]
1C18 — GPIO2_B5_3V3 [35]
A21 — USB_OTG0_PWREN_H [21]
B21 — HP_DET_L [33]

A17 — GMAC1_RXD2_M0 [31]
1A15 — GMAC1_RXD3_M0 [31]
1D15 — GMAC1_RXCLK_M0 [31]
A15 — R83 — 0R1%R0201 — GMAC1_TXD2_M0 [31]
1A13 — R81 — 0R1%R0201 — GMAC1_TXD3_M0 [31]
1C15 — R334 — 0R1%R0201 — GMAC1_TXCLK_M0 [31]
1A14 — R82 — 0R1%R0201 — GMAC1_TXD0_M0 [31]
B15 — R78 — 0R1%R0201 — GMAC1_TXD1_M0 [31]

B16 — R75 — 0R1%R0201 — GMAC1_TXCTL_M0 [31]
1A16 — GMAC1_RXD0_M0 [31]
B17 — GMAC1_RXD1_M0 [31]
B18 — GMAC1_RXCTL_M0 [31]
1B13 — R338 — 0R1%R0201 — GMAC1_MDC_M0 [31]
1B15 — GMAC1_MDIO_M0 [31]
1D18 — R322 — 0R1%R0201 — ETH_CLK1_25M_OUT_M0 [31]
1E15 — R332 — 0R1%R0201 — GMAC1_MCLKINOUT_M0 [31]

1D16 — I2C7_SCL_M1_Sensor [27]
1B18 — I2C7_SDA_M1_Sensor [27]
1A20 — CAN1_TX_M3 [35]
1A19 — CAN1_RX_M3 [35]

VCC_3V3_S0
R378 2.2K 1% R0402 — R380 2.2K 1% R0402
I2C7_SCL_M1_Sensor
I2C7_SDA_M1_Sensor

MODE1: RGMII1(Default)

VCCIO4_VCC — 2A7
C261 100nF 10V,X5R C0201 DNP
C260 1uF 6.3V,X5R C0201
VCC_3V3_S0

RK3576_I(VCCIO5)

U7I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d	
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GSSE	VO_LCDC_D22	GPIO3_A5_d	
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GSOE	VO_LCDC_D21	GPIO3_A6_d	
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d	
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d	
PWM1_CH3_M3	--	SPI4_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d	
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d	
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d	
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDOI5	VO_LCDC_D15	GPIO3_B4_d	
PWM1_CH5_M3	--	--	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDOI4	VO_LCDC_D14	GPIO3_B5_d	
PWM0_CH1_M3	--	SPI3_CSN0_M1	--	--	--	FLEXBUS0_CLK	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDOI3	VO_LCDC_D13	GPIO3_B6_d	
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDOI2	VO_LCDC_D12	GPIO3_B7_d	
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDOI1	VO_LCDC_D11	GPIO3_C0_d	
CAN0_RX_M3	I2C5_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO2_M1	ETH0_PPS_REFCLK_M0	VO_EBC_SDDOI0	VO_LCDC_D10	GPIO3_C1_d	
PWM2_CH0_M3	I2C9_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D7	DSMC_INT1	SAI2_SCLK_M2	ETH0_RXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d	
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS1_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_RXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d	
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA5	SAI1_SDO1_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d	
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D6	DSMC_DATA4	SAI1_SDO0_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d	
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d	
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d	
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d	
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS1_D11	DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d	
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART2_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS0_D12	DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d	
PWM2_CH5_M3	I3C1_SCL_M2	--	UART2_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d	
--	I2C3_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d	
--	I2C3_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKP	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d	
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d	
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS1_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d	
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d	
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS0_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d	

RK3576

BGA698_0d65_16R1x17R2x1R08

BGA698_0d65_16R1x17R2x1R08

1D13 GPIO3_A4 — R342 — 0R1%R0201 — ETH_CLK0_25M_OUT_M0 [30]
A9 — GMAC0_MDIO_M0 [30]
1A7 GPIO3_A6 — R98 — 0R1%R0201 — GMAC0_MDC_M0 [30]
B13 — GMAC0_RXCTL_M0 [30]

B14 — PWM0_CH0_M3 [37]
1A11 — GMAC0_RXD1_M0 [30]
A13 — GMAC0_RXD0_M0 [30]
A11 GPIO3_B3 — R92 — 0R1%R0201 — GMAC0_TXCTL_M0 [30]
B10 GPIO3_B4 — R93 — 0R1%R0201 — GMAC0_TXD1_M0 [30]
1A9 GPIO3_B5 — R86 — 0R1%R0201 — GMAC0_TXD0_M0 [30]
B11 GPIO3_B6 — R89 — 0R1%R0201 — GMAC0_TXCLK_M0 [30]
1D12 — I2C4_SDA_M3_EEPROM [25,35]

1E9 — I2C4_SCL_M3_EEPROM [25,35]
1B10 — GPIO3_C1_1V8 [35]
B9 GPIO3_C2 — R95 — 0R1%R0201 — GMAC0_TXD3_M0 [30]
1A8 GPIO3_C3 — R88 — 0R1%R0201 — GMAC0_TXD2_M0 [30]
1D9 — GPIO3_C4_1V8 [35]
1B9 — FAN_TACH [37]
1D7 — I2C3_INT_GPIO3C6_1V8 [35]
1C7 — MIPI_DPHY_CSI0_IO2_1V8 [35]

1C12 — PCIe_SX1261_BUSY_1V8 [38]
1A12 — GMAC0_RXCLK_M0 [30]
1A10 — GMAC0_RXD3_M0 [30]
B12 — GMAC0_RXD2_M0 [30]
1E12 — SPI3_CLK_M1_1V8 [35]
1D10 — SPI3_MISO_M1_1V8 [35]
1C10 — SPI3_MOSI_M1_1V8 [35]
1E7 — SPI3_CSN1_M1_1V8 [35]

1B12 — UART3_TX_M1_1V8 [35]
1B7 — UART3_RX_M1_1V8 [35]

VCCIO5_VCC_0
VCCIO5_VCC_1
2A4
2A5
C274 100nF 10V,X5R C0201 DNP
C287 1uF 6.3V,X5R C0201
VCC_1V8_S0

VCC_1V8_S0
DNP R45 10K 1% R0201
DNP R46 10K 1% R0201
I2C4_SDA_M3_EEPROM
I2C4_SCL_M3_EEPROM

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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Title: RK3576_AIOT_REF_SCH

Size:	Document Number:	Rev:
A3	17.RK3576-GPIO VCCIO4/5	V1.0

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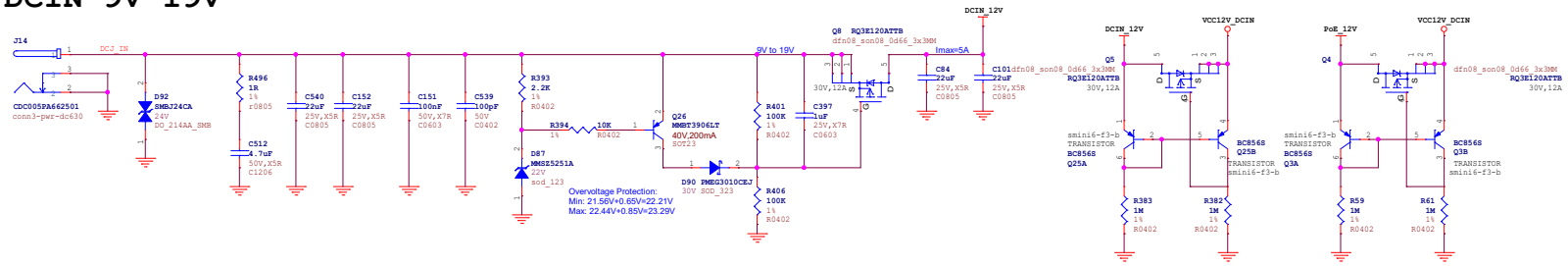
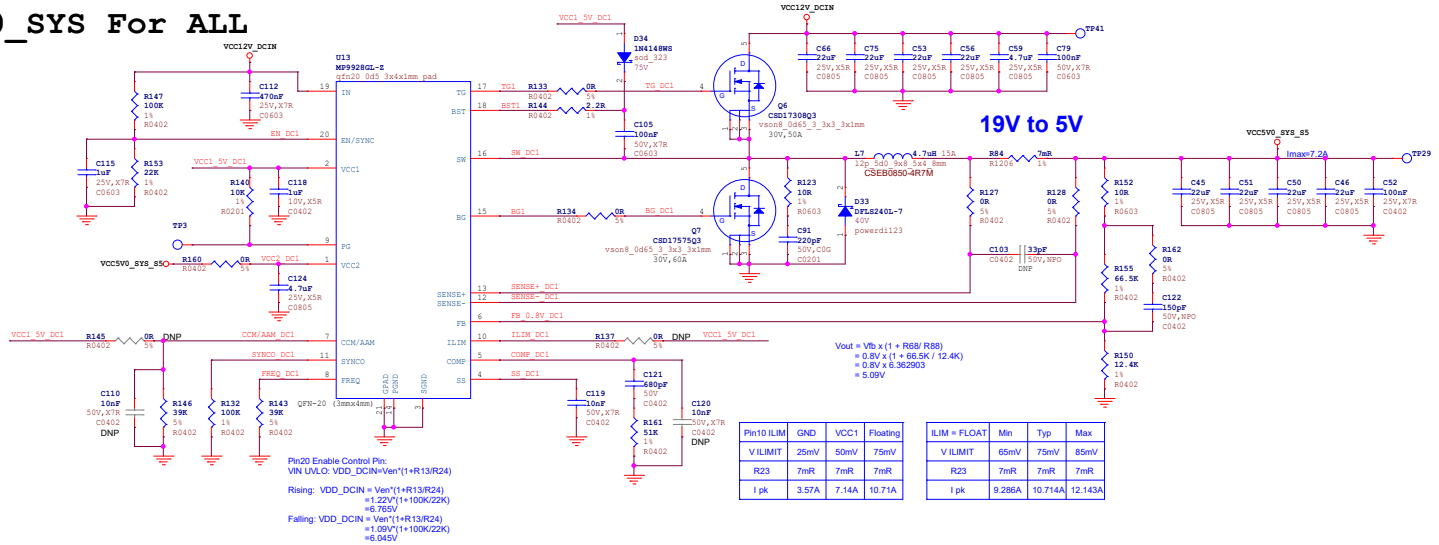
DCIN-9V-19V



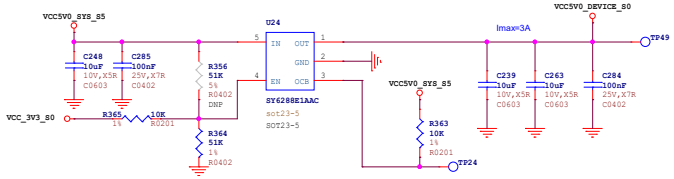
VCC5V0_SYS For ALL



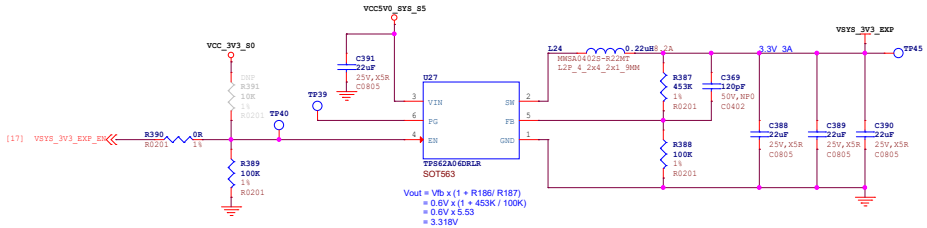
Pin10 ILIM	GND	VCC1	Floating
V ILIMIT	25mV	50mV	75mV
R23	7mR	7mR	7mR
I pk	3.57A	7.14A	10.71A

ILIM = FLOAT	Min	Typ	Max
V ILIMIT	65mV	75mV	85mV
R23	7mR	7mR	7mR
I pk	9.286A	10.714A	12.143A

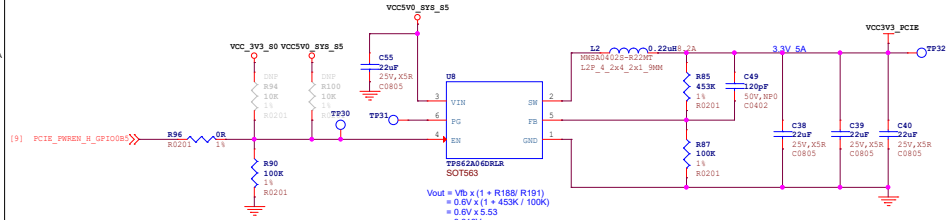
VCC5V0_DEVICE_S0 For FAN & HDMI & USB & TYPE-C (Total: 3A)



VSYS_3V3_EXP For CSI & DSI & RPi 40Pin (Total: 4A)



VCC3V3_PCIE For PCIE-M.2



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Title:	RK3576_AIOT_REF_SCH
Size: A2	Document Number: 18.Power-DC IN
Rev:	V1.0
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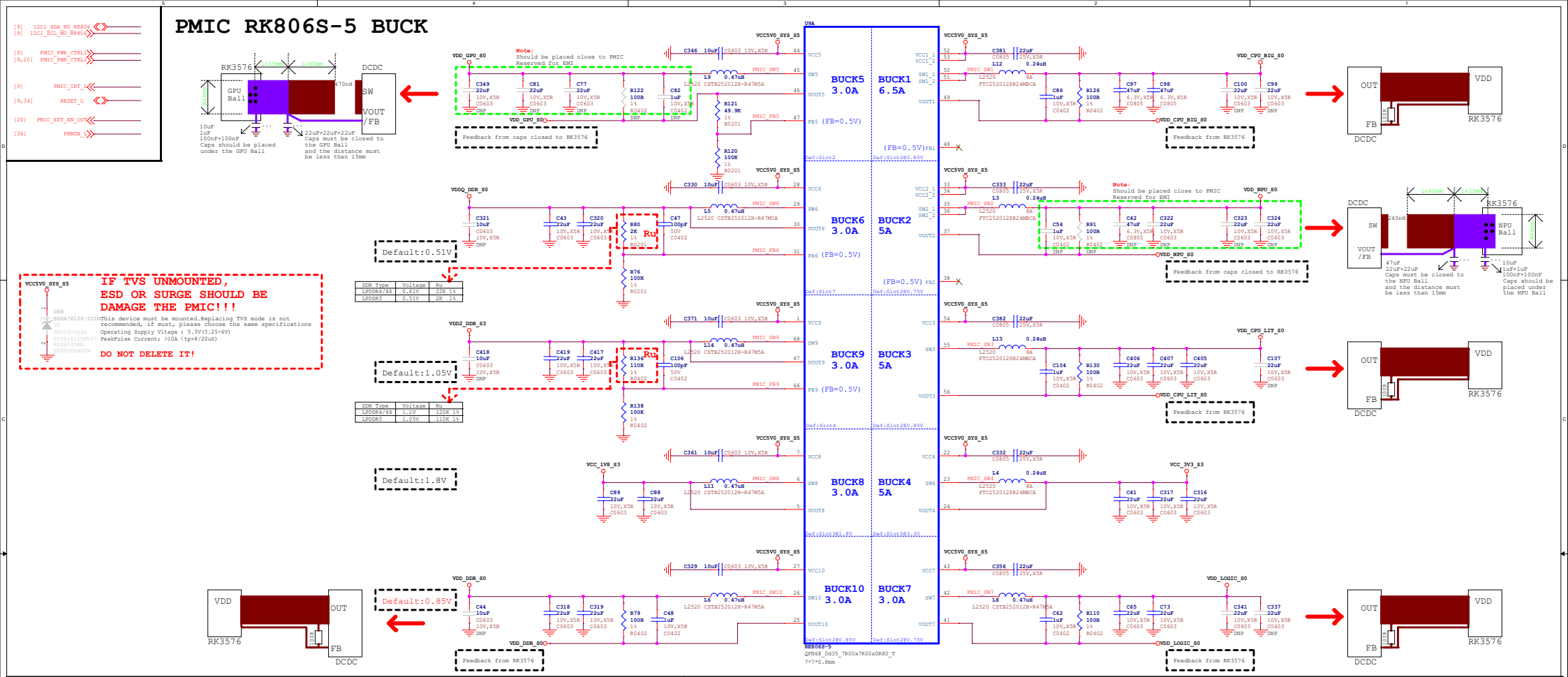
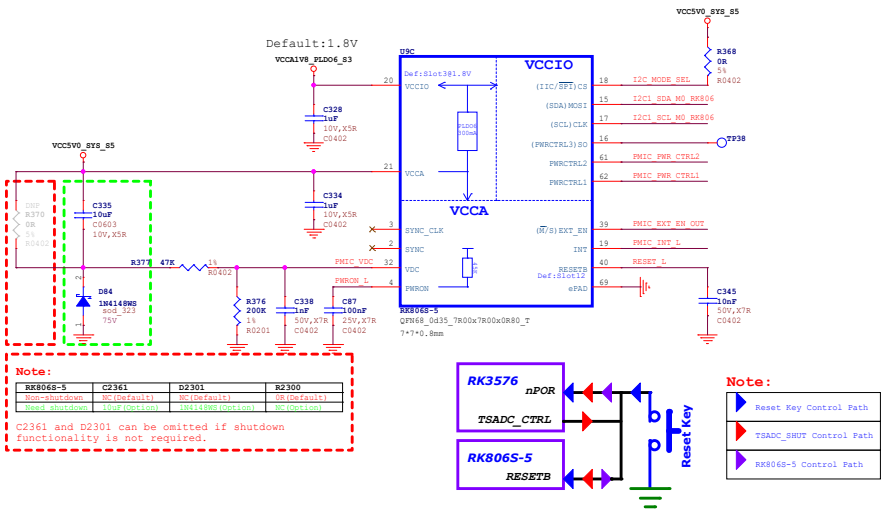
PMIC RK806S-5 BUCK



PMIC RK806S-5 Managerment



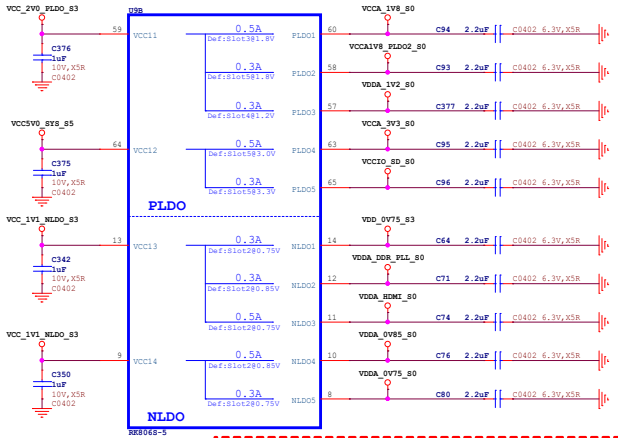
Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND

RK806S-5	C2361	D2301	R2300
Non-shutdown	NC(Default)	NC(Default)	0R(Default)
Need shutdown	10uF(Option)	1N4148WS(Option)	NC(Option)

C2361 and D2301 can be omitted if shutdown functionality is not required.

Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806S-5 Control Path

PMIC RK806S-5 LDO



This power supply needs to be adjusted from 0.75V to 0.8375V after power on !

Note:
The RK806S-5 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

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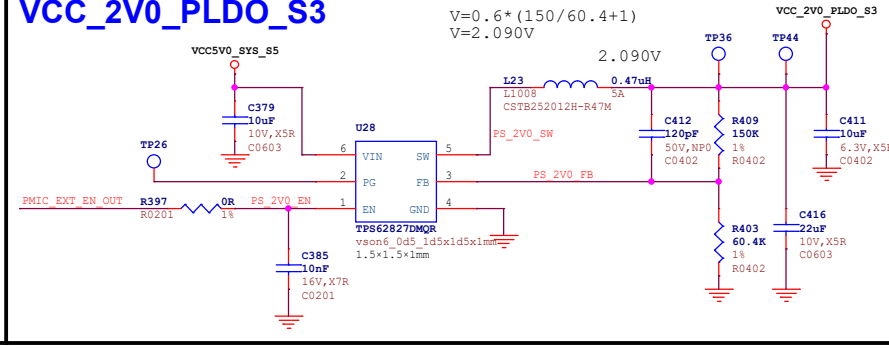
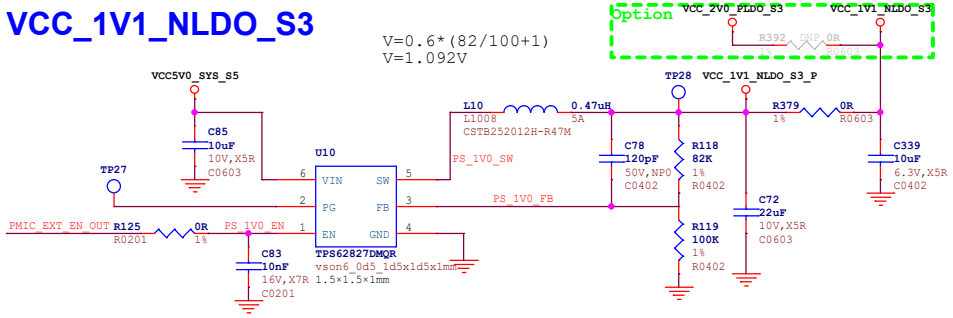
	Title: RK3576_AIOT_REF_SCH		
Size: A2	Document Number: 19.Power-PMIC RK806S-5		Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 19 of 38	

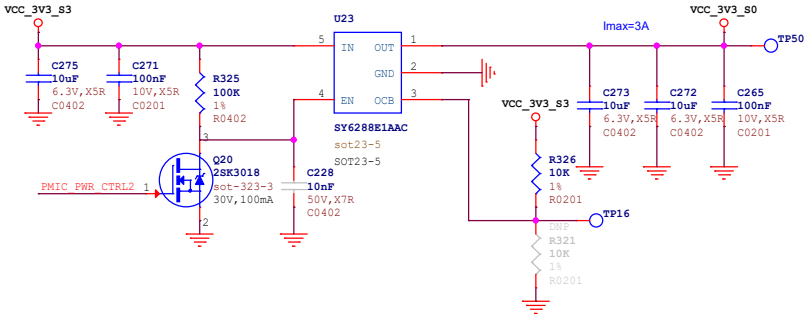
VCC_2V0_PLDO_S3



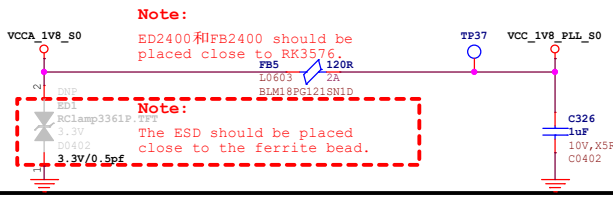
VCC_1V1_NLDO_S3



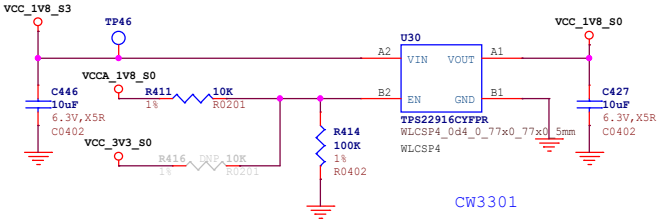
VCC_3V3_S0



VCC_1V8_PLL_S0

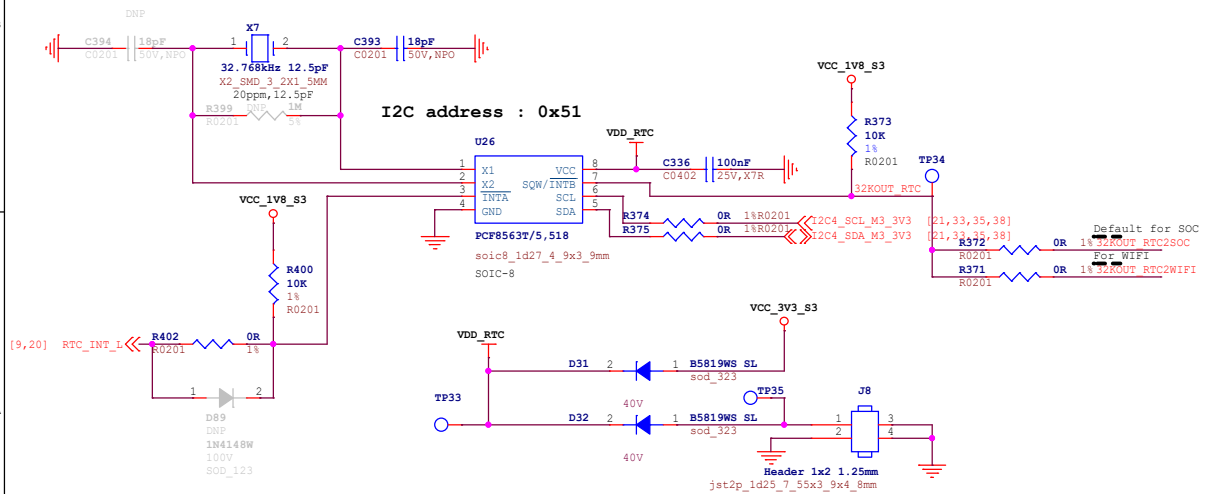


VCC_1V8_S0

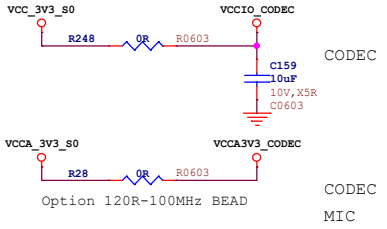


RTC

RTC IC



Audio Power



WIFI/BT Power

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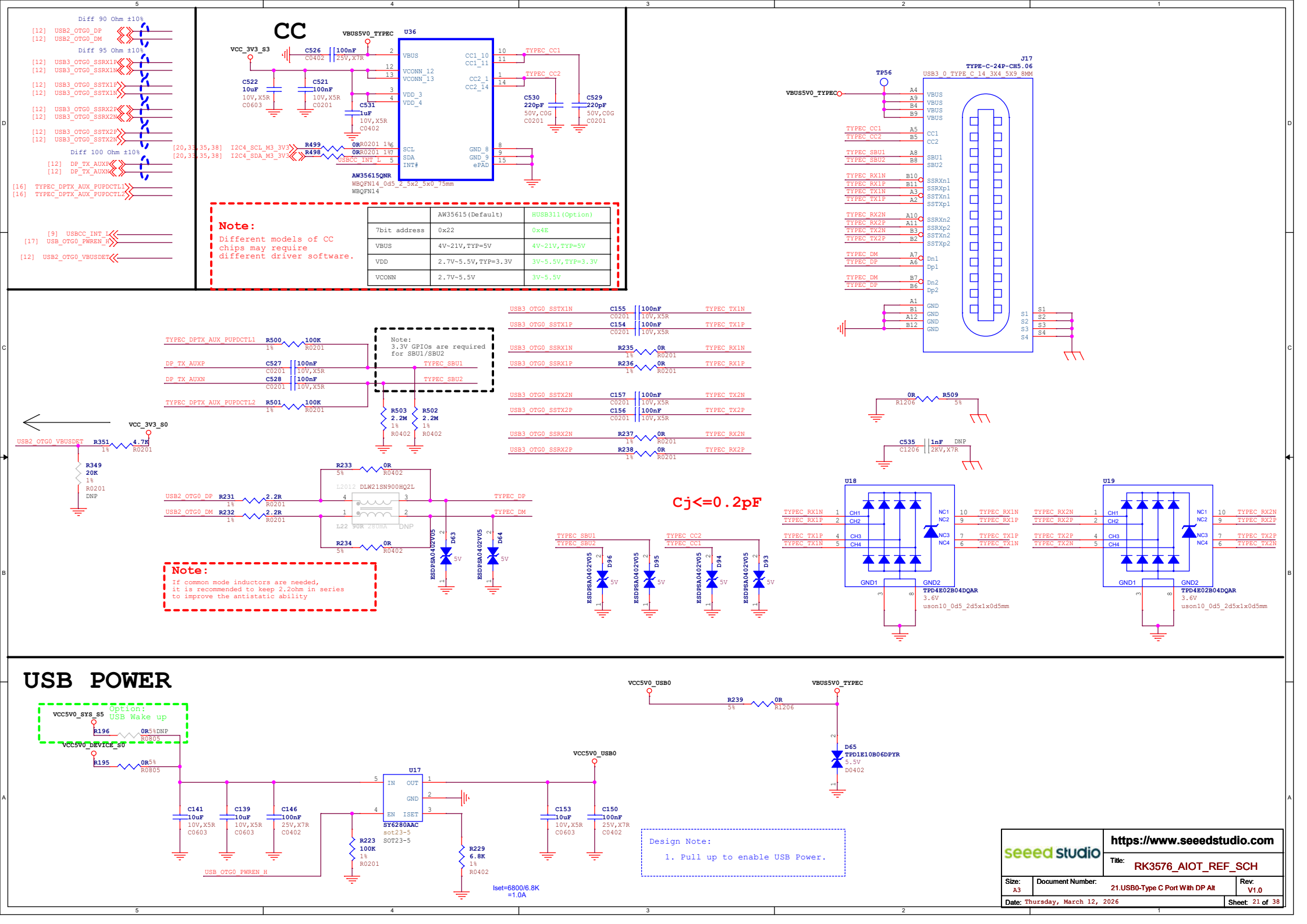
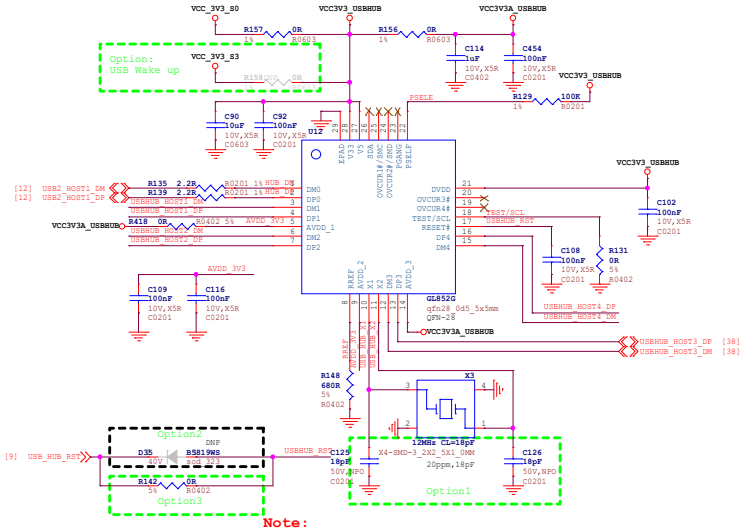
	Title: RK3576_AIOT_REF_SCH	
Size: A3	Document Number: 20.Power-Ext Discrete/RTC IC	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 20 of 38


CC
Diff 90 Ohm ±10%
[12] USB2_OTG0_DP
[12] USB2_OTG0_DM
Diff 95 Ohm ±10%
[12] USB3_OTG0_SSRX1P
[12] USB3_OTG0_SSRX1N
[12] USB3_OTG0_SSTX1P
[12] USB3_OTG0_SSTX1N
[12] USB3_OTG0_SSRX2P
[12] USB3_OTG0_SSRX2N
[12] USB3_OTG0_SSTX2P
[12] USB3_OTG0_SSTX2N
Diff 100 Ohm ±10%
[12] DP_TX_AUXP
[12] DP_TX_AUXN
[16] TYPEC_DPTX_AUX_PUPDCTL1
[16] TYPEC_DPTX_AUX_PUPDCTL2
[9] USBCC_INT_L
[17] USB_OTG0_PWREN_H
[12] USB2_OTG0_VBUSDET
VCC_3V3_S3
VBUS5V0_TYPEC
U36
AW35615QNR
WBQFN14_0d5_2_5x2_5x0_75mm
WBQFN14
C526 100nF 25V,X7R C0402
C522 10uF 10V,X5R C0603
C521 100nF 10V,X5R C0201
C531 1uF 10V,X5R C0402
C530 220pF 50V,C0G C0201
C529 220pF 50V,C0G C0201
R499 0R R0201 1%
R498 0R R0201 1%
[20,33,35,38] I2C4_SCL_M3_3V3
[20,33,35,38] I2C4_SDA_M3_3V3
USBCC_INT_L
TYPEC_CC1
TYPEC_CC2
VBUS
VCONN_12
VCONN_13
VDD_3
VDD_4
SCL
SDA
INT#
CC1_10
CC1_11
CC2_1
CC2_14
GND_8
GND_9
ePAD
Note:
Different models of CC chips may require different driver software.
AW35615(Default)
HUSB311(Option)
7bit address
0x22
0x4E
VBUS
4V~21V,TYP=5V
4V~21V,TYP=5V
VDD
2.7V~5.5V,TYP=3.3V
3V~5.5V,TYP=3.3V
VCONN
2.7V~5.5V
3V~5.5V
J17
TYPE-C-24P-CH5.06
USB3_0_TYPE_C_14_3X4_5X9_8MM
TP56
VBUS5V0_TYPEC
TYPEC_CC1
TYPEC_CC2
TYPEC_SBU1
TYPEC_SBU2
TYPEC_RX1N
TYPEC_RX1P
TYPEC_TX1N
TYPEC_TX1P
TYPEC_RX2N
TYPEC_RX2P
TYPEC_TX2N
TYPEC_TX2P
TYPEC_DM
TYPEC_DP
VBUS
CC1
CC2
SBU1
SBU2
SSRXn1
SSRXp1
SSTXn1
SSTXp1
SSRXn2
SSRXp2
SSTXn2
SSTXp2
Dn1
Dp1
Dn2
Dp2
GND
S1
S2
S3
S4
TYPEC_DPTX_AUX_PUPDCTL1
TYPEC_DPTX_AUX_PUPDCTL2
DP_TX_AUXP
DP_TX_AUXN
R500 100K 1% R0201
R501 100K 1% R0201
C527 100nF 10V,X5R C0201
C528 100nF 10V,X5R C0201
Note:
3.3V GPIOs are required for SBU1/SBU2
TYPEC_SBU1
TYPEC_SBU2
R503 2.2M 1% R0402
R502 2.2M 1% R0402
USB3_OTG0_SSTX1N
USB3_OTG0_SSTX1P
USB3_OTG0_SSRX1N
USB3_OTG0_SSRX1P
USB3_OTG0_SSTX2N
USB3_OTG0_SSTX2P
USB3_OTG0_SSRX2N
USB3_OTG0_SSRX2P
C155 100nF C0201 10V,X5R
C154 100nF C0201 10V,X5R
C157 100nF C0201 10V,X5R
C156 100nF C0201 10V,X5R
R235 0R 1% R0201
R236 0R 1% R0201
R237 0R 1% R0201
R238 0R 1% R0201
TYPEC_TX1N
TYPEC_TX1P
TYPEC_RX1N
TYPEC_RX1P
TYPEC_TX2N
TYPEC_TX2P
TYPEC_RX2N
TYPEC_RX2P
R509 0R R1206 5%
C535 1nF 2KV,X7R C1206 DNP
VCC_3V3_S0
USB2_OTG0_VBUSDET
R351 4.7K 1% R0201
R349 20K 1% R0201 DNP
R233 0R 5% R0402
R234 0R 5% R0402
L2012 DLW21SN900HQ2L
L22 90R 280mA DNP
USB2_OTG0_DP
USB2_OTG0_DM
R231 2.2R 1% R0201
R232 2.2R 1% R0201
TYPEC_DP
TYPEC_DM
ESDPSA0402V05
D63
D64
D96
D95
D94
D93
5V
Cj<=0.2pF
U18
U19
NC1
NC2
NC3
NC4
CH1
CH2
CH3
CH4
GND1
GND2
TPD4E02B04DQAR
3.6V
uson10_0d5_2d5x1x0d5mm
Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability
USB POWER
VCC5V0_SYS_S5
Option:
USB Wake up
R196 0R 5% DNP R0805
VCC5V0_DEVICE_S0
R195 0R 5% R0805
U17
SY6280AAC
sot23-5
SOT23-5
IN
OUT
GND
EN
ISET
C141 10uF 10V,X5R C0603
C139 10uF 10V,X5R C0603
C146 100nF 25V,X7R C0402
C153 10uF 10V,X5R C0603
C150 100nF 25V,X7R C0402
R223 100K 1% R0201
R229 6.8K 1% R0402
Iset=6800/6.8K
=1.0A
USB_OTG0_PWREN_H
VCC5V0_USB0
VBUS5V0_TYPEC
R239 0R 5% R1206
D65
TPD1E10B06DPYR
5.5V
D0402
Design Note:
1. Pull up to enable USB Power.
seeed studio
https://www.seeedstudio.com
Title: RK3576_AIOT_REF_SCH
Size: A3
Document Number: 21.USB0-Type C Port With DP Alt
Rev: V1.0
Date: Thursday, March 12, 2026
Sheet: 21 of 38

USB20_HUB+USB3.0 HOST

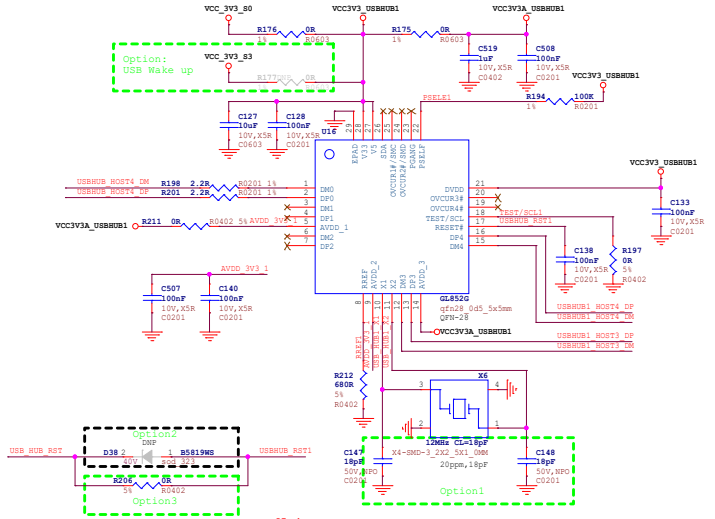


Note:

Yes: option circuit be mounted
No: option circuit not be mounted

OPTION	Option1	Option2	Option3
CH334H	NO	Yes	NO
GL852G	Yes	NO	Yes

USB20_HUB+USB3.0 HOST1

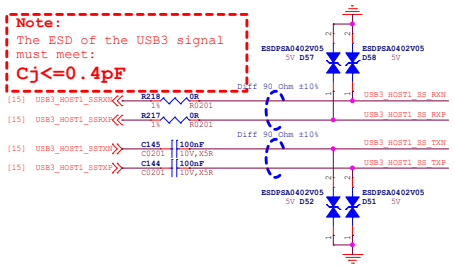


Note:

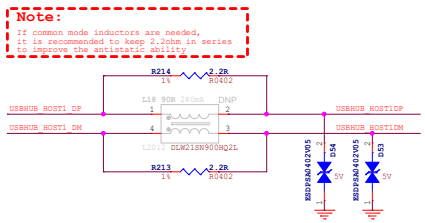
Yes: option circuit be mounted
No: option circuit not be mounted

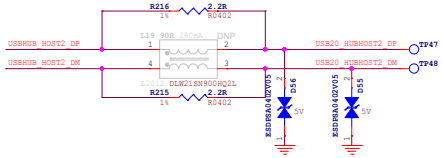
OPTION	Option1	Option2	Option3
CH334H	NO	Yes	NO
GL852G	Yes	NO	Yes

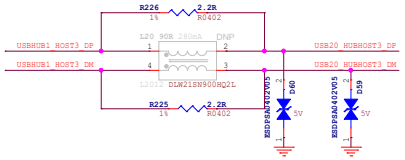
Note:
The ESD of the USB3 signal must meet:
Cj<=0.4pF

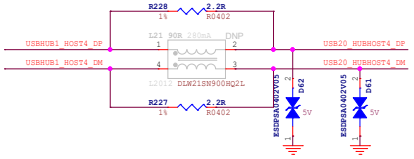


Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability

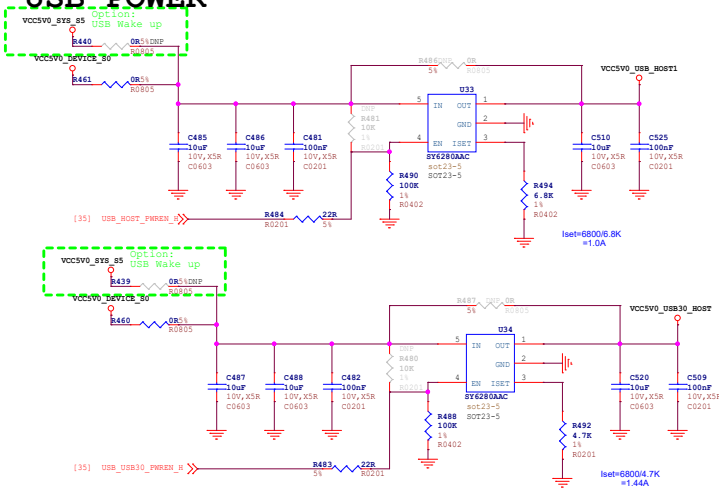


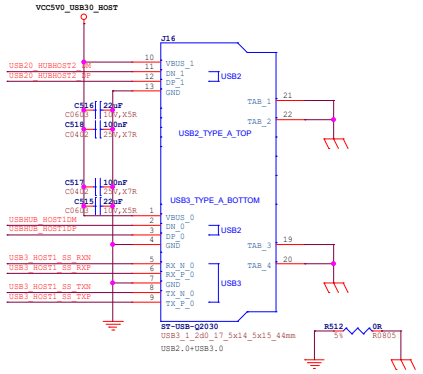




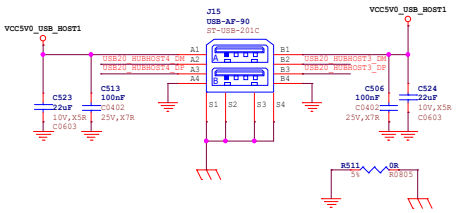


USB_POWER



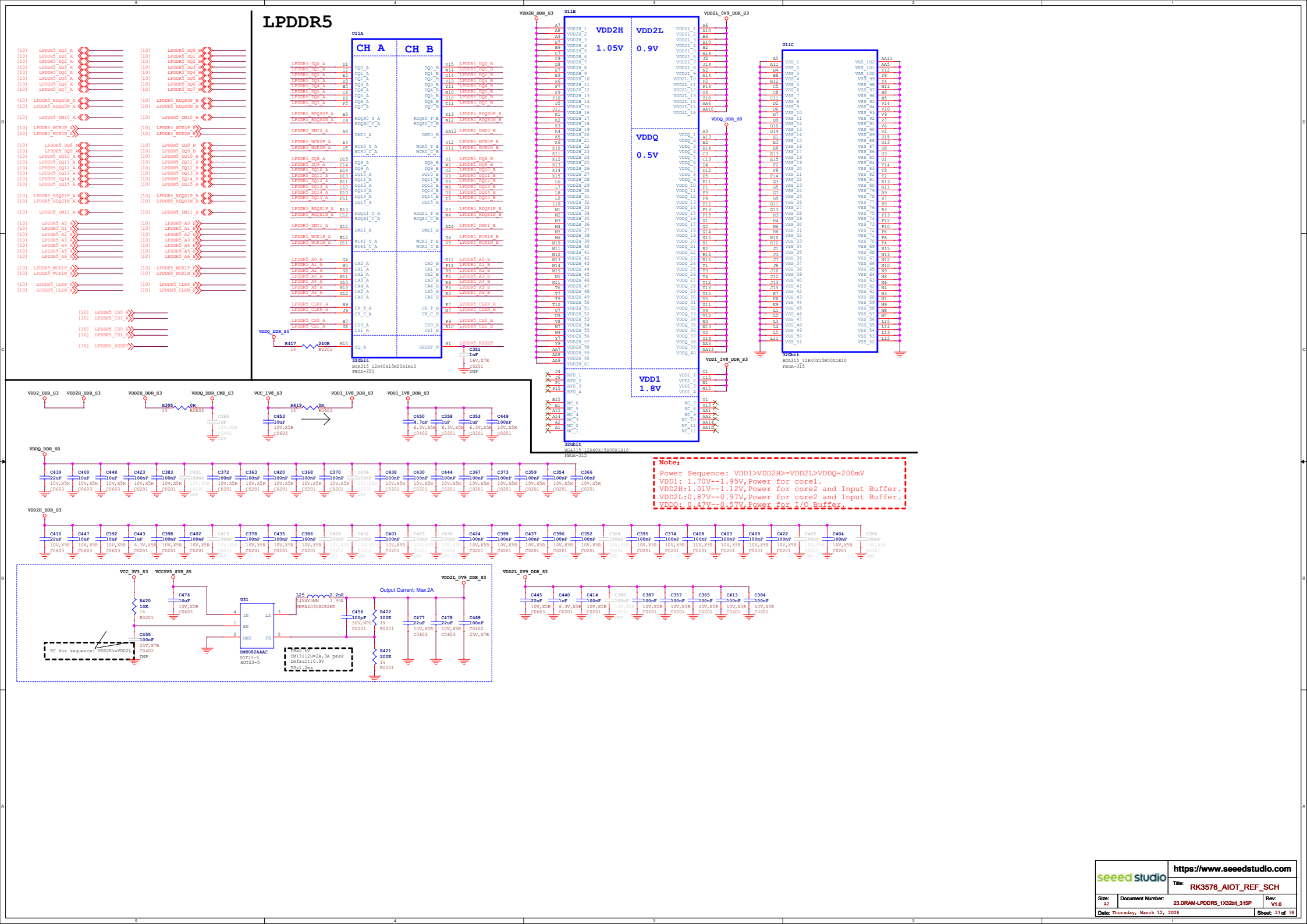


DOUBLE_USB2.0_HOST



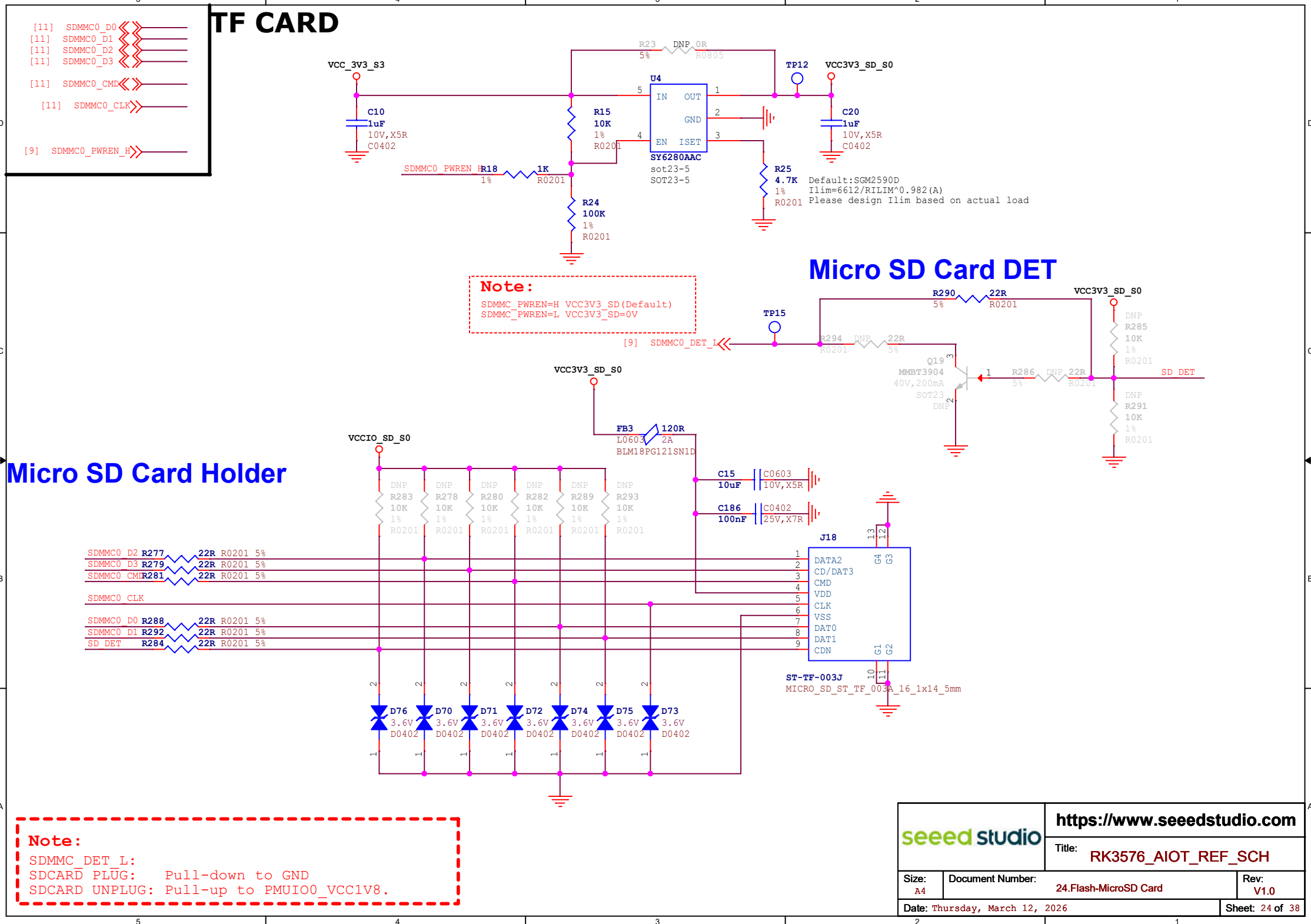
seeed studio	https://www.seeedstudio.com		
	Title: RK3576_AIOT_REF_SCH		
Size: A2	Document Number: 22.USB1-USB20_HUB+USB3.0 HOST	Rev: V1.0	
Date: Thursday, March 12, 2026		Sheet: 22 of 38	

LPDDR5



seeed studio	https://www.seeedstudio.com
Title:	RK3576_AIOT_REF_SCH
Size: A2	Document Number: 23.DRAM-LPDDR5_1X32bit_315P
Rev:	V1.0
Date: Thursday, March 12, 2026	Sheet: 23 of 38

TF CARD



seeed studio	https://www.seeedstudio.com	
	Title: RK3576_AIOT_REF_SCH	
Size: A4	Document Number: 24.Flash-MicroSD Card	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 24 of 38

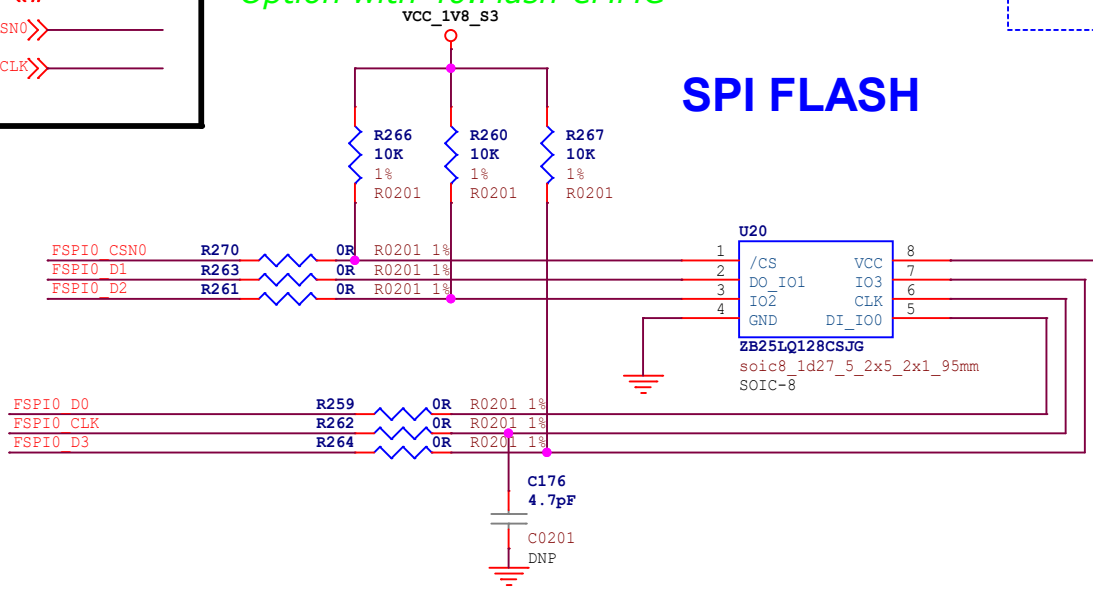
[11] FSPI0_D0
[11] FSPI0_D1
[11] FSPI0_D2
[11] FSPI0_D3
[11] FSPI0_CSN0
[11] FSPI0_CLK

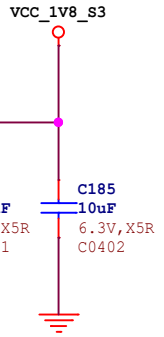
FSPI0 Flash

Option with 40.Flash-eMMC

Layout Note:
1. SPI signals require equal length design and Complete plane.

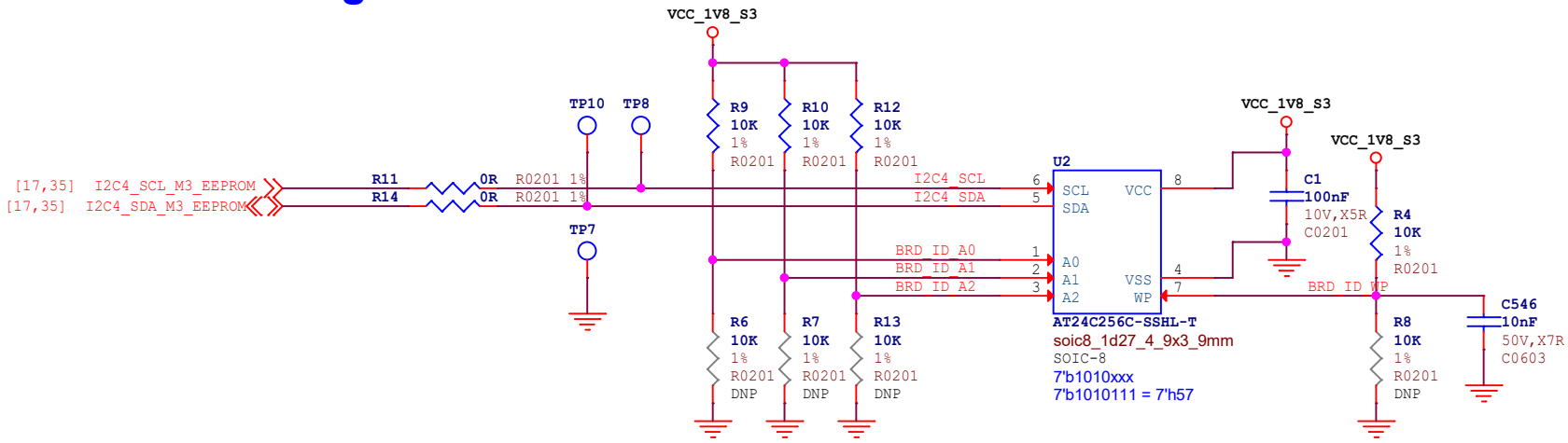
SPI FLASH

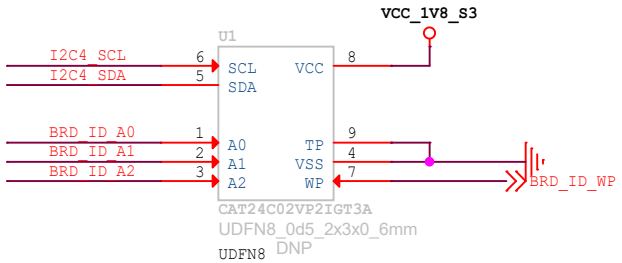




Design Note:
1. VCCIO_FLASH Default : 1.8V
2. Use to store bootloader.

Carrier Board Config



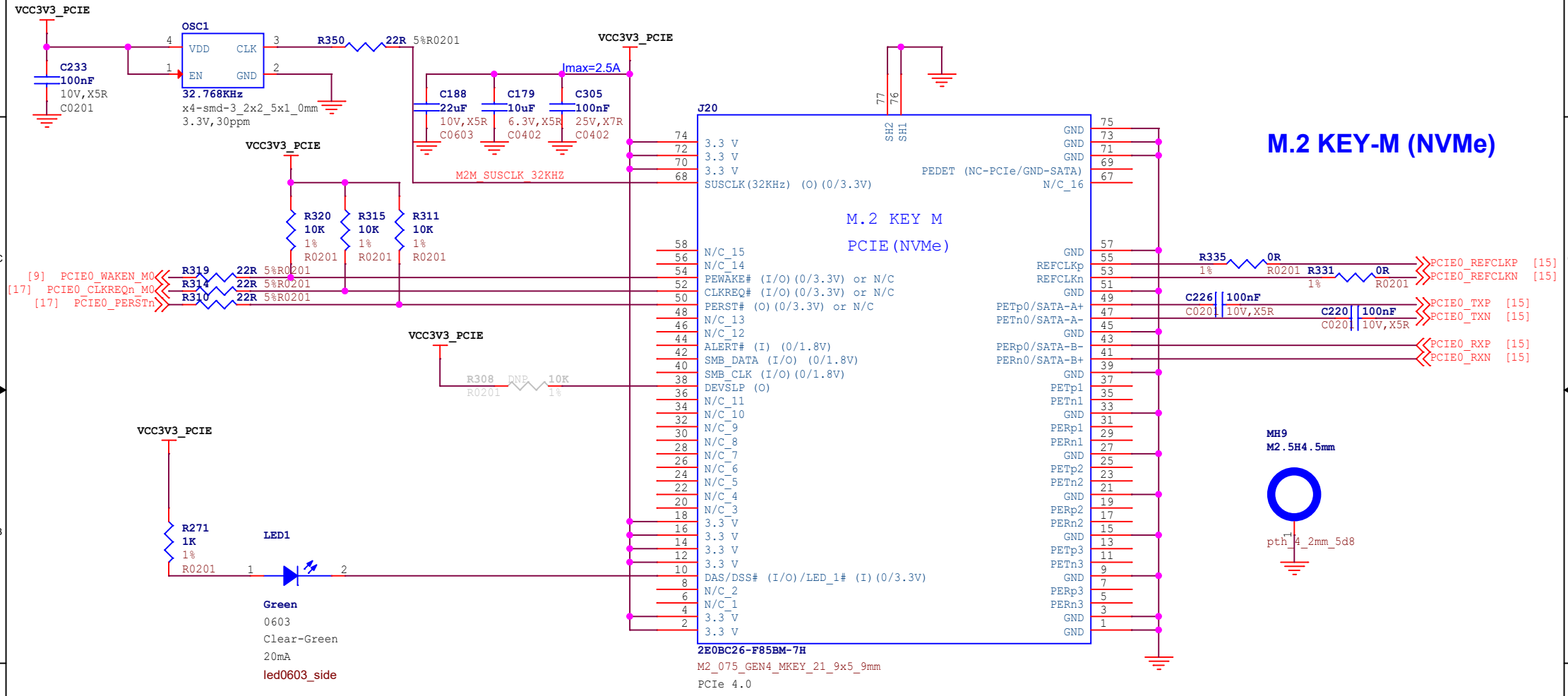


seeed studio

https://www.seeedstudio.com

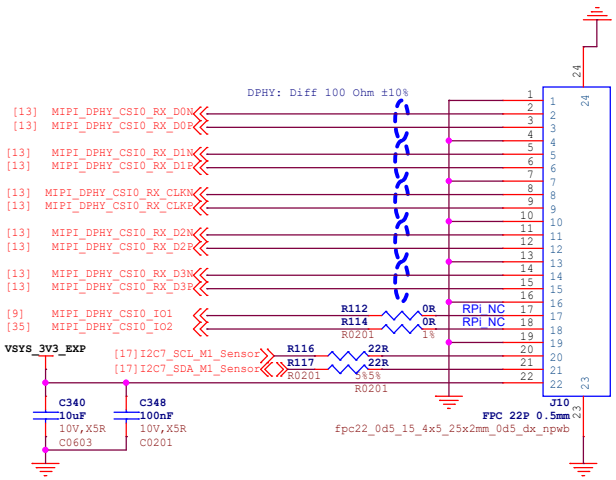
Title: RK3576_AIOT_REF_SCH

Size: A4	Document Number: 25.Flash-SPI Flash&EEPROM	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 25 of 38

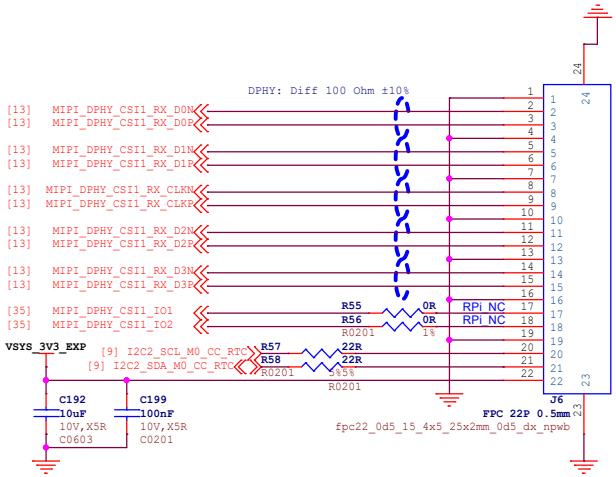


seeed studio	https://www.seeedstudio.com	
	Title: RK3576_AIOT_REF_SCH	
Size: A4	Document Number: 26.M.2 KEY M(NVME)	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 26 of 38

CAM0: VI-CAM MIPI DPHY CSI0 RX

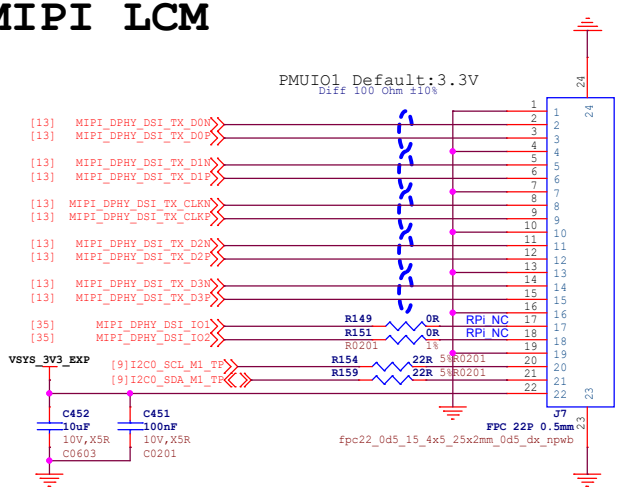


CAM1: VI-CAM MIPI DPHY CSI1/2 RX



Close to FPC Connector

MIPI LCM



seeed studio	https://www.seeedstudio.com	
	Title: RK3576_AIOT_REF_SCH	
Size: A3	Document Number: 27.CAM MIPI CSI0&CSI1 RX&DSI	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 27 of 38

HDMI 2.1

Support video output up to 4Kx2K@120Hz

Diff 100 Ohm ±10%

[14] HDMI_TX_SBDP
[14] HDMI_TX_SBDN
[14] HDMI_TX_D0P
[14] HDMI_TX_D0N
[14] HDMI_TX_D1P
[14] HDMI_TX_D1N
[14] HDMI_TX_D2P
[14] HDMI_TX_D2N
[14] HDMI_TX_D3P
[14] HDMI_TX_D3N
[16] HDMI_TX_SDA
[16] HDMI_TX_SCL
[16] HDMI_TX_CEC_M0
[16] HDMI_TX_HPDIN_M0
[16] HDMI_TX_ON_H

Note:
Close to HDMI Connector

HDMI_TX_D0P — C503 220nF C0201 10V,X5R
HDMI_TX_D0N — C502 220nF C0201 10V,X5R
HDMI_TX_D1P — C505 220nF C0201 10V,X5R
HDMI_TX_D1N — C504 220nF C0201 10V,X5R
HDMI_TX_D2P — C514 220nF C0201 10V,X5R
HDMI_TX_D2N — C511 220nF C0201 10V,X5R
HDMI_TX_D3P — C499 220nF C0201 10V,X5R
HDMI_TX_D3N — C492 220nF C0201 10V,X5R
Diff 100 Ohm ±10%

Note:
Close to HDMI Connector

Default

HDMI_TX0P / HDMI_TX0N
HDMI_TX1P / HDMI_TX1N
HDMI_TX2P / HDMI_TX2N
HDMI_TX3P / HDMI_TX3N

R479 590R 1% R0201
R482 590R 1% R0201
R495 590R 1% R0201
R497 590R 1% R0201
R491 590R 1% R0201
R493 590R 1% R0201
R485 590R 1% R0201
R489 590R 1% R0201

Q12 CJ3134KW sot-323-3 20V,0.75A
Q17 CJ3134KW sot-323-3 20V,0.75A
Q16 CJ3134KW sot-323-3 20V,0.75A
Q15 CJ3134KW sot-323-3 20V,0.75A

HDMI_TX_ON_H

Rds=1.7ohm/2.6V
Coss=7.33pf

Rds=0.45ohm/2.5V
Coss=20pf

U35
HDMI_TX2P / HDMI_TX2N / HDMI_TX1P / HDMI_TX1N
CH1 CH2 CH3 CH4 NC1 NC2 NC3 NC4 GND1 GND2
TPD4E02B04DQAR
3.6V
uson10_0d5_2d5x1x0d5mm

U32
HDMI_TX0P / HDMI_TX0N / HDMI_TX3P / HDMI_TX3N
CH1 CH2 CH3 CH4 NC1 NC2 NC3 NC4 GND1 GND2
TPD4E02B04DQAR
3.6V
uson10_0d5_2d5x1x0d5mm

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:
The controller only support AC coupled link.
In order to backward compatibility or to meet HDMI2.0 (1.4b)
DC common mode spec and Voff, need do R based level-shift.

VCC5V0_DEVICE_S0 — D50 B5819W SOD_123 40V — VCC5V_HDMI_TX
R224 DNP 0R R0402 5%

HDMI TX DDC

VCC5V0_DEVICE_S0
D45 B5819W SOD_123 40V

VCC_3V3_S0
R183 20K 1% R0201
R199 2K 1% R0201
HDMI_TX_SCL R182 100R 1% R0201 HDMI_TX_SCL_PORT
Q10 2SK3018 sot-323-3 30V,100mA

VCC_3V3_S0
R185 20K 1% R0201
R200 2K 1% R0201
HDMI_TX_SDA R184 100R 1% R0201 HDMI_TX_SDA_PORT
Q11 2SK3018 sot-323-3 30V,100mA

HDMI TX ARC

HDMI_TX_SBDP — C132 1uF 10V,X5R C0402 — HDMITX_SBDP
HDMI_TX_SBDN — C131 1uF 10V,X5R C0402 — HDMITX_HPDIN/HDMITX_SBDN

HDMI TX HPD

VCC_3V3_S0
R189 47K 5% R0201
R188 47K 5% R0201
HDMI_TX_HPDIN_M0
3.3V IO
30V,100mA sot-323-3 2SK3018 Q14
30V,100mA sot-323-3 2SK3018 Q13
2.4-5.3V
R186 1K 1% R0201 HDMITX_HPDIN/HDMITX_SBDN
R187 47K 5% R0201

HDMI TX CEC

VCC_3V3_S0 VCC5V0_DEVICE_S0
R181 27K 1% R0201
HDMI_TX_CEC_M0 R180 100R 1% R0201 HDMI_TX_CEC_PORT
Q9 2SK3018 sot-323-3 30V,100mA

HDMI Connector

Cj<=0.2pF

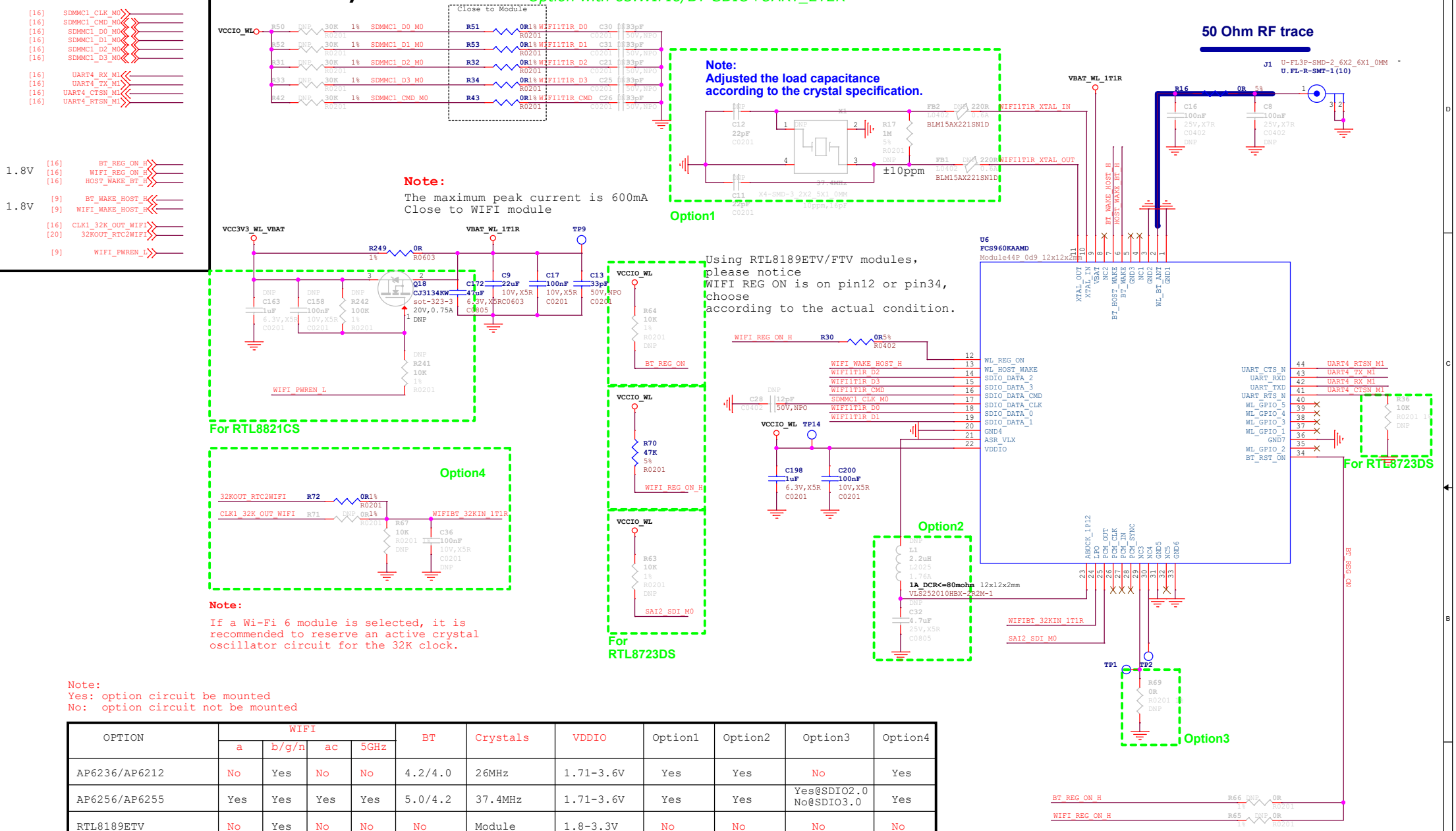
J12 TYPE A
HDMI_TX2P / HDMI_TX2N / HDMI_TX1P / HDMI_TX1N / HDMI_TX0P / HDMI_TX0N / HDMI_TX3P / HDMI_TX3N / HDMI_CEC_PORT / HDMI_TX_SCL_PORT / HDMI_TX_SDA_PORT / HDMITX_HPDIN/HDMITX_SBDN
HDMI_D2P / HDMI_D2N / HDMI_D1P / HDMI_D1N / HDMI_D0P / HDMI_D0N / HDMI_CLKP / HDMI_CLKN / HDMI_CEC / HDMI_DDC_SCL / HDMI_DDC_SDA / HDMI_5V / HPD
HDMITX_SBDP
VCC5V_HDMI_TX
TPD1E10B06DPYR D43 5.5V D0402
TPD1E10B06DPYR D39 5.5V D0402
ESD9B5.0A02V05 D42 5V D0402
ESD9B5.0A02V05 D41 5V D0402
ESD9B5.0A02V05 D44 5V D0402
TPD1E10B06DPYR D40 5.5V D0402
GND
TYPE_A
hdmi19p_1d155_23_1x7_7x16_4mm

R230 0R 5% R0805
C149 1nF 2KV,X7R C1206

seeed studio	https://www.seeedstudio.com	
	Title: RK3576_AIOT_REF_SCH	
Size: A3	Document Number: 28.VO-HDMI TX	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 28 of 38

SDIO WIFI/BT MODULE

Option with 63.WIFI6/BT-SDIO+UART_2T2R

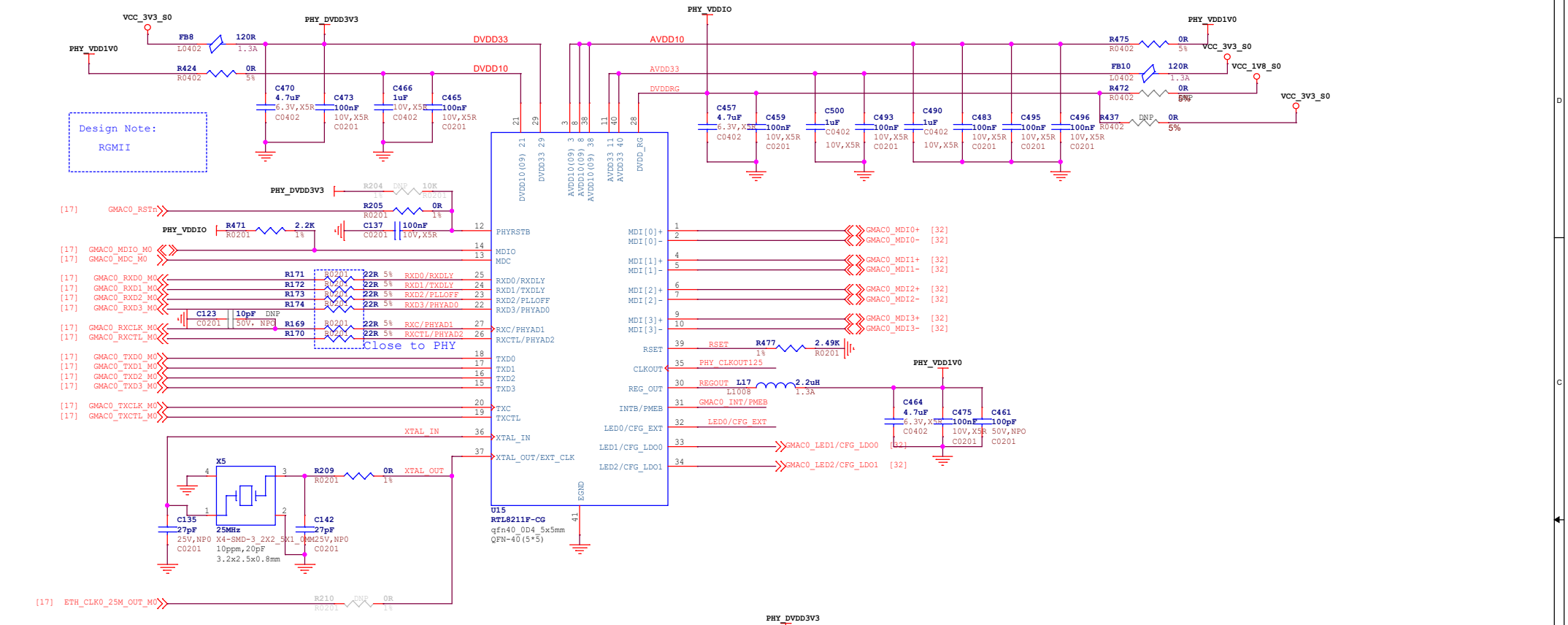


Note:
Yes: option circuit be mounted
No: option circuit not be mounted

OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

seeed studio	https://www.seeedstudio.com	
	Title: RK3576_AIOT_REF_SCH	
Size: A3	Document Number: 29.WIFI/BT-SDIO+UART_1T1R	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 29 of 38

Gigabit Ethernet



RGMII IO Voltage	CFG_EXT	CFG_LDO[1:0]
Internal 1.8V(default)	1'b0	2'b10
External 3.3V	1'b1	2'b10
External 1.8V	1'b1	2'b00

Design Note:

1. PHY_IO : 1.8V
2. PHY Addr : 001
3. Disable PLL

PHY Address	PHYAD[2:0]
1	001

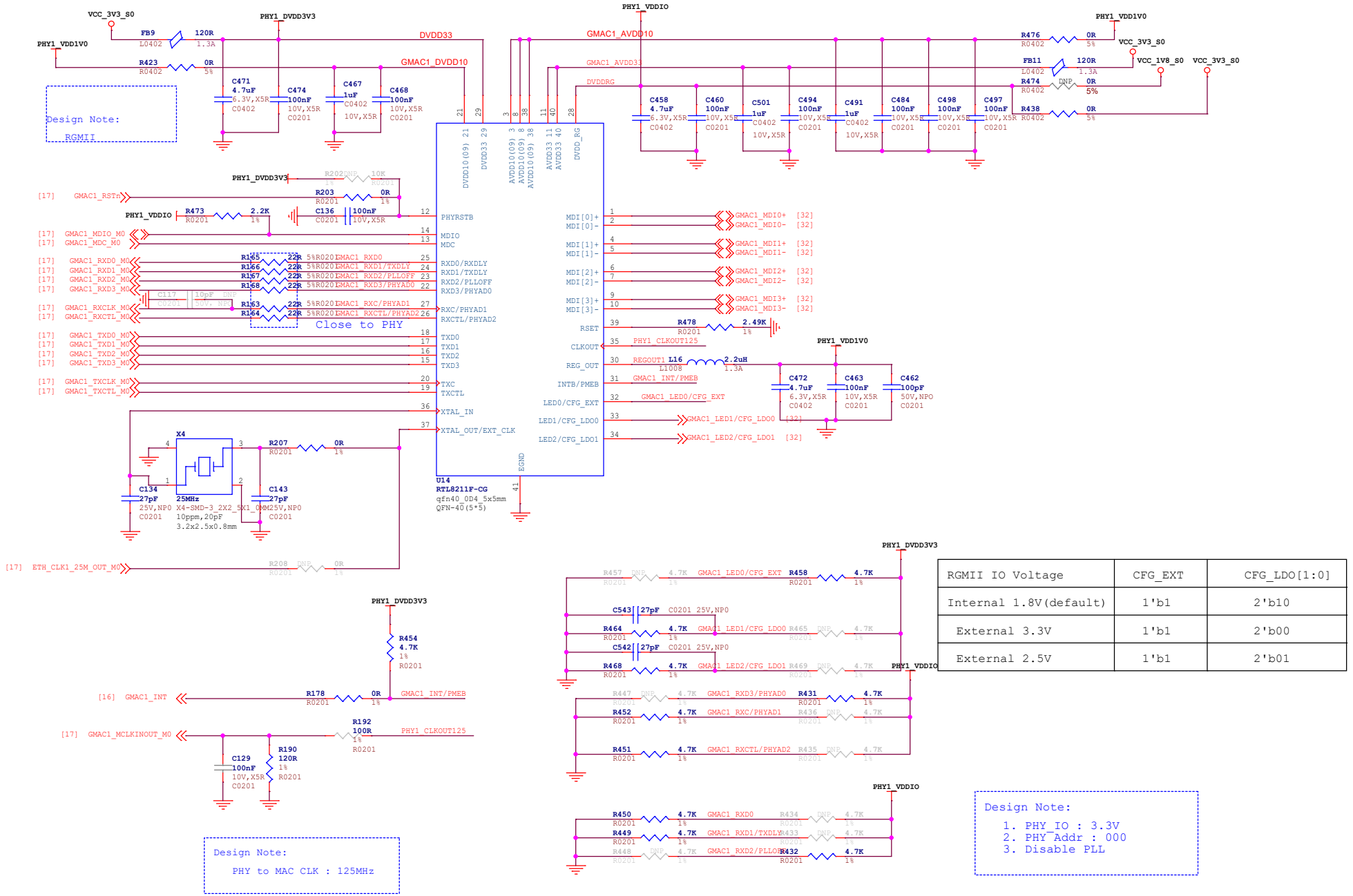
seeed studio https://www.seeedstudio.com

Title: RK3576_AIOT_REF_SCH

Size: A3 | Document Number: 30.RGMII0 Gigabit Ethernet | Rev: V1.0

Date: Thursday, March 12, 2026 | Sheet: 30 of 38

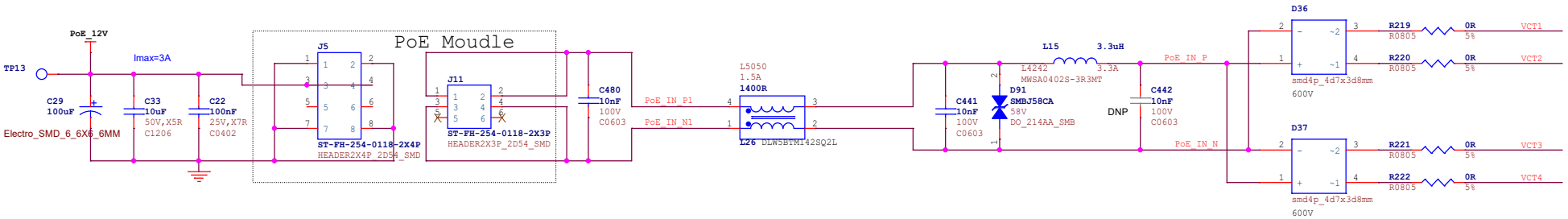
Gigabit Ethernet

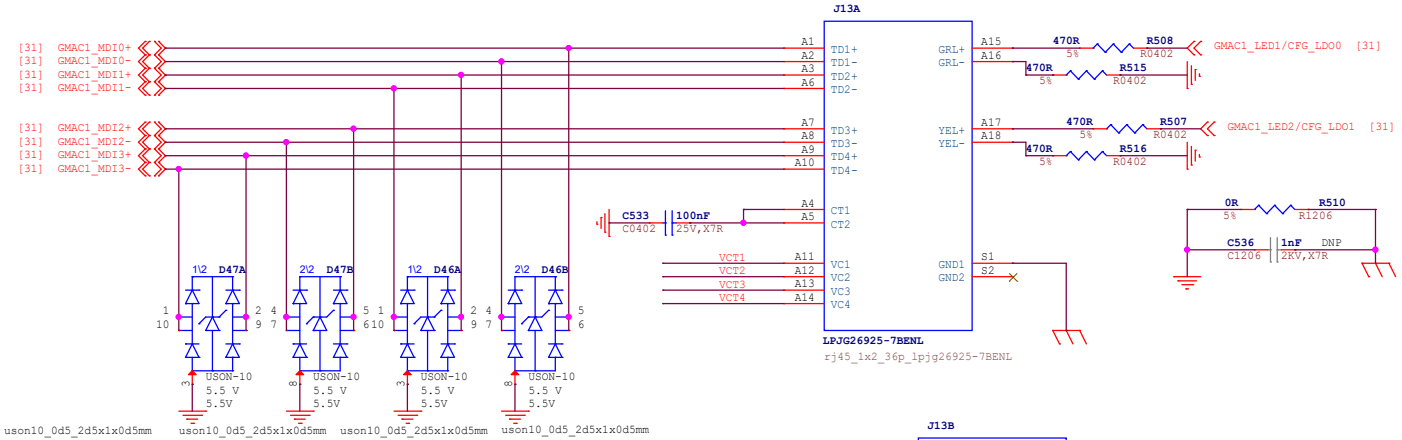


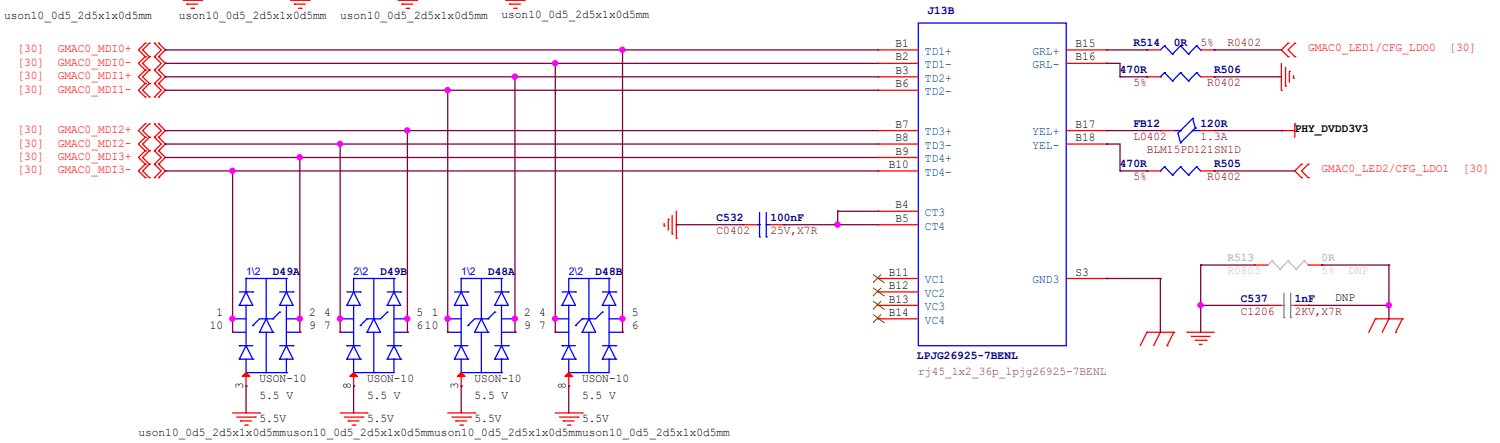
RGMII IO Voltage	CFG_EXT	CFG_LDO[1:0]
Internal 1.8V(default)	1'b1	2'b10
External 3.3V	1'b1	2'b00
External 2.5V	1'b1	2'b01

seeed studio	https://www.seeedstudio.com		
	Title: RK3576_AIOT_REF_SCH		
Size: A3	Document Number: 31.RGMII1 Gigabit Ethernet		Rev: V1.0
Date: Thursday, March 12, 2026			Sheet: 31 of 38

RJ45*2

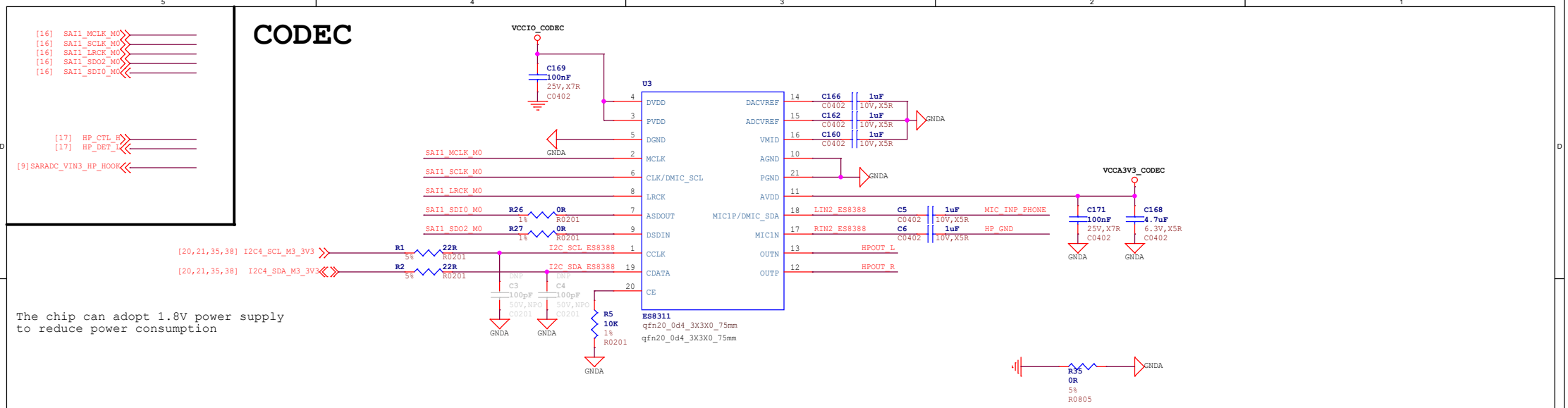






seeed studio	https://www.seeedstudio.com	
	Title: RK3576_AIOT_REF_SCH	
Size: A3	Document Number: 32.RJ45*2	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 32 of 38

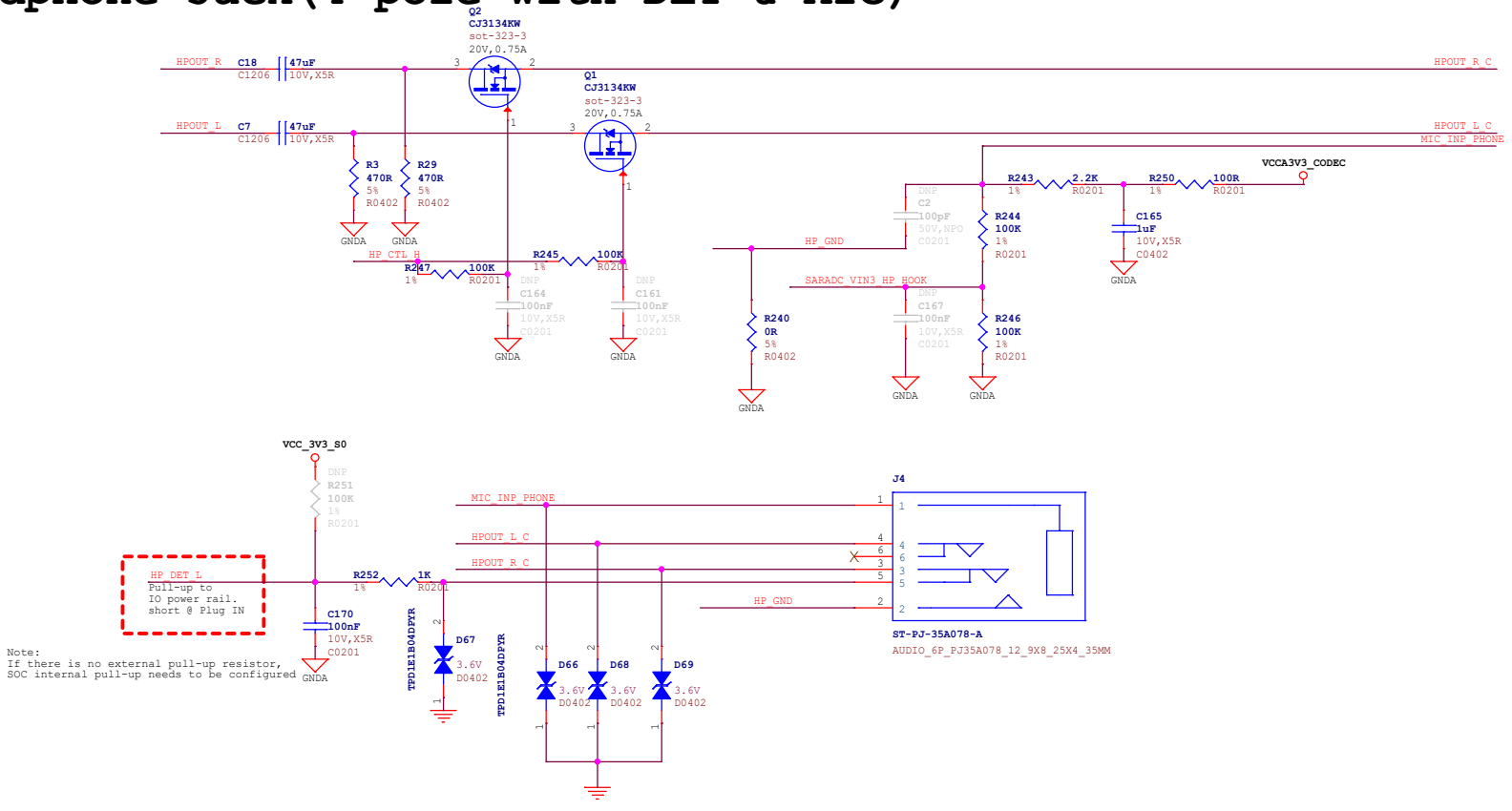
CODEC



The chip can adopt 1.8V power supply
to reduce power consumption

Headphone Jack(4-pole with DET & MIC)

CTIA(L,R,G,M)

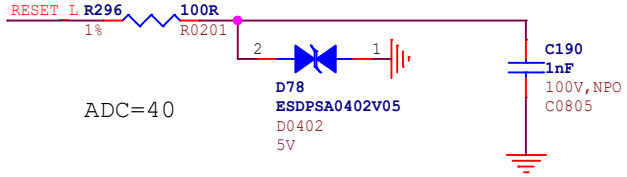


Note:
If there is no external pull-up resistor,
SOC internal pull-up needs to be configured

seeed studio	https://www.seeedstudio.com	
	Title: RK3576_AIOT_REF_SCH	
Size: A3	Document Number: 33.Audio-CODEC(ES8311)	Rev: V1.0
Date: Thursday, March 12, 2026		Sheet: 33 of 38

[9] SARADC_VIN1_KEY/RECOVERY
[9,19] RESET_L
[19] PWRON_L
[9] SARADC_VIN0_BOOT

KEY



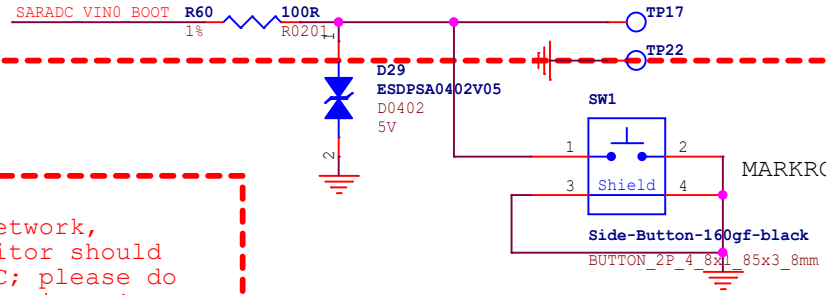
ADC=40

If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN1=0V at after power on and reset, then system will enter into loader mode.

MASKROM Key



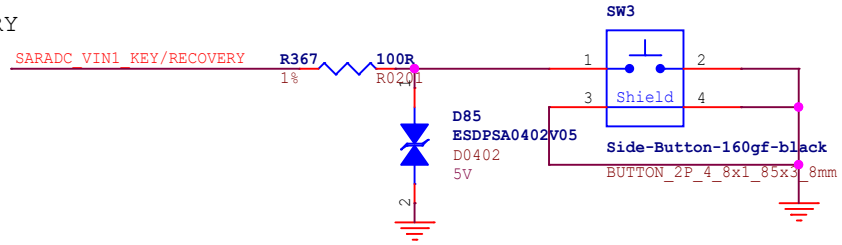
MARKROOM

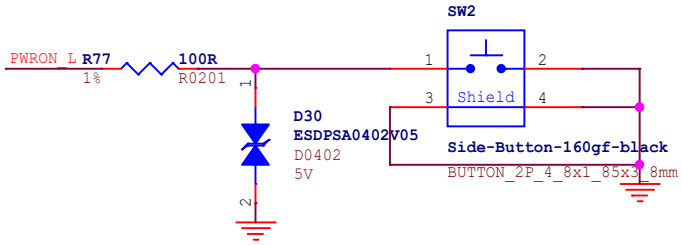
Note:
Please reserve this circuit if the MASKROM_Key is not kept

Note:
On the SARADC_VIN0_BOOT network, only one 1nF ground capacitor should be placed close to the SOC; please do not add any additional capacitors!

Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into MASKROM mode.

RECOVERY





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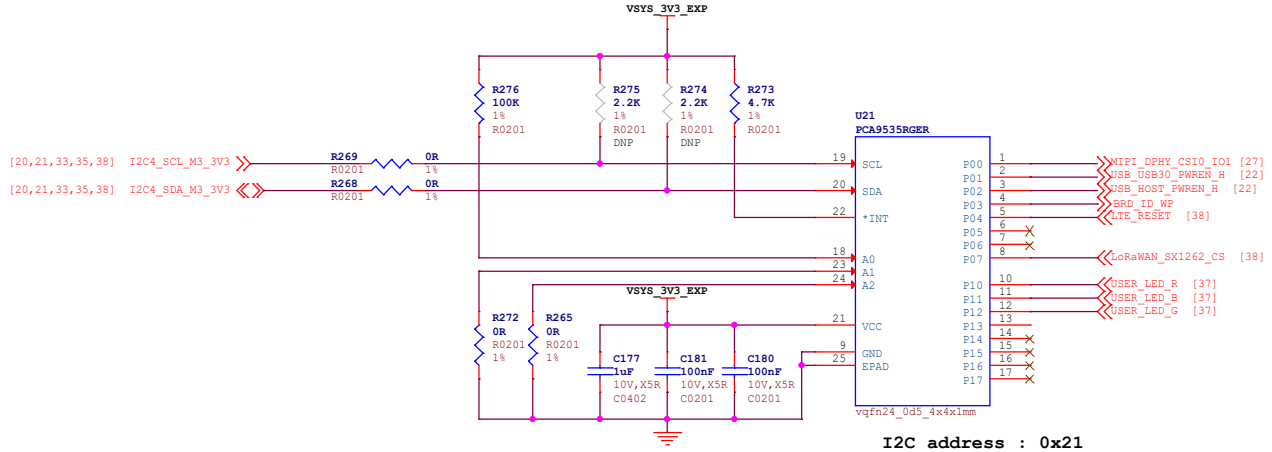
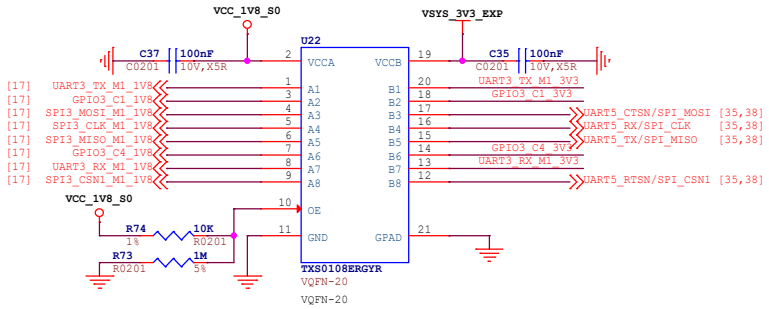
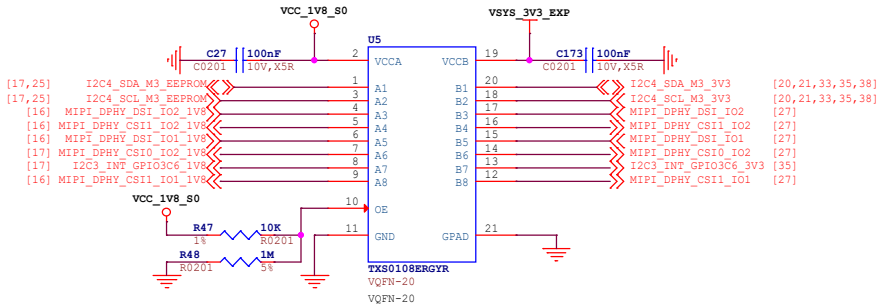
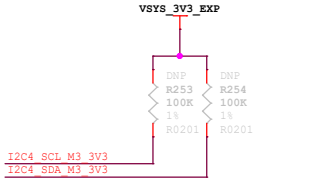
IIC TO IO/40PIN-CM5

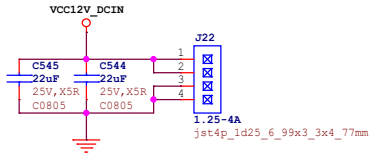


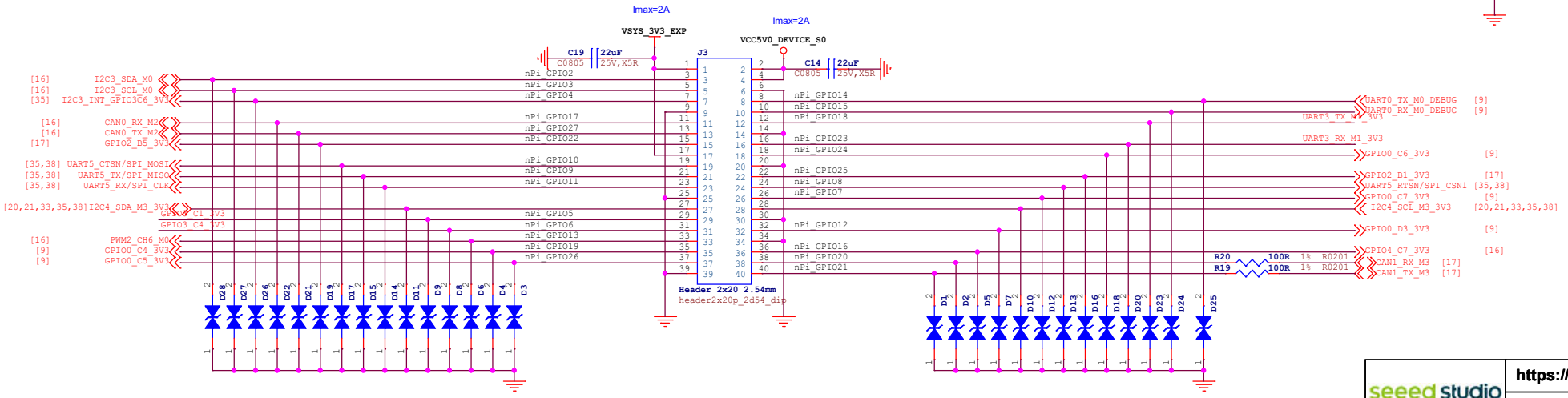
I2C address : 0x21











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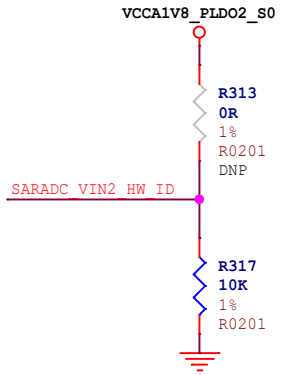
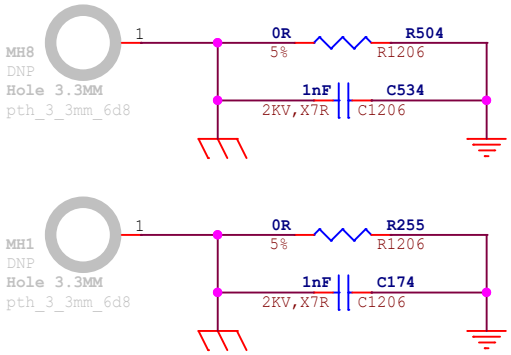
[9] SARADC_VIN2_HW_ID

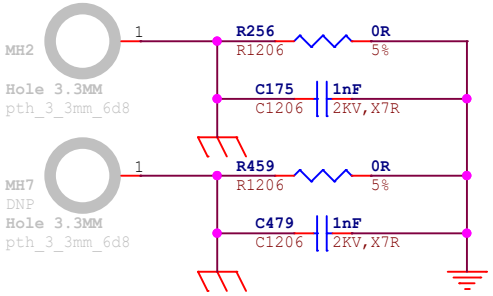
HW_ID

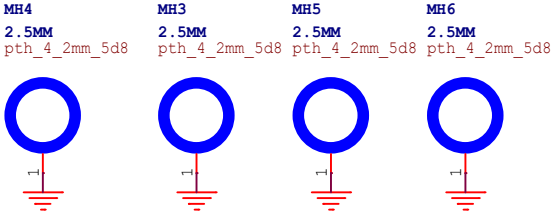


Config Table for SARADC_VIN2_HW_ID				
Item	**Rup**	**Rdown**	**ADC Value**	**VERSION**
HW_ID1	NC	10K	0	HW_ID0
HW_ID2	10K	1.13K	416	RESERVE
HW_ID3	10K	2.49K	816	RESERVE
HW_ID4	10K	4.3K	1231	RESERVE
HW_ID5	10K	6.8K	1658	RESERVE
HW_ID6	10K	10K	2048	RESERVE
HW_ID7	10K	14.7K	2437	RESERVE
HW_ID8	10K	23.2K	2862	RESERVE
HW_ID9	10K	40.2K	3279	RESERVE
HW_ID10	10K	88.7K	3680	RESERVE
HW_ID11	10K	NC	4095	RESERVE

Mount Hole







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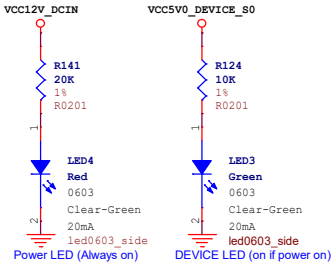
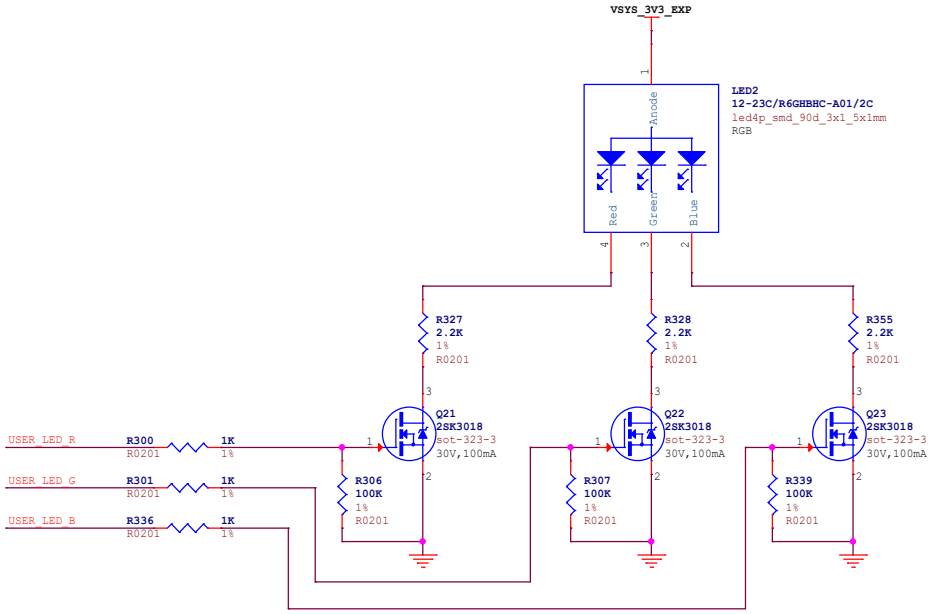
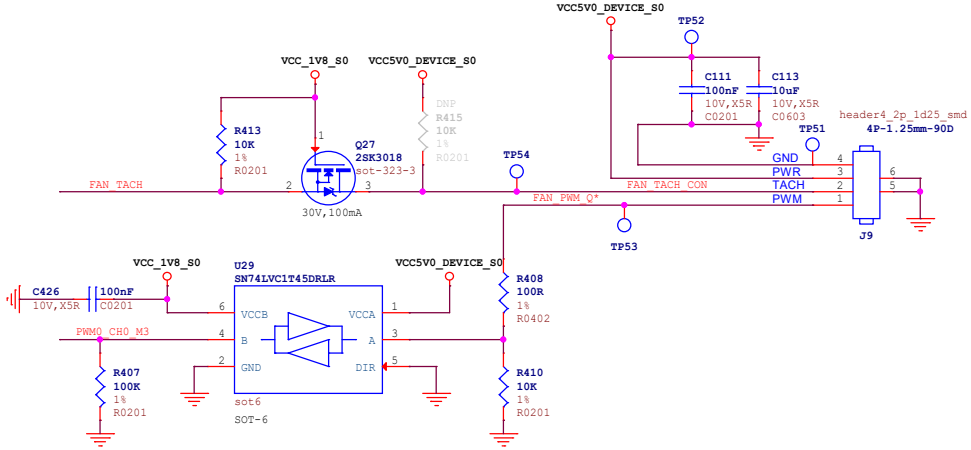
Work_LED





SoC Fan Header 4pin



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	Title: RK3576_AIOT_REF_SCH	
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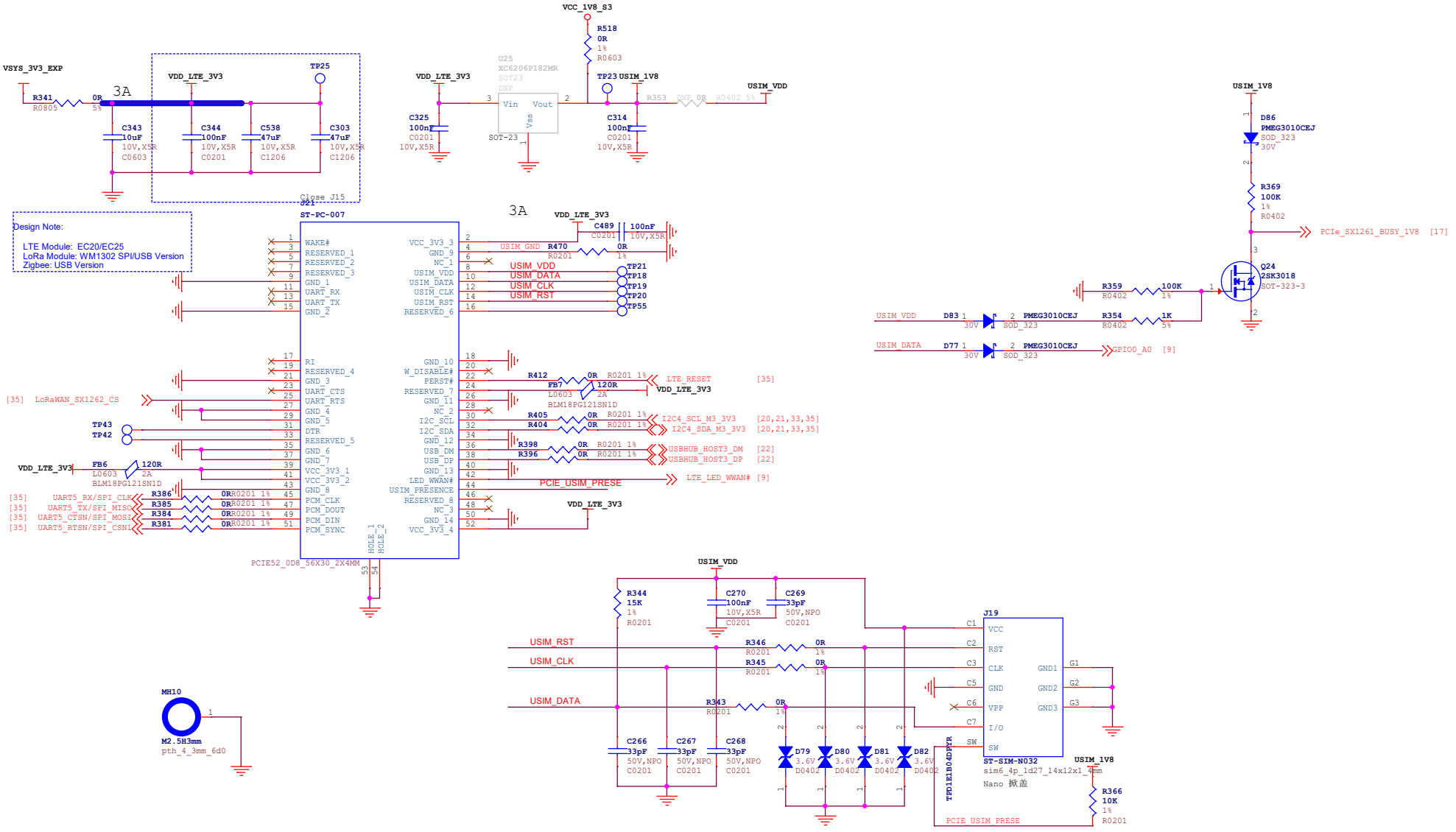

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