Table of Content

Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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	Title: RK3588_AIOT_SCH	
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Revision History

Version	Date	Change Dsecription	Approved
V1.0	2025-12-08		

seeed studio	https://www.seeedstudio.com	
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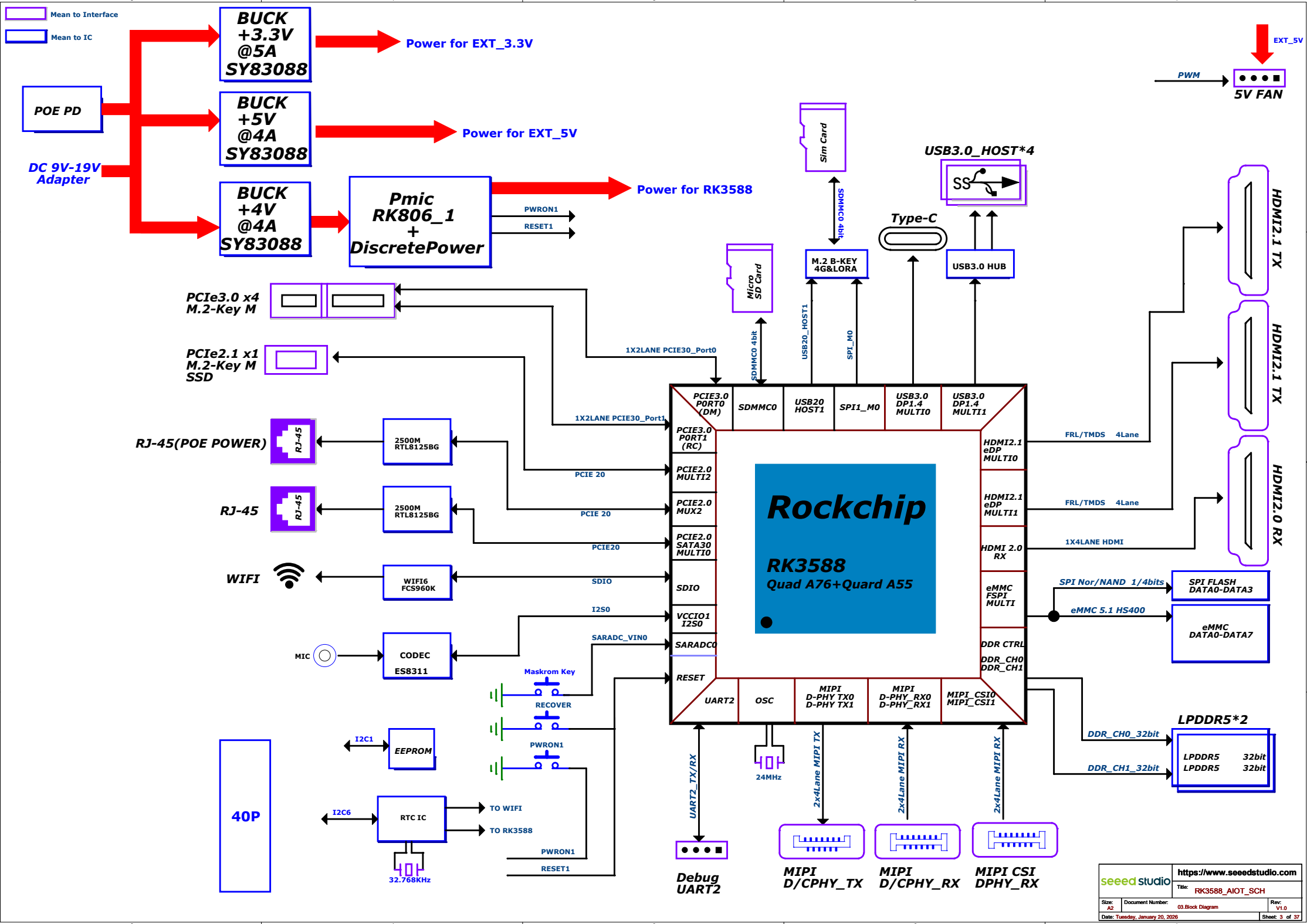
Mean to Interface
Mean to IC
POE PD
DC 9V-19V Adapter
BUCK +3.3V @5A SY83088
Power for EXT_3.3V
BUCK +5V @4A SY83088
Power for EXT_5V
BUCK +4V @4A SY83088
Pmic RK806_1 + DiscretePower
Power for RK3588
PWRON1
RESET1
EXT_5V
PWM
5V FAN
Sim Card
SDMMC0 4bit
USB3.0_HOST*4
SS
Type-C
USB3.0 HUB
M.2 B-KEY 4G&LORA
Micro SD Card
USB20_HOST1
SPI_M0
SDMMC0 4bit
PCIe3.0 x4 M.2-Key M
PCIe2.1 x1 M.2-Key M SSD
1X2LANE PCIE30_Port0
1X2LANE PCIE30_Port1
PCIE 20
PCIE 20
PCIE20
RJ-45(POE POWER)
RJ-45
2500M RTL8125BG
2500M RTL8125BG
WIFI
WIFI6 FCS960K
SDIO
MIC
CODEC ES8311
I2S0
SARADC_VIN0
Maskrom Key
RECOVER
PWRON1
I2C1
EEPROM
I2C6
RTC IC
TO WIFI
TO RK3588
PWRON1
RESET1
32.768KHz
40P
PCIE3.0 P0RT0 (DM)
SDMMC0
USB20 HOST1
SPI1_M0
USB3.0 DP1.4 MULTI0
USB3.0 DP1.4 MULTI1
PCIE3.0 P0RT1 (RC)
PCIE2.0 MULTI2
PCIE2.0 MUX2
PCIE2.0 SATA30 MULTI0
SDIO
VCCIO1 I2S0
SARADC0
RESET
HDMI2.1 eDP MULTI0
HDMI2.1 eDP MULTI1
HDMI 2.0 RX
eMMC FSPI MULTI
DDR CTRL
DDR_CH0 DDR_CH1
UART2
OSC
MIPI D-PHY TX0 D-PHY TX1
MIPI D-PHY_RX0 D-PHY_RX1
MIPI_CSI0 MIPI_CSI1
Rockchip
RK3588
Quad A76+Quard A55
FRL/TMDS 4Lane
FRL/TMDS 4Lane
1X4LANE HDMI
HDMI2.1 TX
HDMI2.1 TX
HDMI2.0 RX
SPI Nor/NAND 1/4bits
SPI FLASH DATA0-DATA3
eMMC 5.1 HS400
eMMC DATA0-DATA7
LPDDR5*2
DDR_CH0_32bit
DDR_CH1_32bit
LPDDR5 32bit
LPDDR5 32bit
UART2_TX/RX
24MHz
2x4Lane MIPI TX
2x4Lane MIPI RX
2x4Lane MIPI RX
Debug UART2
MIPI D/CPHY_TX
MIPI D/CPHY_RX
MIPI CSI DPHY_RX
seeed studio
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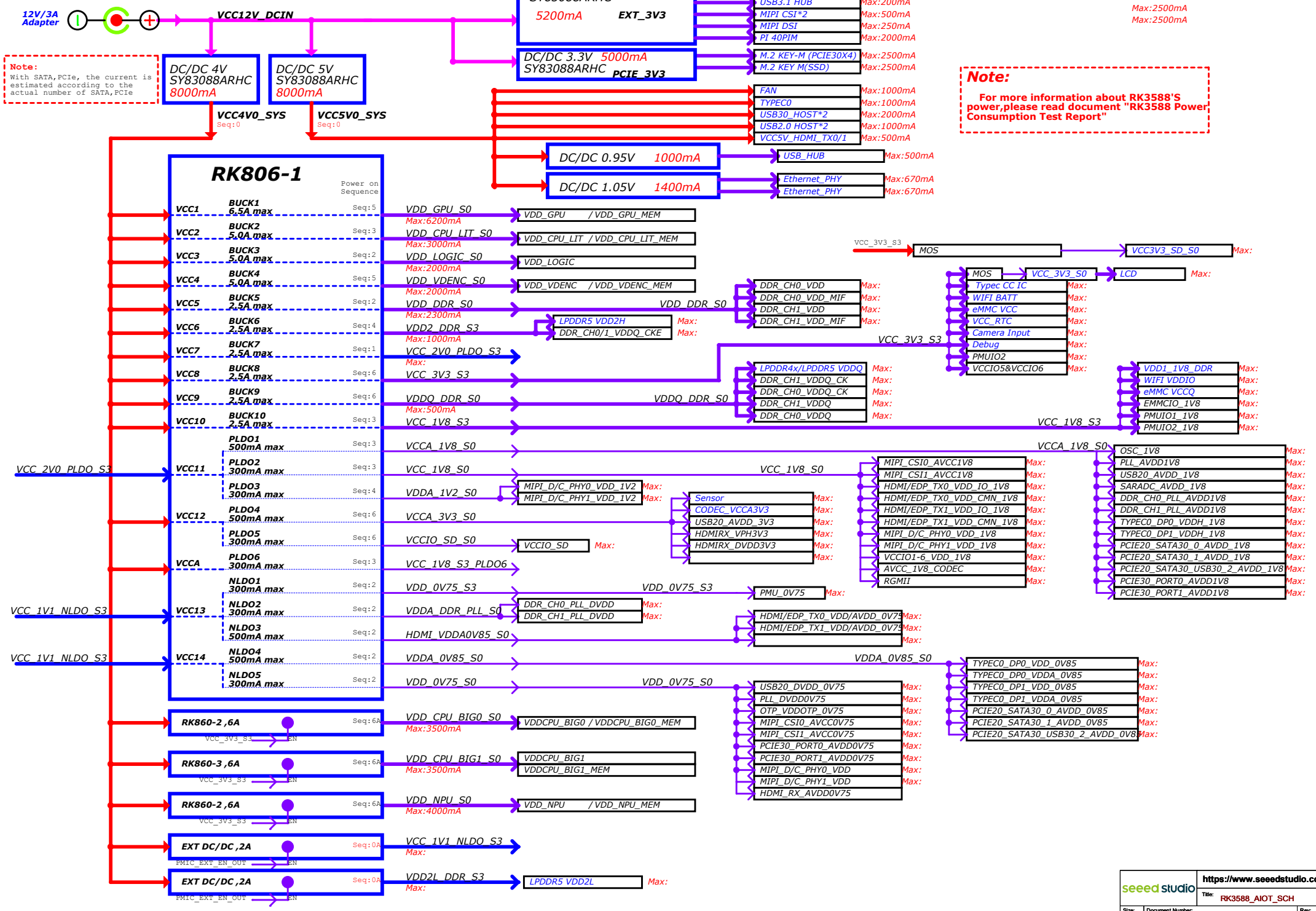
Power Tree


12V/3A Adapter
VCC12V_DCIN
Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe
DC/DC 4V SY83088ARHC 8000mA
DC/DC 5V SY83088ARHC 8000mA
VCC4V0_SYS Seq:0
VCC5V0_SYS Seq:0
DC/DC 3.3V SY83088ARHC 5200mA EXT_3V3
M.2 KEY-B (4G) Max:2000mA
Ethernet_PHY*2 Max:220mA
USB3.1 HUB Max:200mA
MIPI CSI*2 Max:500mA
MIPI DSI Max:250mA
PI 40PIM Max:2000mA
DC/DC 3.3V 5000mA SY83088ARHC PCIE_3V3
M.2 KEY-M (PCIE30X4) Max:2500mA
M.2 KEY M(SSD) Max:2500mA
Max:2500mA
Max:2500mA
Note:
For more information about RK3588'S power,please read document "RK3588 Power Consumption Test Report"
FAN Max:1000mA
TYPEC0 Max:1000mA
USB30_HOST*2 Max:2000mA
USB2.0 HOST*2 Max:1000mA
VCC5V_HDMI_TX0/1 Max:500mA
DC/DC 0.95V 1000mA
USB_HUB Max:500mA
DC/DC 1.05V 1400mA
Ethernet_PHY Max:670mA
Ethernet_PHY Max:670mA
RK806-1
Power on Sequence
VCC1 BUCK1 6.5A max Seq:5 VDD_GPU_S0 Max:6200mA
VCC2 BUCK2 5.0A max Seq:3 VDD_CPU_LIT_S0 Max:3000mA
VCC3 BUCK3 5.0A max Seq:2 VDD_LOGIC_S0 Max:2000mA
VCC4 BUCK4 5.0A max Seq:5 VDD_VDENC_S0 Max:2000mA
VCC5 BUCK5 2.5A max Seq:2 VDD_DDR_S0 Max:2300mA
VCC6 BUCK6 2.5A max Seq:4 VDD2_DDR_S3 Max:1000mA
VCC7 BUCK7 2.5A max Seq:1 VCC_2V0_PLDO_S3 Max:
VCC8 BUCK8 2.5A max Seq:6 VCC_3V3_S3
VCC9 BUCK9 2.5A max Seq:6 VDDQ_DDR_S0 Max:500mA
VCC10 BUCK10 2.5A max Seq:3 VCC_1V8_S3
VCC11 PLDO1 500mA max Seq:3 VCCA_1V8_S0
PLDO2 300mA max Seq:3 VCC_1V8_S0
PLDO3 300mA max Seq:4 VDDA_1V2_S0
VCC12 PLDO4 500mA max Seq:6 VCCA_3V3_S0
PLDO5 300mA max Seq:6 VCCIO_SD_S0
VCCA PLDO6 300mA max Seq:3 VCC_1V8_S3_PLDO6
NLDO1 300mA max Seq:2 VDD_0V75_S3
VCC13 NLDO2 300mA max Seq:2 VDDA_DDR_PLL_S0
NLDO3 500mA max Seq:2 HDMI_VDDA0V85_S0
VCC14 NLDO4 500mA max Seq:2 VDDA_0V85_S0
NLDO5 300mA max Seq:2 VDD_0V75_S0
VCC_2V0_PLDO_S3
VCC_1V1_NLDO_S3
VCC_1V1_NLDO_S3
RK860-2 ,6A Seq:6A VDD_CPU_BIG0_S0 Max:3500mA
VCC_3V3_S3 EN
RK860-3 ,6A Seq:6A VDD_CPU_BIG1_S0 Max:3500mA
RK860-2 ,6A Seq:6A VDD_NPU_S0 Max:4000mA
EXT DC/DC ,2A Seq:0A VCC_1V1_NLDO_S3 Max:
PMIC_EXT_EN_OUT EN
EXT DC/DC ,2A Seq:0A VDD2L_DDR_S3 Max:
VDD_GPU / VDD_GPU_MEM
VDD_CPU_LIT / VDD_CPU_LIT_MEM
VDD_LOGIC
VDD_VDENC / VDD_VDENC_MEM
VDD_DDR_S0
LPDDR5 VDD2H Max:
DDR_CH0/1_VDDQ_CKE Max:
DDR_CH0_VDD Max:
DDR_CH0_VDD_MIF Max:
DDR_CH1_VDD Max:
DDR_CH1_VDD_MIF Max:
VCC_3V3_S3
MOS
VCC3V3_SD_S0 Max:
MOS
VCC_3V3_S0
LCD Max:
Typec CC IC Max:
WIFI BATT Max:
eMMC VCC Max:
VCC_RTC Max:
Camera Input Max:
Debug Max:
PMUIO2 Max:
VCCIO5&VCCIO6 Max:
VDDQ_DDR_S0
LPDDR4x/LPDDR5 VDDQ Max:
DDR_CH1_VDDQ_CK Max:
DDR_CH0_VDDQ_CK Max:
DDR_CH1_VDDQ Max:
DDR_CH0_VDDQ Max:
VDD1_1V8_DDR Max:
WIFI VDDIO Max:
eMMC VCCQ Max:
EMMCIO_1V8 Max:
PMUIO1_1V8 Max:
PMUIO2_1V8 Max:
VCC_1V8_S3
VCCA_1V8_S0
OSC_1V8 Max:
PLL_AVDD1V8 Max:
USB20_AVDD_1V8 Max:
SARADC_AVDD_1V8 Max:
DDR_CH0_PLL_AVDD1V8 Max:
DDR_CH1_PLL_AVDD1V8 Max:
TYPEC0_DP0_VDDH_1V8 Max:
TYPEC0_DP1_VDDH_1V8 Max:
PCIE20_SATA30_0_AVDD_1V8 Max:
PCIE20_SATA30_1_AVDD_1V8 Max:
PCIE20_SATA30_USB30_2_AVDD_1V8 Max:
PCIE30_PORT0_AVDD1V8 Max:
PCIE30_PORT1_AVDD1V8 Max:
VCC_1V8_S0
MIPI_D/C_PHY0_VDD_1V2 Max:
MIPI_D/C_PHY1_VDD_1V2 Max:
Sensor Max:
CODEC_VCCA3V3 Max:
USB20_AVDD_3V3 Max:
HDMIRX_VPH3V3 Max:
HDMIRX_DVDD3V3 Max:
MIPI_CSI0_AVCC1V8 Max:
MIPI_CSI1_AVCC1V8 Max:
HDMI/EDP_TX0_VDD_IO_1V8 Max:
HDMI/EDP_TX0_VDD_CMN_1V8 Max:
HDMI/EDP_TX1_VDD_IO_1V8 Max:
HDMI/EDP_TX1_VDD_CMN_1V8 Max:
MIPI_D/C_PHY0_VDD_1V8 Max:
MIPI_D/C_PHY1_VDD_1V8 Max:
VCCIO1-6_VDD_1V8 Max:
AVCC_1V8_CODEC Max:
RGMII Max:
VCCIO_SD Max:
VDD_0V75_S3
PMU_0V75 Max:
DDR_CH0_PLL_DVDD Max:
DDR_CH1_PLL_DVDD Max:
HDMI/EDP_TX0_VDD/AVDD_0V75 Max:
HDMI/EDP_TX1_VDD/AVDD_0V75 Max:
VDD_0V75_S0
USB20_DVDD_0V75 Max:
PLL_DVDD0V75 Max:
OTP_VDDOTP_0V75 Max:
MIPI_CSI0_AVCC0V75 Max:
MIPI_CSI1_AVCC0V75 Max:
PCIE30_PORT0_AVDD0V75 Max:
PCIE30_PORT1_AVDD0V75 Max:
MIPI_D/C_PHY0_VDD Max:
MIPI_D/C_PHY1_VDD Max:
HDMI_RX_AVDD0V75
VDDA_0V85_S0
TYPEC0_DP0_VDD_0V85 Max:
TYPEC0_DP0_VDDA_0V85 Max:
TYPEC0_DP1_VDD_0V85 Max:
TYPEC0_DP1_VDDA_0V85 Max:
PCIE20_SATA30_0_AVDD_0V85 Max:
PCIE20_SATA30_1_AVDD_0V85 Max:
PCIE20_SATA30_USB30_2_AVDD_0V85 Max:
VDDCPU_BIG0 / VDDCPU_BIG0_MEM
VDDCPU_BIG1
VDDCPU_BIG1_MEM
VDD_NPU / VDD_NPU_MEM
LPDDR5 VDD2L Max:
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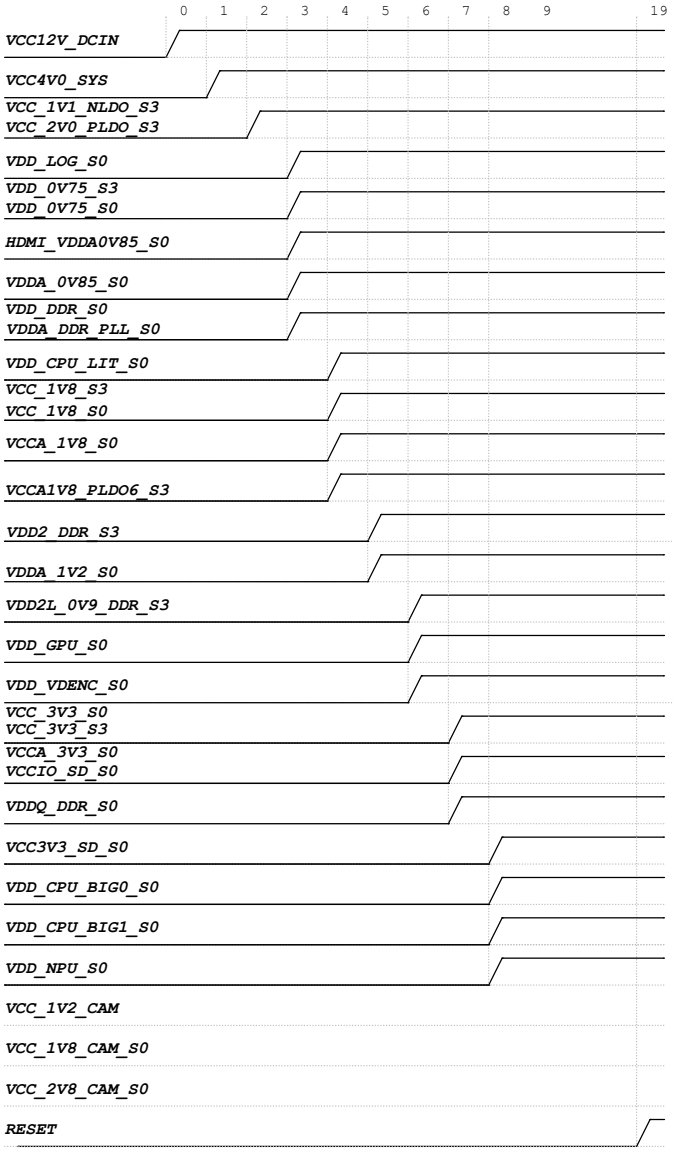
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	HDMI_VDDA0V85_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

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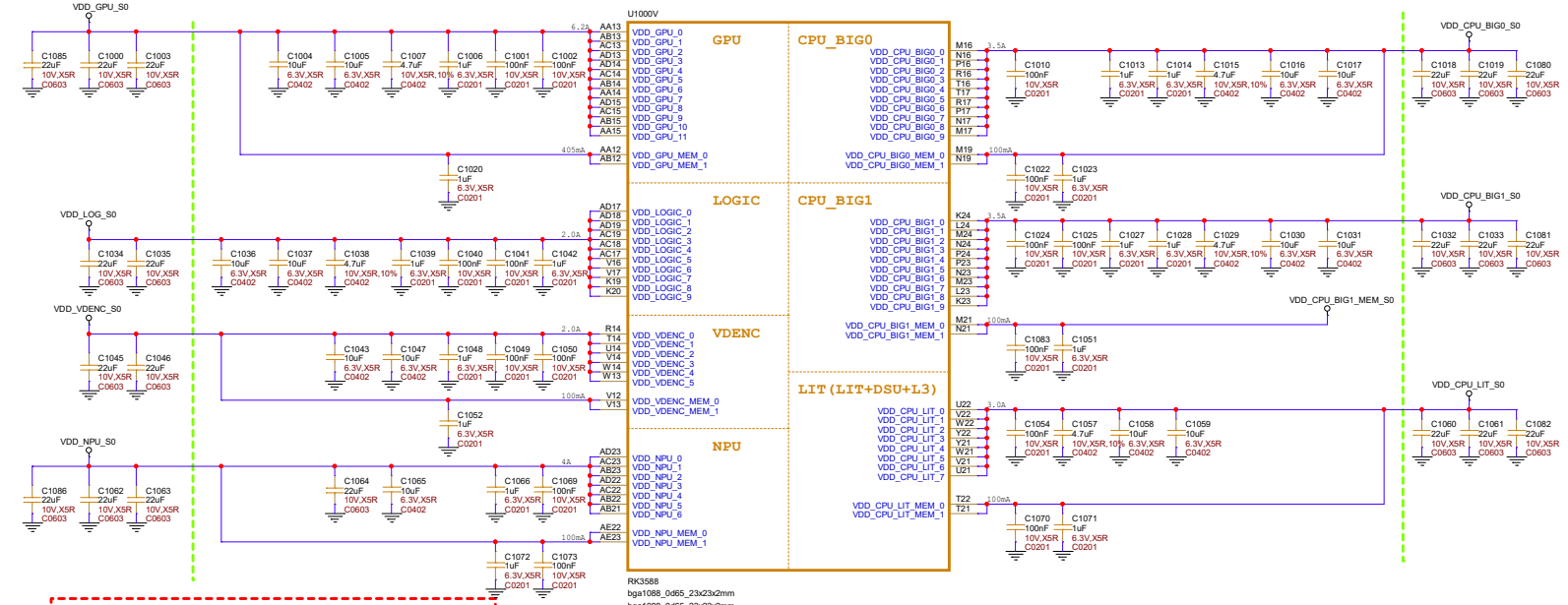
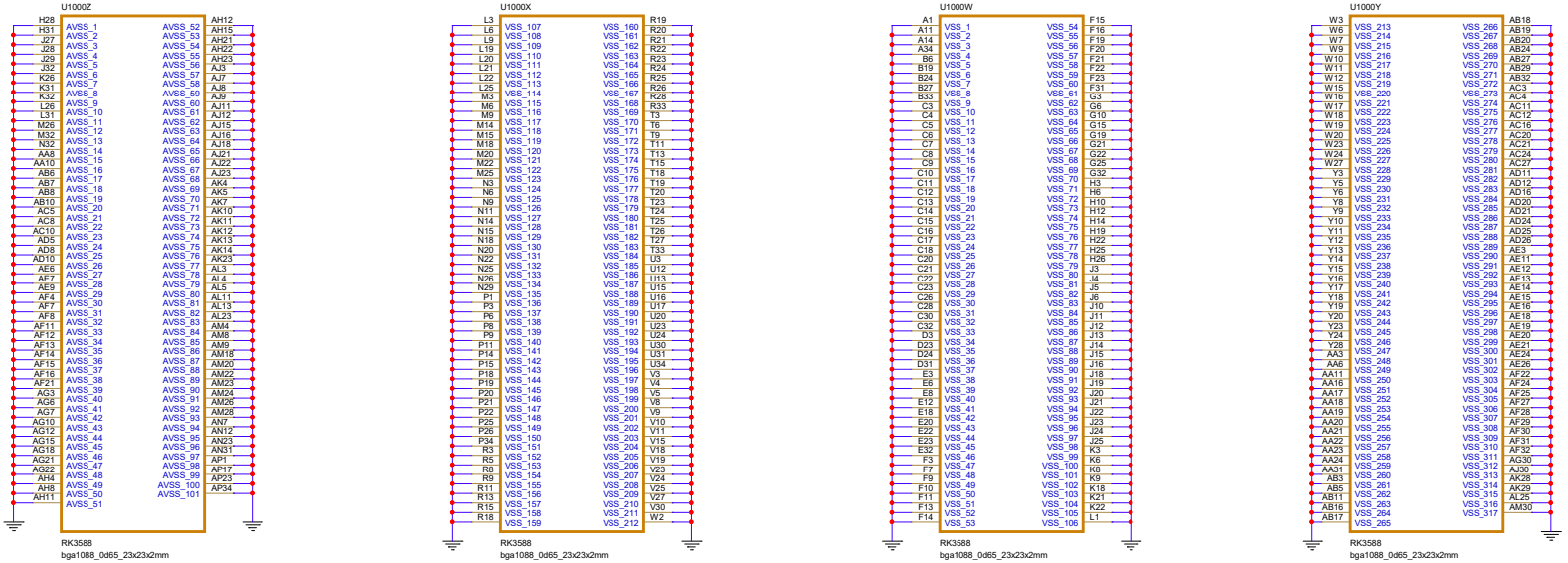
RK3588_V(POWER)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



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	Title: RK3588_AIOT_SCH		
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RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

U1000E

OSC
XOUT_24M
XIN_24M

R1100 22R 5% R0201
Y1 24MHz x4_smd_2_0x1_6mm 10ppm,9pF
C1101 9pF 50V,NPO C0402
R1101 510K 1% R0402
C1102 9pF 50V,NPO C0402
XOUT24M T34
XIN24M R34

PLL
PLL_DVDD0V75
PLL_AVDD1V8
PLL_AVSS
OSC_1V8

VCCA_1V8_S0 N27
C1103 1uF C0201 6.3V,X5R
C1104 100nF C0201 10V,X5R
VDD_0V75_S0 V20
C1105 1uF C0201 6.3V,X5R
C1106 100nF C0201 10V,X5R
VCCA_1V8_S0 U18
C1109 100nF C0201 10V,X5R
U19

Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

PMUIO1 Domain
Operating Voltage=1.8V Only

NPOR_u M31 RESET_L
TVSS M29
C1100 100nF C0201 10V,X5R
R467 0R 1% R0201 TSADC_SHUT_H
RESET_L [19,28]

REFCLK_OUT / GPIO0_A0_d P33
TSADC_SHUT_ORG / TSADC_SHUT / GPIO0_A1_z P32 TSADC_SHUT_H
PMIC_SLEEP1 / GPIO0_A2_d R32
PMIC_SLEEP2 / GPIO0_A3_d R31
SDMMC_DET / GPIO0_A4_u P31
PMU_DEBUG / SDMMC_PWREN / SPI2_CLK_M2 / GPIO0_A5_d N31 SPI2_CLK_M2
I2C0_SDA_M0 / SPI2_MOSI_M2 / GPIO0_A6_z N30
PMIC_INT_L / GPIO0_A7_u M30
R1137 0R 1% R0201 BT_WAKE_HOST_H [24]
R1104 22R 5% R0201
R1107 22R 5% R0201
PMIC_PWR_CTRL1 [19]
CPU_BIG0_VSEL [20]
SDMMC_DET_L [27]
PMIC_SPI_CLK [19]
PMIC_SPI_MOSI [19]
PMIC_INT_L [19]

UART0_RX_M1 / I2C1_SCL_M1 / SPI2_CS1_M2 / GPIO0_B0_z L30
PWM5_M0 / UART0_TX_M1 / I2C1_SDA_M1 / SPI2_CS0_M2 / GPIO0_B1_z K30
CLK32K_OUT0 / CLK32K_IN / GPIO0_B2_u K29
I2C0_SCL_M0 / SPI2_MISO_M2 / GPIO0_B3_z L29
RTC_INT_L [21]
PMIC_SPI_CS [19]
WIFI_WAKE_HOST_H [24]

PMUIO1_1V8 N28
C1107 100nF C0201 10V,X5R
VCC_1V8_S3

PMUIO1/2 Domain Logic Power
Operating Voltage=0.75V

PMU_0V75 P27
C1110 100nF C0201 10V,X5R
C1111 1uF C0201 6.3V,X5R
VDD_0V75_S3

Note:
If the soc is interconnected with other chips,In the scenario where the soc is not power on,isolation needs to be considered seriously to prevent the leakage to the soc through GPIO or power,which causes soc power-on sequence abnormality.

若SOC和其它芯片存在互联，在SOC未加电的情况下，需要仔细考虑隔离措施，以防止通过GPIO或电源路径向SOC漏电，这可能会导致SOC的上电时序出现异常。

RK3588_F(PMUIO2)

U1000F

PMUIO2 Domain
Operating Voltage=1.8V/3.3V

/ UART2_TX_M0 / / I2S1_MCLK_M1 / PCIE30X1_1_CLKREQN_M0 / / I2C1_SCL_M0 / JTAG_TCK_M2 / GPIO0_B5_d P29 UART2_TX_DEBUG_PORT [28]
/ UART2_RX_M0 / / I2S1_SCLK_M1 / PCIE30X1_1_WAKEN_M0 / / I2C1_SDA_M0 / JTAG_TMS_M2 / GPIO0_B6_d R29 UART2_RX_DEBUG_PORT [28]
/ / CAN0_TX_M0 / I2S1_LRCK_M1 / PCIE30X1_1_PERSTN_M0 / SPI0_CS1_M0 / I2C2_SCL_M0 / PWM0_M0 / GPIO0_B7_d T28 GPIO0_B7 [29]
/ / CAN0_RX_M0 / PDM0_CLK0_M1 / / PCIE30X1_0_CLKREQN_M0 / SPI0_MOSI_M0/ I2C2_SDA_M0 / PWM1_M0 / GPIO0_C0_d T31 GPIO0_C0 [28]
/ / / / / PMIC_SLEEP3 / GPIO0_C1_d U32 NPU_VSEL [20]
/ / / / / PMIC_SLEEP4 / GPIO0_C2_d T32 GPU R183 DNP 100K 1% R0201 PMIC_PWR_CTRL3 [19]
/ / / / / PMIC_SLEEP5 / GPIO0_C3_d T30 DDR R429 1% 100K R0201 PMIC_PWR_CTRL2 [19]
/ UART0_RX_M0 / DP0_HPDIN_M1 / PDM0_CLK1_M1 / / PCIE30X1_0_WAKEN_M0 / / I2C4_SDA_M2 / PWM2_M0 / GPIO0_C4_d R30 GPIO0_C4 [28]
PWM4_M0 / UART0_TX_M0 / DP1_HPDIN_M1 / / I2S1_SDI0_M1 / PCIE30X1_0_PERSTN_M0 / / I2C4_SCL_M2 / GPU_AVS / GPIO0_C5_u P30 GPIO0_C5_u [28]
PWM5_M1 / UART0_RTSN / SATA_CP_POD / / I2S1_SDI1_M1 / PCIE30X4_CLKREQN_M0 / SPI0_CLK_M0 / / NPU_AVS / GPIO0_C6_u T29 GPIO0_C6_u [28]
/ UART1_RTSN_M2 / / PDM0_SDI0_M1 / I2S1_SDI2_M1 / PCIE30X4_WAKEN_M0 / SPI0_MISO_M0/ I2C6_SDA_M0 / PWM6_M0 / GPIO0_C7_d V31 I2C6_SDA_3V3 [18,21,28,29,33]
/ UART1_CTSN_M2 / / PDM0_SDI1_M1 / I2S1_SDI3_M1 / PCIE30X4_PERSTN_M0 / SPI3_MOSI_M0/ I2C6_SCL_M0 / PWM7_IR_M0 / GPIO0_D0_d W31 I2C6_SCL_3V3 [18,21,28,29,33]
HDMI_TX0_CEC_M1 / UART1_TX_M2 / UART0_CTSN / HDMI_RX_SDA_M0/ I2S1_SDO0_M1 / PCIE30X2_CLKREQN_M0 / SPI3_CS0_M0 / I2C0_SCL_M2 / CPU_BIG0_AVS / GPIO0_D1_u W30 I2C0_SCL_M2 [20]
HDMI_TX1_CEC_M1 / UART1_RX_M2 / / HDMI_RX_SCL_M0/ I2S1_SDO1_M1 / PCIE30X2_WAKEN_M0 / SPI3_MOSI_M2/ I2C0_SDA_M2 / / GPIO0_D2_u W29 I2C0_SDA_M2 [20]
/ / / / / SPI3_CLK_M2 / LITCPU_AVS / GPIO0_D3_u U33 CC_INT_L [7,18]
HDMI_TX0_SDA_M1 / SATA_CPDET / CAN2_RX_M1 / PDM0_SDI2_M1 / I2S1_SDO2_M1 / PCIE30X2_PERSTN_M0 / SPI3_CS0_M2 / I2C1_SCL_M2 / PWM3_IR_M0 / GPIO0_D4_u V29 I2C1_SCL_M2 [20]
HDMI_TX0_SCL_M1 / SATA_MP_SWITCH/ CAN2_TX_M1 / / I2S1_SDO3_M1 / / SPI3_CS1_M2 / I2C1_SDA_M2 / CPU_BIG1_AVS / GPIO0_D5_u V28 I2C1_SDA_M2 [20]
/ PDM0_SDI3_M1 / / / / / PMIC_SLEEP6 / GPIO0_D6_d W28 CPU_BIG1_VSEL [20]

PMUIO2_1V8 R27 C1112 100nF C0201 10V,X5R VCC_1V8_S3
PMUIO2 P28 R200 DNP 0R 5% R0402 VCC_1V8_S3
R199 5% 0R R0402 VCC_3V3_S3
C1113 100nF C0201 10V,X5R

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

Pay attention to whether the voltage is matches.

R430 120K 1% R0402
R431 DNP 120K 1% R0402

VCC_3V3_S3
R1139 2.2K R0201 1%
R1140 2.2K R0201 1%
I2C0_SCL_M2 TP90
I2C0_SDA_M2 TP91

VCC_3V3_S3
R481 10K R0201 1%
R5067 2.2K R0201 1%
R5068 2.2K R0201 1%
I2C6_SDA_3V3 TP86
I2C6_SCL_3V3 TP87
CC_INT_L [7,18]

VCC_3V3_S3
R1113 2.2K R0201 1%
R1114 2.2K R0201 1%
I2C1_SCL_M2 TP88
I2C1_SDA_M2 TP89

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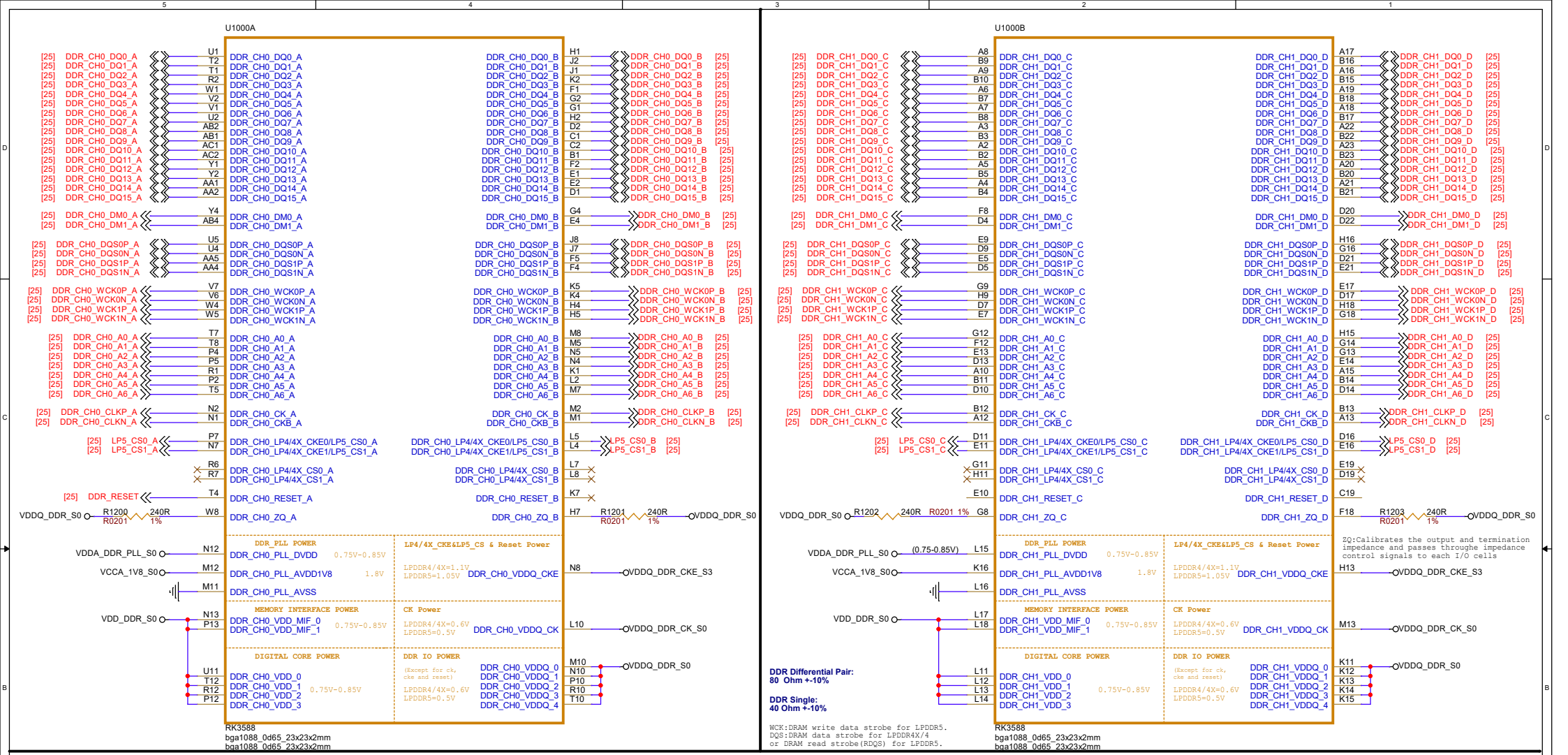
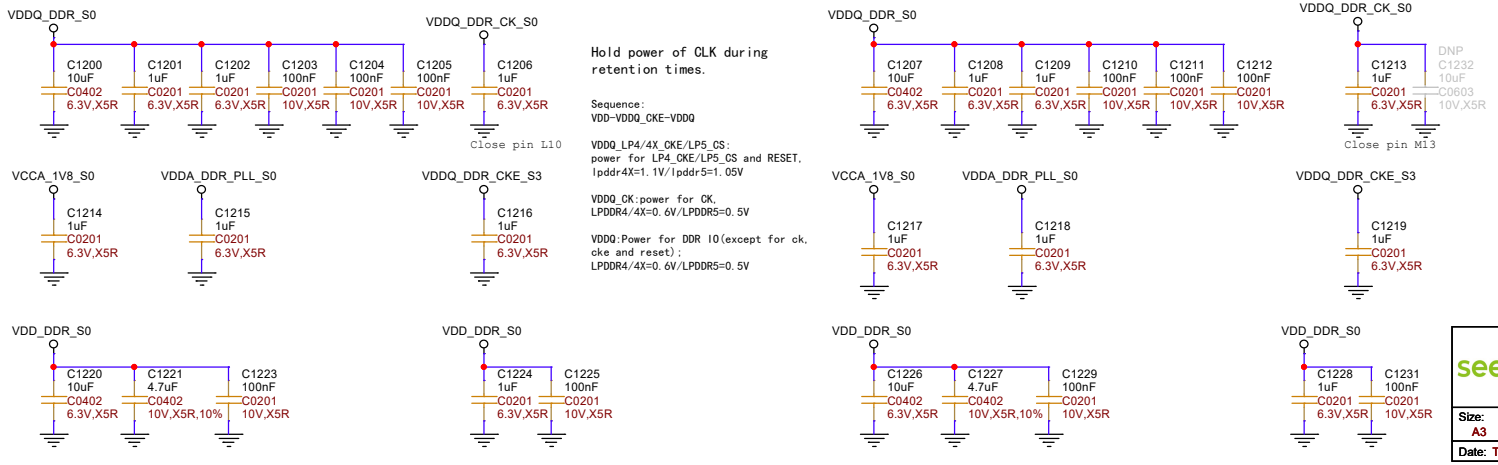


DDR FILTER



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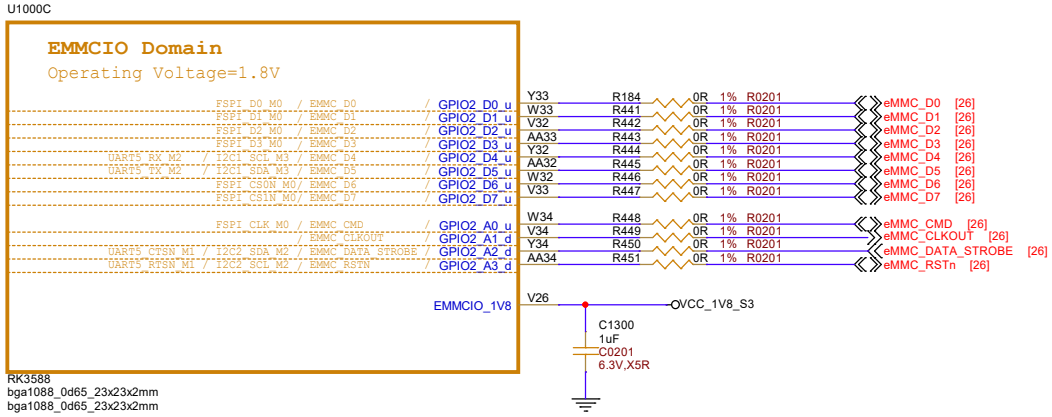
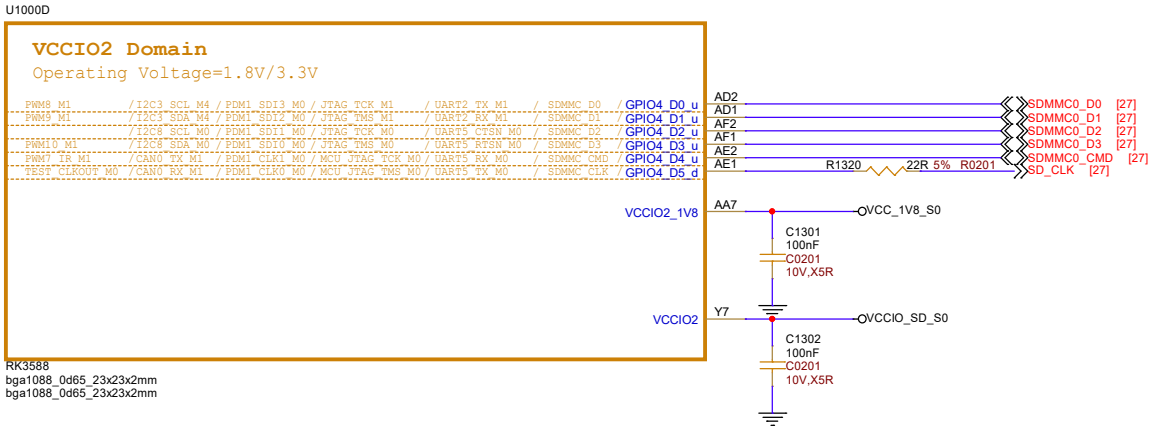
RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)



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RK3588_M(TYPEC/DP)

U1000M

Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

TYPEC0_SBU1/DP0_AUXP — AL15 — TYPEC0_SBU1 [18]
TYPEC0_SBU2/DP0_AUXN — AM15 — TYPEC0_SBU2 [18]
TYPEC0_SSRX1P/DP0_TX0P — AN13 — TYPEC0_SSRX1P [18]
TYPEC0_SSRX1N/DP0_TX0N — AP13 — TYPEC0_SSRX1N [18]
TYPEC0_SSTX1P/DP0_TX1P — AP14 — TYPEC0_SSTX1P [18]
TYPEC0_SSTX1N/DP0_TX1N — AN14 — TYPEC0_SSTX1N [18]
TYPEC0_SSRX2P/DP0_TX2P — AN15 — TYPEC0_SSRX2P [18]
TYPEC0_SSRX2N/DP0_TX2N — AP15 — TYPEC0_SSRX2N [18]
TYPEC0_SSTX2P/DP0_TX3P — AP16 — TYPEC0_SSTX2P [18]
TYPEC0_SSTX2N/DP0_TX3N — AN16 — TYPEC0_SSTX2N [18]

For Typec

TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +-10%
USB30 Differential Pair:
DATE:90 Ohm +-10%
DP Differential Pair:
DATE:100 Ohm +-10%

TYPEC0_DP0_REXT — AH16 TYPEC0_REXT — R1401 8.2K 1% R0201

TYPEC0_DP0_VDD_0V85 / TYPEC0_DP0_VDDA_0V85 — AJ14 / AH14 — VDDA_0V85_S0
C1404 1uF C0201 6.3V,X5R
C1405 100nF C0201 10V,X5R

Do not delete!!!

For USB30 For DP

TYPEC0_DP0_VDDH_1V8 — AG14 — VCCA_1V8_S0
C1406 1uF C0201 6.3V,X5R
C1407 100nF C0201 10V,X5R

VCCA_1V8_S0
R61 DNP 10K 1% R0201
[10] TYPEC0_USB20_OTG_ID — R63 DNP 100R 1% R0201
DNP R64 10K 1% R0201

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3

TYPEC1_SBU1/DP1_AUXP — AL10
TYPEC1_SBU2/DP1_AUXN — AM10
TYPEC1_SSRX1P/DP1_TX0P — AN8 — TYPEC1_SSRX1P [22]
TYPEC1_SSRX1N/DP1_TX0N — AP8 — TYPEC1_SSRX1N [22]
TYPEC1_SSTX1P/DP1_TX1P — AP9 — TYPEC1_SSTX1P [22]
TYPEC1_SSTX1N/DP1_TX1N — AN9 — TYPEC1_SSTX1N [22]
TYPEC1_SSRX2P/DP1_TX2P — AN10
TYPEC1_SSRX2N/DP1_TX2N — AP10
TYPEC1_SSTX2P/DP1_TX3P — AP11
TYPEC1_SSTX2N/DP1_TX3N — AN11

TYPEC1_DP1_REXT — AG16 TYPEC1_REXT — R1410 8.2K 1% R0201

TYPEC1_DP1_VDD_0V85 / TYPEC1_DP1_VDDA_0V85 — AH13 / AJ13 — VDDA_0V85_S0
C1419 1uF C0201 6.3V,X5R
C1420 100nF C0201 10V,X5R

TYPEC1_DP1_VDDH_1V8 — AG13 — VCCA_1V8_S0
C1422 1uF C0201 6.3V,X5R
C1423 100nF C0201 10V,X5R

Note:
If need full function of Typec1 (With DP funtion) please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)

U1000L

USB2.0 of TYPEC0 (OTG/HOST/DEVICE)

HS/FS/LS

USB20 Differential Pair:
DATE:90 Ohm +-10%

Download Port
TYPEC0_USB20_OTG_DP / TYPEC0_USB20_OTG_DM — AL12 / AM12 — TYPEC0_OTG_DP [18] / TYPEC0_OTG_DM [18]
TYPEC0_USB20_OTG_ID — AL14 =1.8V — TYPEC0_USB20_OTG_ID [10]
TYPEC0_USB20_VBUSDET — 40K — AM14 <=3.3V — TYPEC0_USB20_VBUSDET [18]
TYPEC0_USB20_OTG0_REXT — AP12 OTG0_REXT — R1400 200R 1% R0201

USB2.0 of TYPEC1 (OTG/HOST/DEVICE)

HS/FS/LS

TYPEC1_USB20_OTG_DP / TYPEC1_USB20_OTG_DM — AK9 / AL9 — TYPEC1_OTG_DP [22] / TYPEC1_OTG_DM [22]
TYPEC1_USB20_OTG_ID — AK8 — TP105
TYPEC1_USB20_VBUSDET — 40K — AL8 — TP106
TYPEC1_USB20_OTG1_REXT — AP7 OTG1_REXT — R1402 200R 1% R0201

USB2.0 HOST0

HS/FS/LS

USB20_HOST0_DP / USB20_HOST0_DM — AK6 / AL6
USB20_HOST0_REXT — AG9 HOST0_REXT — R1403 200R 1% R0201

USB2.0 HOST1

HS/FS/LS

USB20_HOST1_DP / USB20_HOST1_DM — AL7 / AM7 — USB20_HOST1_DP [33] / USB20_HOST1_DM [33]
USB20_HOST1_REXT — AH9 HOST1_REXT — R1404 200R 1% R0201

USB2.0 POWER

USB20_DVDD_0V75 — AH10 — VDD_0V75_S0
C1412 100nF C0201 10V,X5R

USB20_AVDD_1V8 — AG11 — VCCA_1V8_S0
C1418 100nF C0201 10V,X5R
C1417 1uF C0201 6.3V,X5R

USB20_AVDD_3V3 — AJ10 — VCCA_3V3_S0
C1421 100nF C0201 10V,X5R

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

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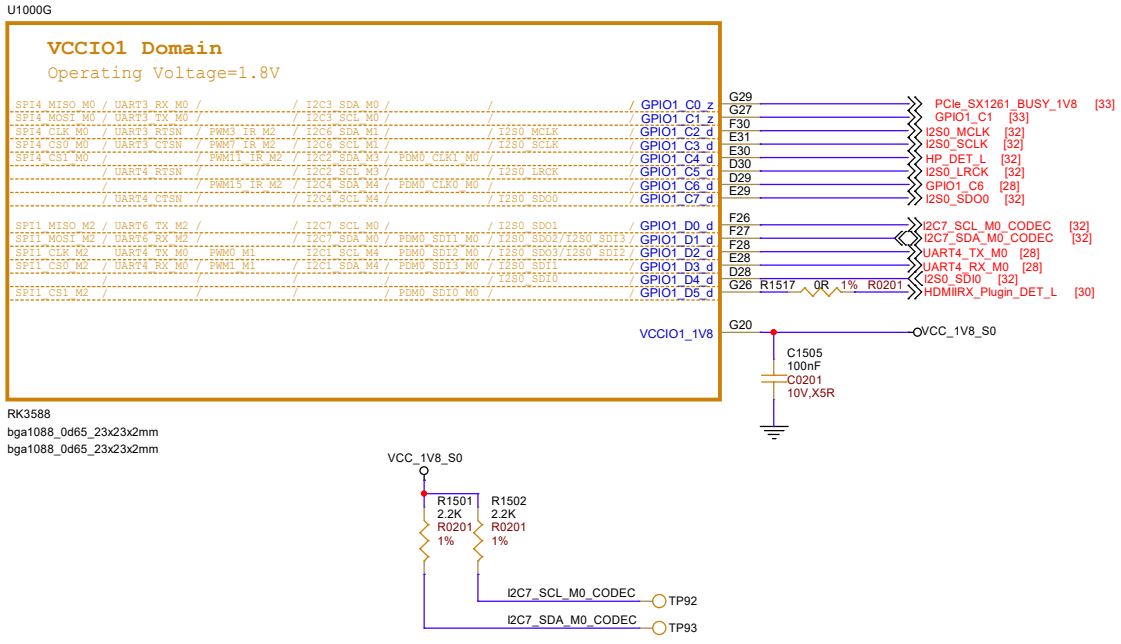
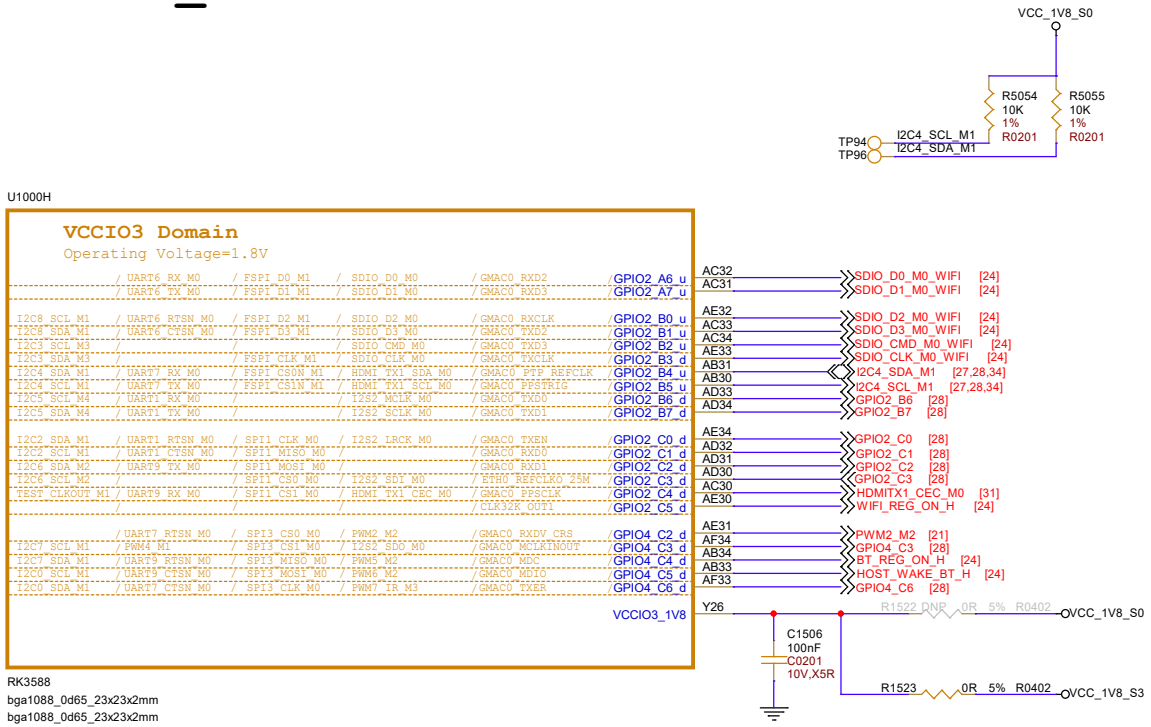
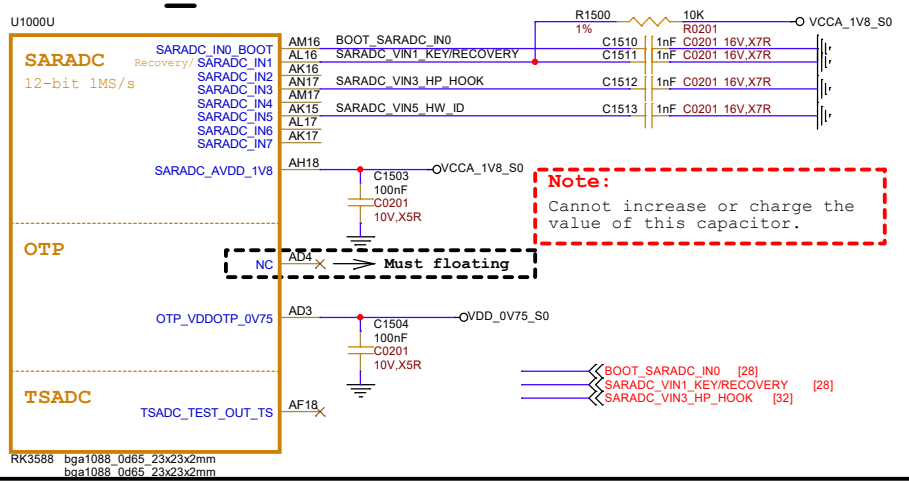
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

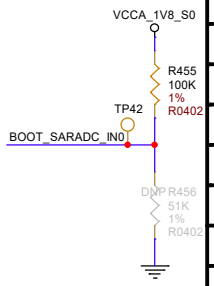


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

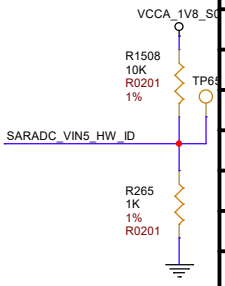


TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

Note:

If the soc is interconnected with other chips,In the scenario where the soc is not power on,isolation needs to be considered seriously to prevent the leakage to the soc through GPIO or power,which causes soc power-on sequence abnormality.

若SOC和其它芯片存在互联，在SOC未加电的情况下，需要仔细考虑隔离措施，以防止通过GPIO或电源路径向SOC漏电，这可能会导致SOC的上电时序出现异常。

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RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 2.0Gsps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26 — MIPI_DPHY0_TX_CLKP [29]
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26 — MIPI_DPHY0_TX_CLKN [29]
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24 — MIPI_DPHY0_TX_D0P [29]
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24 — MIPI_DPHY0_TX_D0N [29]
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25 — MIPI_DPHY0_TX_D1P [29]
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25 — MIPI_DPHY0_TX_D1N [29]
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27 — MIPI_DPHY0_TX_D2P [29]
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27 — MIPI_DPHY0_TX_D2N [29]
MIPI_DPHY0_TX_D3P /NO_USE_AN28 — AN28 — MIPI_DPHY0_TX_D3P [29]
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28 — MIPI_DPHY0_TX_D3N [29]

MIPI DPHY Differential Pair: 100 Ohm +-10%
MIPI CPHY Single: 50 Ohm +-10%

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 2.5Gsps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32
MIPI_DPHY0_RX_D3P /NO_USE_AN34 — AN34
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C4 1uF C0201 6.3V,X5R
MIPI_D/C_PHY0_VDD — AG20 — C1 100nF C0201 10V,X5R; C5 1uF C0201 6.3V,X5R — VDD_0V75_S0
C-PHY 5.7Gbps 0.85V
C-PHY 2.5Gbps & C-PHY 5.7Gbps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — C2 1uF C0201 6.3V,X5R — VDDA_1V2_S0
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — C1605 1uF C0201 6.3V,X5R — VCC_1V8_S0

RK3588
bga1088_0d65_23x23x2mm

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 2.0Gsps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21
MIPI_DPHY1_TX_D3P /NO_USE_AN22 — AN22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 2.5Gsps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21
MIPI_DPHY1_RX_D3P /NO_USE_AK22 — AK22
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C78 1uF C0201 6.3V,X5R
MIPI_D/C_PHY1_VDD — AG19 — C1606 100nF C0201 10V,X5R; C1607 1uF C0201 6.3V,X5R — VDD_0V75_S0
MIPI_D/C_PHY1_VDD_1V2 — AH19 — C1608 100nF C0201 10V,X5R; C1609 1uF C0201 6.3V,X5R — VDDA_1V2_S0
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — C1610 100nF C0201 10V,X5R; C1611 1uF C0201 6.3V,X5R — VCC_1V8_S0

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588
bga1088_0d65_23x23x2mm

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33/AJ34 — MIPI_CSI0_RX_CLK0P/CLK0N [29]
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33/AG34 — MIPI_CSI0_RX_D0P/D0N [29]
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33/AH34 — MIPI_CSI0_RX_D1P/D1N [29]
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33/AM34
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33/AK34 — MIPI_CSI0_RX_D2P/D2N [29]
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33/AL34 — MIPI_CSI0_RX_D3P/D3N [29]
MIPI_CSI0_AVCC0V75 — AB25 — C1600 100nF C0201 10V,X5R; C1601 1uF C0201 6.3V,X5R — VDD_0V75_S0
MIPI_CSI0_AVCC1V8 — AB26 — C1602 1uF C0201 6.3V,X5R — VCC_1V8_S0

MIPI CSI Differential Pair: 100 Ohm +-10%

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31/AJ32 — MIPI_CSI1_RX_CLK0P/CLK0N [29]
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31/AG32 — MIPI_CSI1_RX_D0P/D0N [29]
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31/AH32 — MIPI_CSI1_RX_D1P/D1N [29]
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31/AM32
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31/AK32 — MIPI_CSI1_RX_D2P/D2N [29]
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31/AL32 — MIPI_CSI1_RX_D3P/D3N [29]
MIPI_CSI1_AVCC0V75 — AA25 — C1604 1uF C0201 6.3V,X5R — VDD_0V75_S0
MIPI_CSI1_AVCC1V8 — AA26 — C1603 100nF C0201 10V,X5R — VCC_1V8_S0

Note:
建义优先使用U1000P这个模块的DPHY CSI_RX。
First use the DPHY_CSI_RX controller of U1000P.

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lanel is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lanel,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588
bga1088_0d65_23x23x2mm

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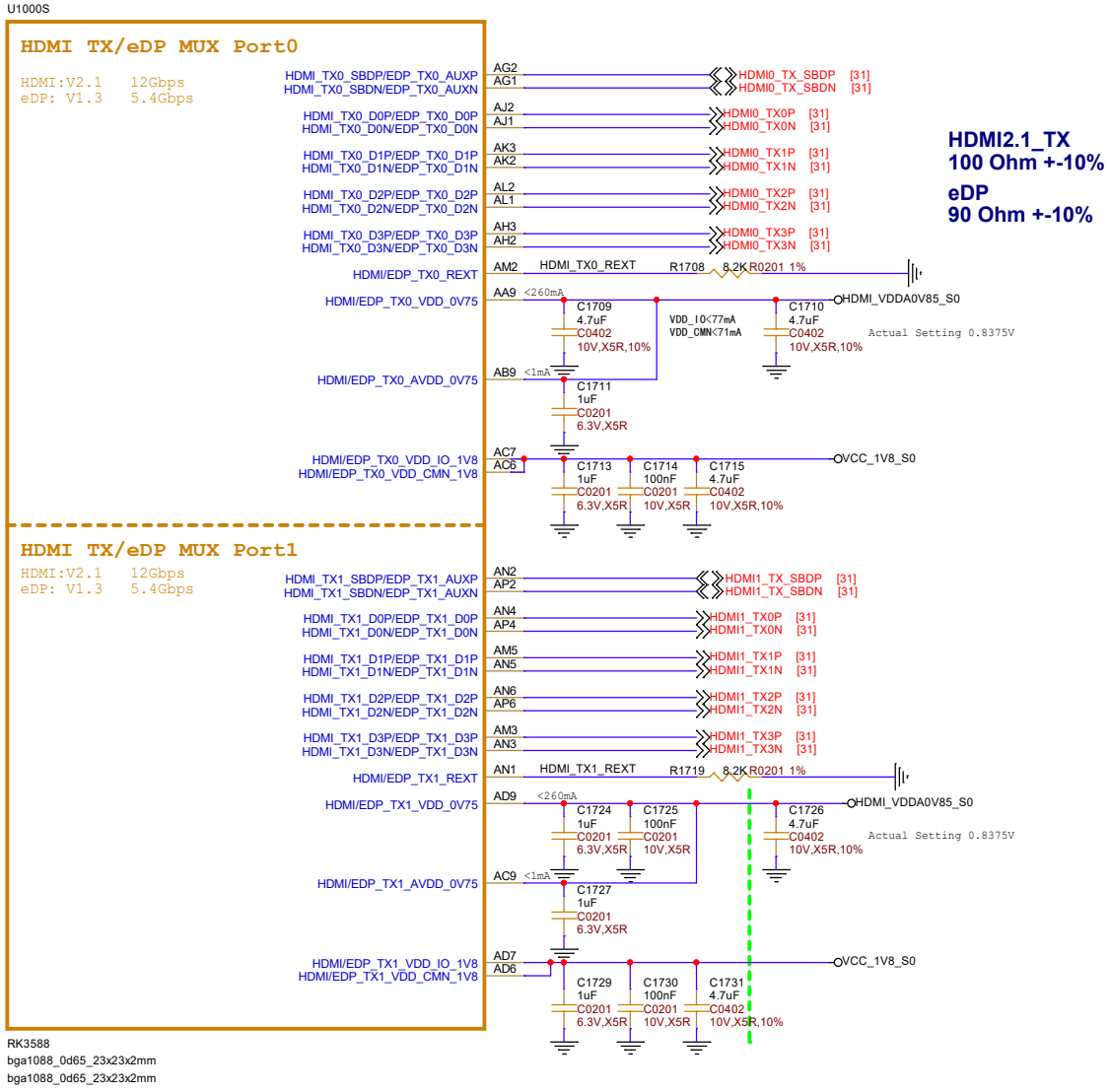
RK3588_S(HDMI2.1 TX)

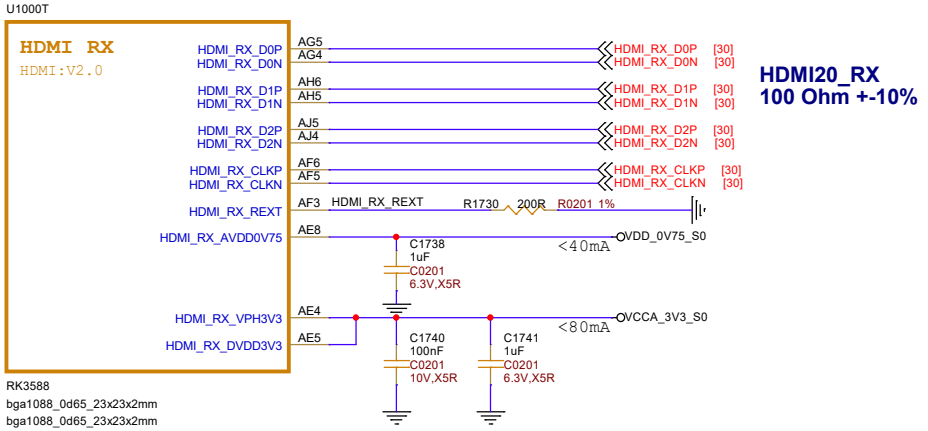
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Note:
If not used:
Signal:leave floating
Power: Floating

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RK3588_N(PCIE20)

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2 1Lane(RC)--4(1L2)

SATA30 HOST Controller0

MUX

input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN

PCIE20_0_TXP/SATA30_0_TXP / PCIE20_0_TXN/SATA30_0_TXN

PCIE20_0_RXP/SATA30_0_RXP / PCIE20_0_RXN/SATA30_0_RXN

PCIE20_SATA30_0_AVDD_0V85

PCIE20_SATA30_0_AVDD_1V8

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0 1Lane(RC)--2(1L0)

SATA30 HOST Controller1

MUX

input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN

PCIE20_1_TXP/SATA30_1_TXP / PCIE20_1_TXN/SATA30_1_TXN

PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN

PCIE20_SATA30_1_AVDD_0V85

PCIE20_SATA30_1_AVDD_1V8

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1 1Lane(RC)--3(1L1)

SATA30 HOST Controller2

USB30 HOST Controller2

MUX

input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN

PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN

PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN

PCIE20_SATA30_USB30_2_AVDD_0V85

PCIE20_SATA30_USB30_2_AVDD_1V8

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

Note:
If not used:
Signal:leave floating
Power: gnd

CLK Differential Pair:
100 Ohm±10%

DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

L32	PCIE20_0_REFCLKP	PCIE20_0_REFCLKP	[35]
L33	PCIE20_0_REFCLKN	PCIE20_0_REFCLKN	[35]
M34	PCIE20_0_TXP	PCIE20_0_TXP	[35]
M33	PCIE20_0_TXN	PCIE20_0_TXN	[35]
N33	PCIE20_0_RXP	PCIE20_0_RXP	[35]
N34	PCIE20_0_RXN	PCIE20_0_RXN	[35]

M28 — PCIE20_SATA30_0_AVDD_0V85 — VDDA_0V85_S0

C1801 10uF C0402 6.3V,X5R

PCIe20x1_2 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin AH24/AJ24/AG23
Option1 :Pin AJ25/AJ28/AK24

M27 — PCIE20_SATA30_0_AVDD_1V8 — VCCA_1V8_S0

C1803 4.7uF C0402 6.3V,X5R

H32	PCIE20_1_REFCLKP	PCIE20_1_REFCLKP	[36]
H33	PCIE20_1_REFCLKN	PCIE20_1_REFCLKN	[36]
K33	PCIE20_1_TXP	PCIE20_1_TXP	[36]
K34	PCIE20_1_TXN	PCIE20_1_TXN	[36]
J33	PCIE20_1_RXP	PCIE20_1_RXP	[36]
J34	PCIE20_1_RXN	PCIE20_1_RXN	[36]

L28 — PCIE20_SATA30_1_AVDD_0V85 — VDDA_0V85_S0

C1808 100nF C0201 10V,X5R

PCIe30x1_0 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin R30/T31/P30
Option1 :Pin AL28/AL29/AK27
Option2: Pin D27/E25/E24

L27 — PCIE20_SATA30_1_AVDD_1V8 — VCCA_1V8_S0

C1810 100nF C0201 10V,X5R

G31	PCIE20_2_REFCLKP	PCIE20_2_REFCLKP	[34]
G30	PCIE20_2_REFCLKN	PCIE20_2_REFCLKN	[34]
H30	PCIE20_2_TXP	PCIE20_2_TXP	[34]
H29	PCIE20_2_TXN	PCIE20_2_TXN	[34]
J31	PCIE20_2_RXP	PCIE20_2_RXP	[34]
J30	PCIE20_2_RXN	PCIE20_2_RXN	[34]

K28 — PCIE20_SATA30_USB30_2_AVDD_0V85 — VDDA_0V85_S0

C1816 1uF C0201 6.3V,X5R

PCIe30x1_1 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin R29/P29/T28
Option1 :Pin AL30/AK30/AM29
Option2: Pin A25/A24/C25

K27 — PCIE20_SATA30_USB30_2_AVDD_1V8 — VCCA_1V8_S0

C1819 1uF C0201 6.3V,X5R

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

Note:
每个SATA PORT最多只能扩展5个SATA，
不支持二级扩展。
Each sata port can only expand 5 sata port at most,No support level-2 expand.

PCIe支持极性反转（polarity inversion）功能，
不支持通道翻转（lane reversal）功能。
PCIe support polarity inversion function, However,it does not support lane reversal.

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4 4Lane(DM)--0(4L)

PCIe30x1_0 1Lane(RC)--2(1L0)

PCIe30x2 2Lane(RC)--1(2L)

PCIe30x1_1 1Lane(RC)--3(1L1)

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input

PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN

Lane0

PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N

PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N

Lane1

PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N

PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF

PCIE30_PORT0_AVDD0V75

PCIE30_PORT0_AVDD1V8

PCIE30 PORT1

input

PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN

Lane0

PCIE30_PORT1_TX0P / PCIE30_PORT1_TX0N

PCIE30_PORT1_RX0P / PCIE30_PORT1_RX0N

Lane1

PCIE30_PORT1_TX1P / PCIE30_PORT1_TX1N

PCIE30_PORT1_RX1P / PCIE30_PORT1_RX1N

PCIE30_PORT1_RESREF

PCIE30_PORT1_AVDD0V75

PCIE30_PORT1_AVDD1V8

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bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

CLK Differential Pair:
100 Ohm ±10%

DATA Differential Pair:
PCIE30: 85 Ohm ±10%

E33	PCIE30_PORT0_REFCLKP_IN	PCIE30_PORT0_REFCLKP_IN	[34]
E34	PCIE30_PORT0_REFCLKN_IN	PCIE30_PORT0_REFCLKN_IN	[34]
D32	PCIE30_PORT0_TX0P	PCIE30_PORT0_TX0P	[34]
D33	PCIE30_PORT0_TX0N	PCIE30_PORT0_TX0N	[34]
G33	PCIE30_PORT0_RX0P	PCIE30_PORT0_RX0P	[34]
G34	PCIE30_PORT0_RX0N	PCIE30_PORT0_RX0N	[34]
C33	PCIE30_PORT0_TX1P	PCIE30_PORT0_TX1P	[34]
C34	PCIE30_PORT0_TX1N	PCIE30_PORT0_TX1N	[34]
F32	PCIE30_PORT0_RX1P	PCIE30_PORT0_RX1P	[34]
F33	PCIE30_PORT0_RX1N	PCIE30_PORT0_RX1N	[34]

B34 — PCIE30_0_REF — R1800 200R 1% R0201

G24 — VDD_0V75_S0

C1804 1uF C0201 6.3V,X5R

C1805 4.7uF C0402 10V,X5R,10%

G23 — VCCA_1V8_S0

C1806 1uF C0201 6.3V,X5R

C1807 4.7uF C0402 10V,X5R,10%

A28	PCIE30_PORT1_REFCLKP_IN	PCIE30_PORT1_REFCLKP_IN	[34]
B28	PCIE30_PORT1_REFCLKN_IN	PCIE30_PORT1_REFCLKN_IN	[34]
B30	PCIE30_PORT1_TX2P	PCIE30_PORT1_TX2P	[34]
A30	PCIE30_PORT1_TX2N	PCIE30_PORT1_TX2N	[34]
B32	PCIE30_PORT1_RX2P	PCIE30_PORT1_RX2P	[34]
A32	PCIE30_PORT1_RX2N	PCIE30_PORT1_RX2N	[34]
C29	PCIE30_PORT1_TX3P	PCIE30_PORT1_TX3P	[34]
B29	PCIE30_PORT1_TX3N	PCIE30_PORT1_TX3N	[34]
C31	PCIE30_PORT1_RX3P	PCIE30_PORT1_RX3P	[34]
B31	PCIE30_PORT1_RX3N	PCIE30_PORT1_RX3N	[34]

A33 — PCIE30_1_REF — R1801 200R 1% R0201

H24 — VDD_0V75_S0

C1812 1uF C0201 6.3V,X5R

C1813 4.7uF C0402 10V,X5R,10%

H23 — VCCA_1V8_S0

C1814 100nF C0201 10V,X5R

C1815 4.7uF C0402 10V,X5R,10%

PCIe30x4 Controller:
Wake/clkreq/perstn Optional:
Option0: Pin V31/T29/W31
Option1 :Pin AJ26/AL26/AJ27
Option2: Pin AH25/AH26/AG26
Option3: Pin D25/C27/D26

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

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RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u	AA29 FSPI_D0 [26]
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u	AA30 FSPI_D1 [26]
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u	AD27 FSPI_D2 [26]
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u	AE27 FSPI_D3 [26]
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d	AD28 USER_LED_R [21]
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d	AH30 FSPI_CLK [26]
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d	AH27 USER_LED_G [21]
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u	AG29 LoRaWAN_SX1262_CS [33]
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u	AG28 GPIO3_B0_u [29]
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d	AH29 USER_LED_B [21]
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d	AE28 WIFI_PWREN_L [24]
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u	AC28 USB_HUB30_EN [17]
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u	AC29 GPIO3_B4_u [29]
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u	AD29 GPIO3_B5_u [29]
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d	AE29 FAN_TACH [21]
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d	AA28 I2C3_SCL_M1 [22,28,29]
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d	Y29 I2C3_SDA_M1 [22,28,29]
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d	Y27 PCIE0_PWR_0V95_EN [35,36]
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d	Y31 PCIe_SX1261_RST_3V3 [33]
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d	Y30 SYS_3V3_EN [22]
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u	AH26 FSPI_CS0 [26]
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u	AH25 HDMITX1_SDA_M1 [31]
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u	AG26 HDMITX1_SCL_M1 [31]
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u	AJ24 PCIE20_1_2_CLKREQn_M1_L [35]
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u	AH24 PCIE20_1_2_WAKEn_M1_L [35]
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d	AG23 HDMI_RX_CEC [30]
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d	AG25 HDMI_RX_SCL_M1 [30]
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d	AG24 HDMI_RX_SDA_M1 [30]
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d	AA27 HDMIIRX_HPDOUT_H [30]
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d	AB28 GPIO3_D5 [29]

VCCIO5_1V8 — W25 — C3 100nF C0201 10V,X5R — VCC_1V8_S0

VCCIO5 — W26 — C1901 100nF C0201 10V,X5R — VCC_3V3_S0

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

VCC_3V3_S0 — R465 2.2K R0201 1% — R466 2.2K R0201 1%

I2C3_SCL_M1 — TP95

I2C3_SDA_M1 — TP97

Note:

If the soc is interconnected with other chips,In the scenario where the soc is not power on,isolation needs to be considered seriously to prevent the leakage to the soc through GPIO or power,which causes soc power-on sequence abnormality.

若SOC和其它芯片存在互联，在SOC未加电的情况下，需要仔细考虑隔离措施，以防止通过GPIO或电源路径向SOC漏电，这可能会导致SOC的上电时序出现异常。

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1			I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d	AK30 PCIEX1_1_CLKREQn_M1_L [34]
	SPI0_MOSI_M1	UART9_CTSN_M1			I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d	AL30 PCIEX1_1_WAKEn_M1_L [34]
	SPI0_CLK_M1				I2S1_LRCK_M0	PCIE30X1_1_PERSTn_M1	BT1120_D2	CIF_D2	GPIO4_A2_d	AM29 PCIEX1_1_PERSTn_M1_L [34]
		UART0_TX_M2				PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d	AL29 PCIE30x1_0_CLKREQn_M1_L [36]
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2			PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d	AL28 PHONE_CTL [32]
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2		I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d	AK27 PCIE30x1_0_PERSTn_M1_L [36]
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2		I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d	AL27 TYPEC0_SBU1_DC [18]
	SPI2_CS0_M1		I2C5_SDA_M2		I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d	AM27 TYPEC0_SBU2_DC [18]
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3		I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d	AK26 GPIO4_B0 [28]
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3	I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA0_CLK_M0	GPIO4_B1_u	AL24 HDMI0_TX_ON_H [31]
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3	I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u	AK25 HDMI1_TX_ON_H [31]
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3	I2S1_SDO2_M0	PCIE30X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u	AM25 LTE_RESET [33]
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1		I2S1_SDI3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u	AL26 PCIE30X4_CLKREQn_M1_L [34]
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1		HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d	AJ26 PCIE30X4_WAKEn_M1_L [34]
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1	HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d	AJ27 PCIE30X4_PERSTn_M1_L [34]
		SPI3_CLK_M1		I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u	AJ28 HDMITX0_SCL_M0 [31]
		SPI3_CS0_M1		I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u	AJ25 HDMITX0_SDA_M0 [31]
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d	AK24 HDMITX0_CEC_M0 [31]

VCCIO6_1V8 — AC25 — C1902 100nF C0201 10V,X5R — VCC_1V8_S0

VCCIO6 — AC26 — C1905 100nF C0201 10V,X5R — VCC_3V3_S0

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2		I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d	A24 UART6_TX_M1_BT [24]
SATA1_ACT_LED_M1		SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2		I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d	A25 UART6_RX_M1_BT [24]
	PWM0_M2	SPI4_CLK_M2		VOP_POST_EMPTY		I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d	A26 UART6_RTSn_M1_BT [24]
	PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2		I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d	A27 UART6_CTSn_M1_BT [24]
		SPI2_MISO_M0		HDMI_TX1_SCL_M2				GPIO1_A4_d	B25 PECIE30_CLK_EN [34]
		SPI2_MOSI_M0		HDMI_TX0_HPD_M0				GPIO1_A5_d	B26 HDMITX0_HPDIN_M0 [31]
		SPI2_CLK_M0		HDMI_TX1_HPD_M0				GPIO1_A6_d	C24 HDMITX1_HPDIN_M0 [31]
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2			PDM1_SDI0_M1		GPIO1_A7_u	C25 GPIO1_A7_u [28]
		SPI2_CS1_M0	PCIE30X4_CLKREQN_M3			PDM1_SDI1_M1		GPIO1_B0_u	C27 GPIO1_B0_u [28]
		SPI0_MISO_M2	PCIE30X4_WAKEN_M3			PDM1_SDI2_M1		GPIO1_B1_d	D25 SDMMC_PWREN [27]
		SPI0_MOSI_M2	PCIE30X4_PERSTN_M3			PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d	D26 TYPEC5V_PWREN_H [18]
SATA0_ACT_LED_M1		SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2			PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d	D27 GPIO1_B3 [28]
		SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2			PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u	E24 GPIO1_B4_u [28]
		SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2				UART7_TX_M2	GPIO1_B5_u	E25 GPIO1_B5_u [28]
	HDMI_RX_HPDOUT_M2	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0		I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u	E26 M2M1_ALERT_N [34]
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u	E27 GPIO1_B7_u [28]
	HDMI_RX_SCL_M2	PWM14_M2			MIPI_CAMERA3_CLK_M0	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u	F24 GPIO1_D6_u [28]
	HDMI_RX_SDA_M2	PWM15_IR_M3		PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u	F25 GPIO1_D7_u [28]

VCCIO4_1V8 — H20 — C1903 100nF C0201 10V,X5R — VCC_1V8_S0

VCCIO4 — H21

RK3588
bga1088_0d65_23x23x2mm
bga1088_0d65_23x23x2mm

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	Title: RK3588_AIOT_SCH	
Size: A2	Document Number: 15.RK3588_1.8V/ 3.3V GPIO	Rev: V1.0
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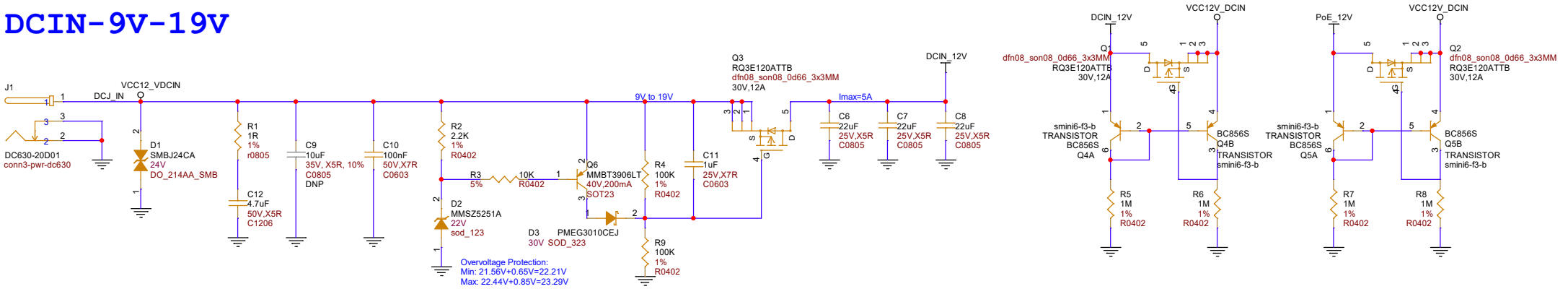
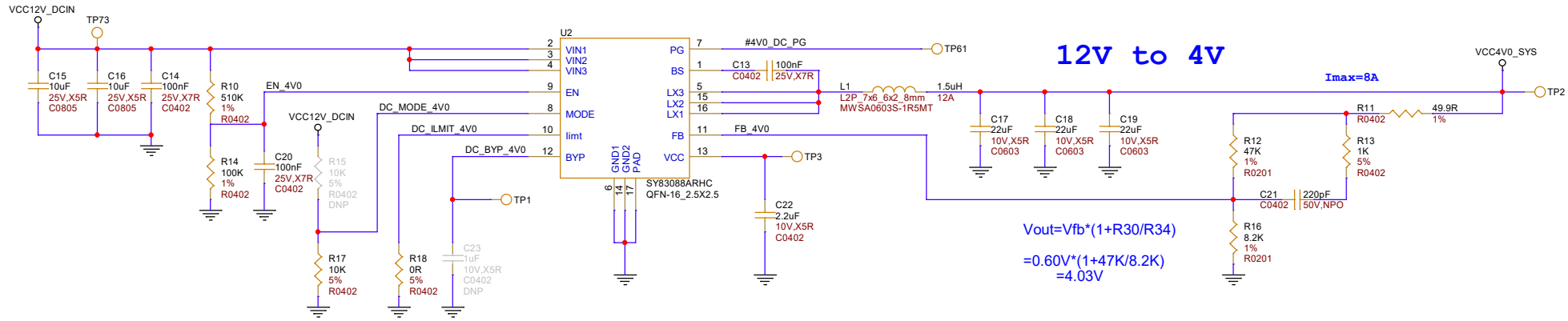
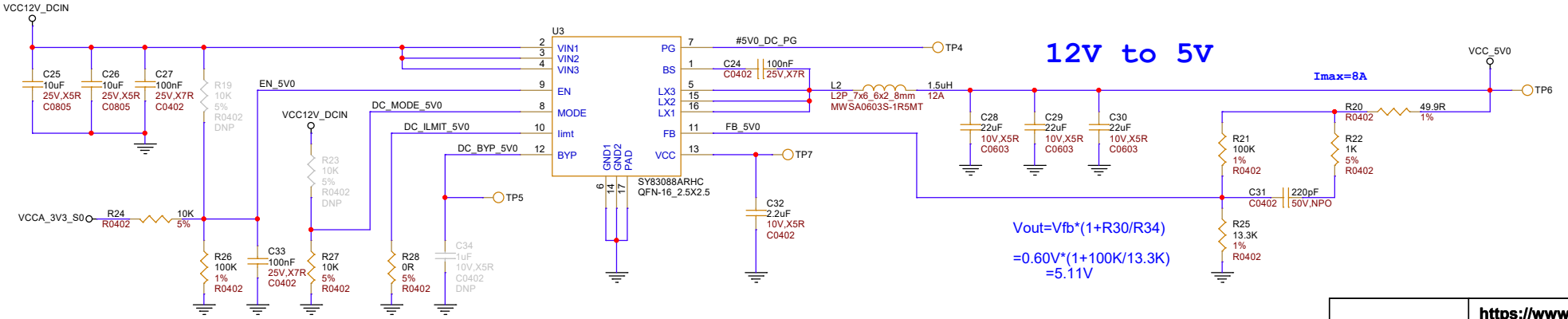
DCIN-9V-19V



VCC4V0_SYS



VCC5V0_SYS



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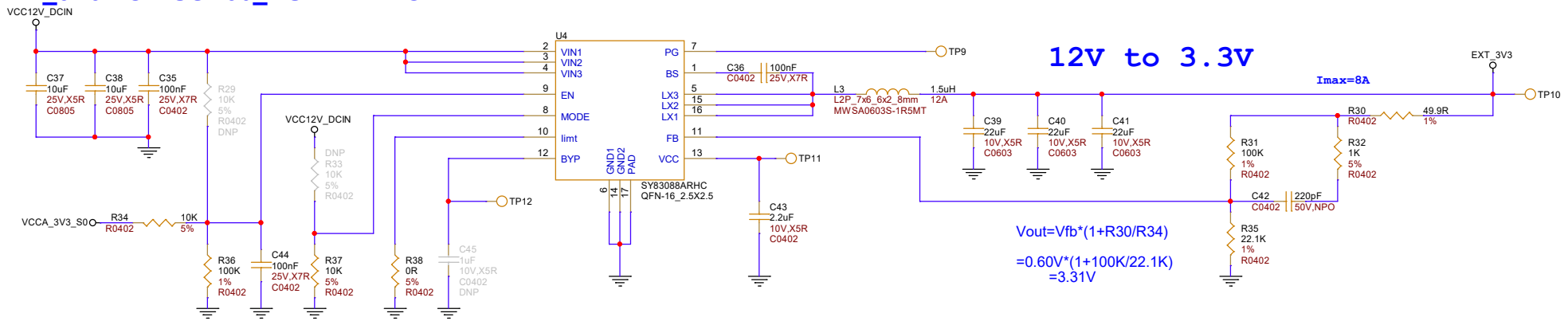
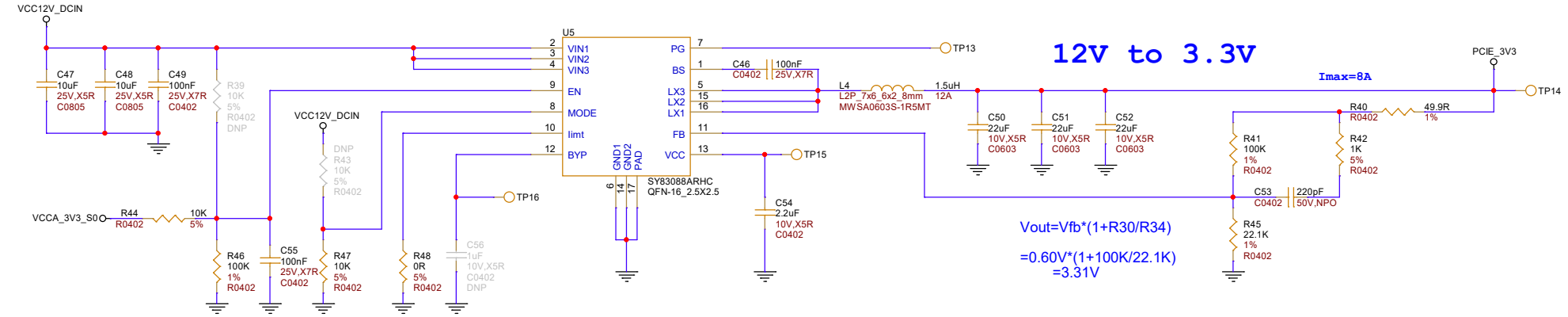
	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 16.DC IN/VCC4V0_SYS/VCC_5V0	Rev: V1.0
Date: Tuesday, January 20, 2026		Sheet: 16 of 37

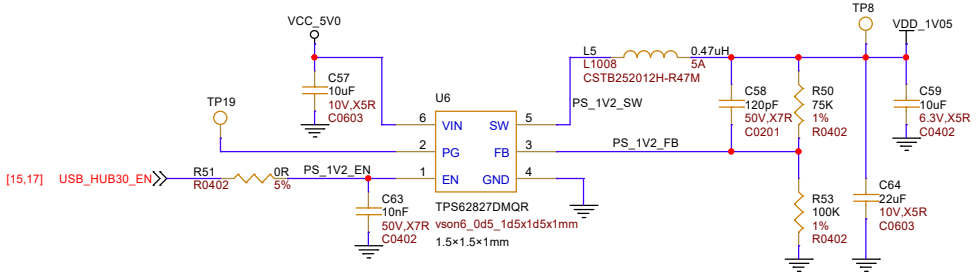
EXT_3V3 FOR USB30_HUB PHY 4G



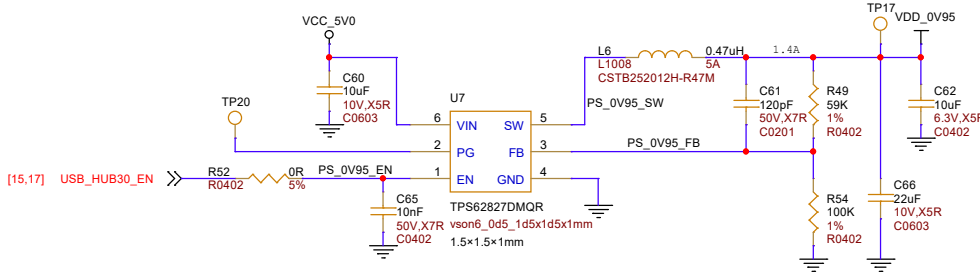
EXT_3V3 FOR SSD



VDD_1V05 FOR USB_HUB30



VDD_0.95V FOR RTL8215BG



seeed studio	https://www.seeedstudio.com	
	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 17.EXT/PCIE_3V3/VDD_1V0/VDD_V95	Rev: V1.0
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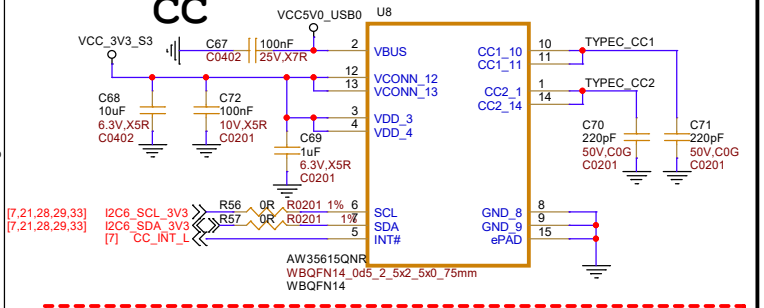
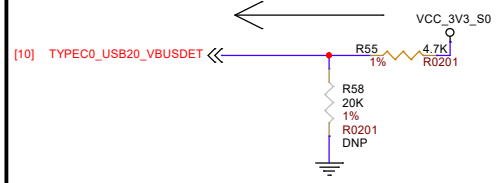
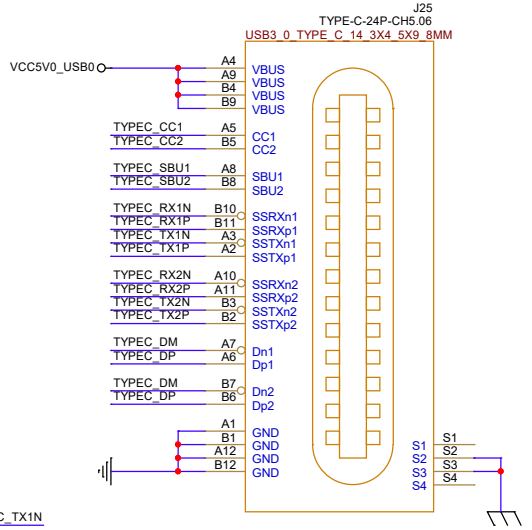
CC

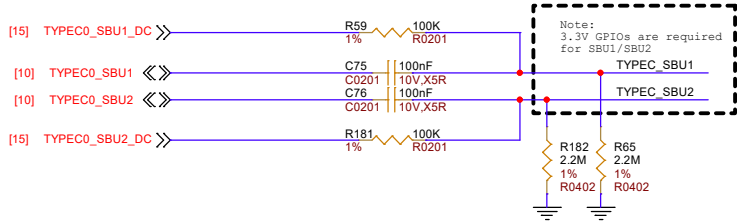


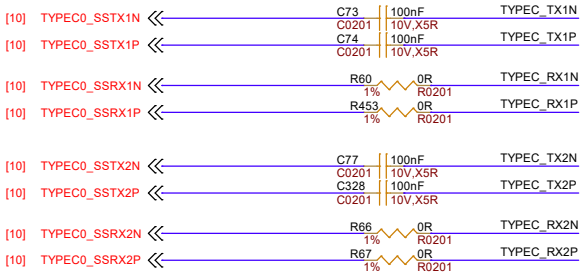
Note:
Different models of CC chips may require different driver software.

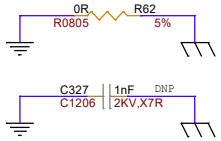
	AW35615(Default)	HUSB311(Option)
7bit address	0x22	0x4E
VBUS	4V~21V,TYP=5V	4V~21V,TYP=5V
VDD	2.7V~5.5V,TYP=3.3V	3V~5.5V,TYP=3.3V
VCONN	2.7V~5.5V	3V~5.5V

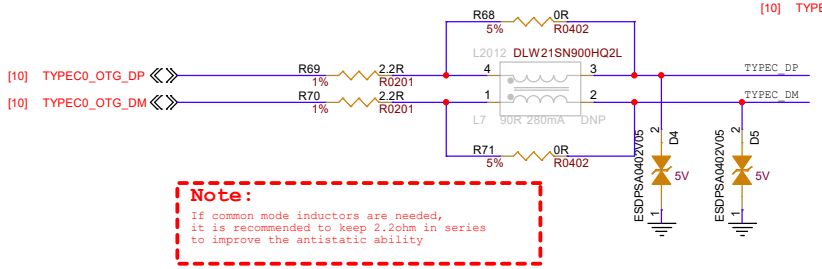






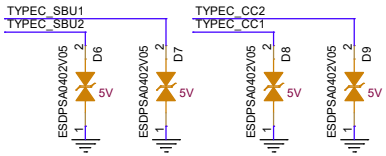


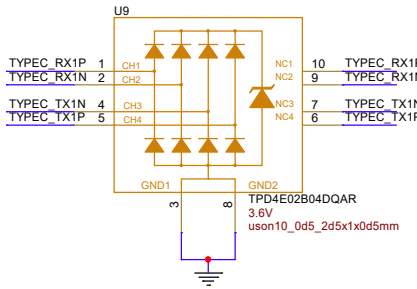


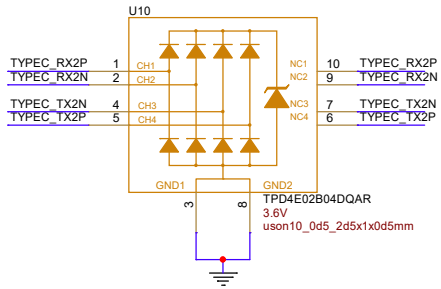


Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability

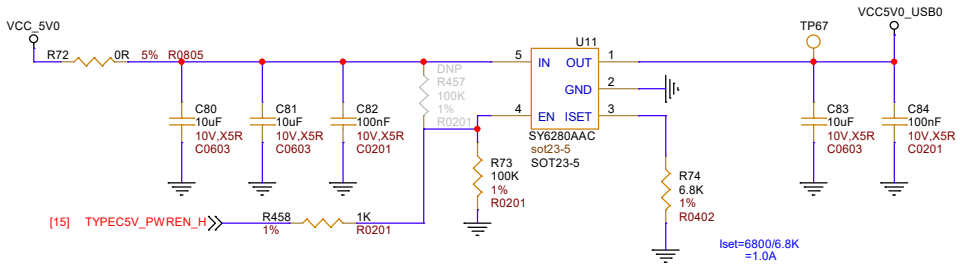
Cj<=0.2pF







USB POWER



Design Note:
1. Pull up to enable USB Power.

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Title: RK3588_AIOT_SCH

Size: A3	Document Number: 18.USB0-Type C Port With DP Alt	Rev: V1.0
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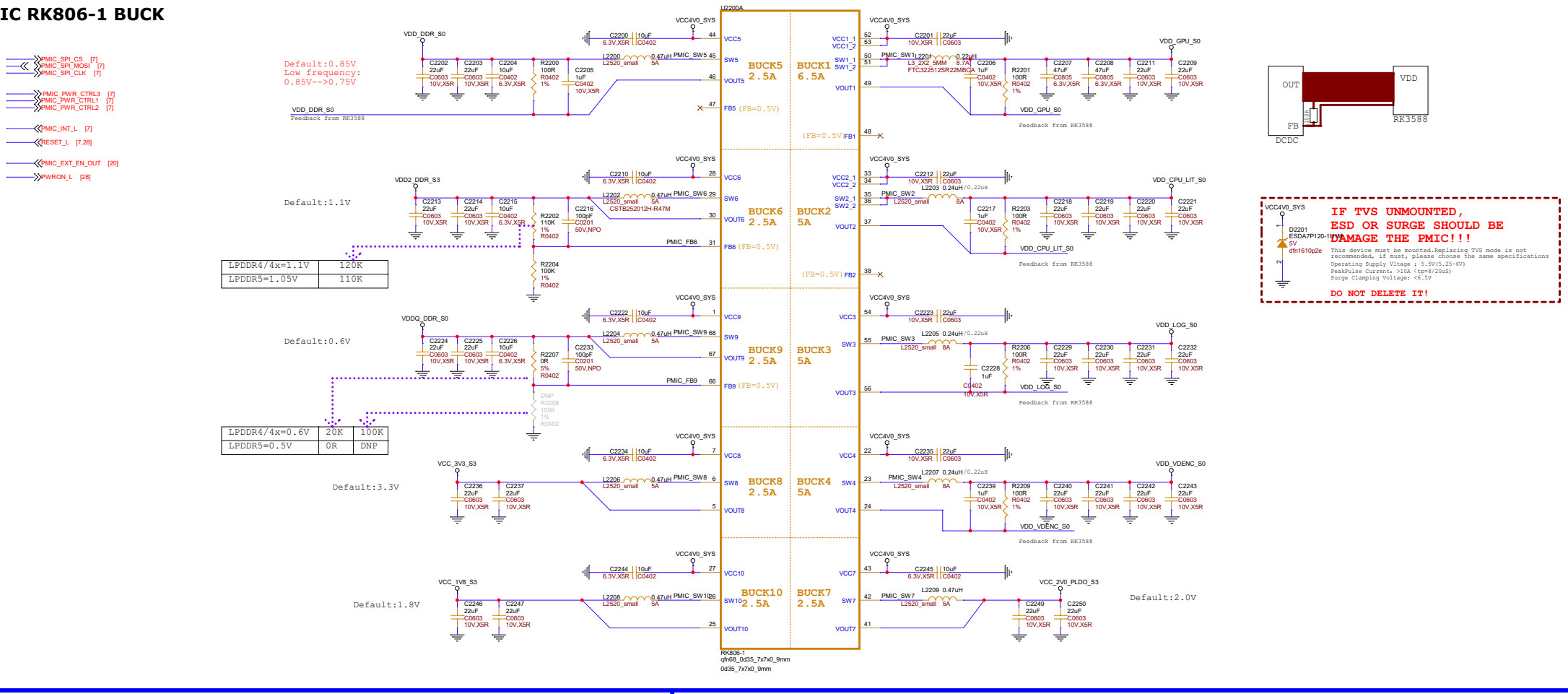
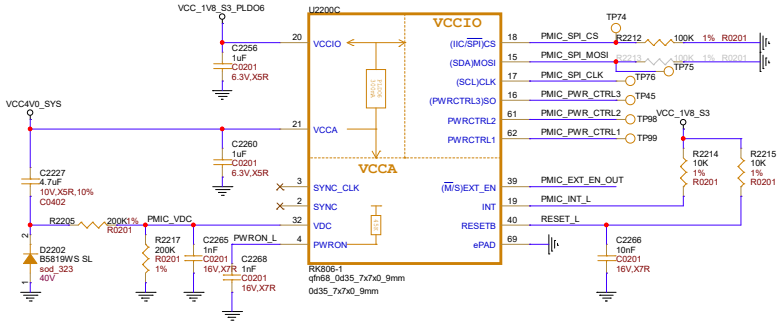
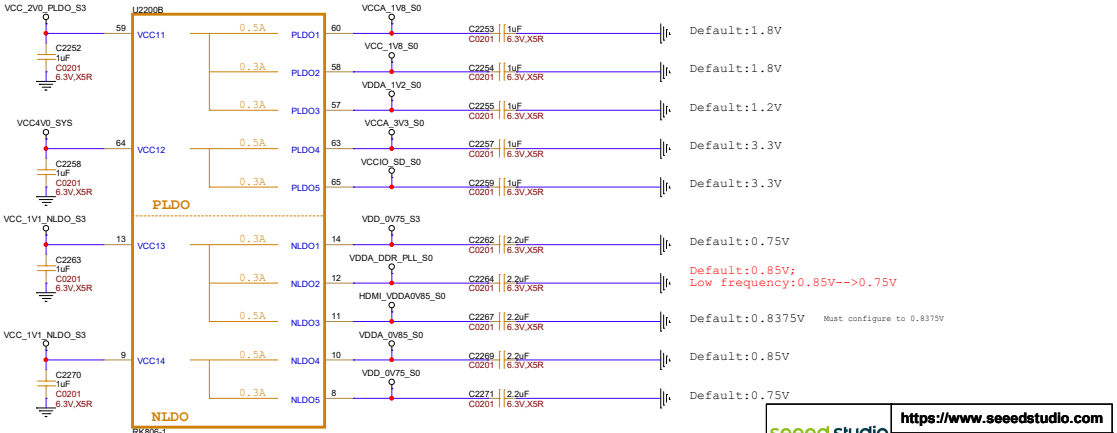
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



PMIC RK806-1 LDO



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Title: RK3588_AIOT_SCH

Size: A2	Document Number: 19.Power-PMIC_RK806-1	Rev: V1.0
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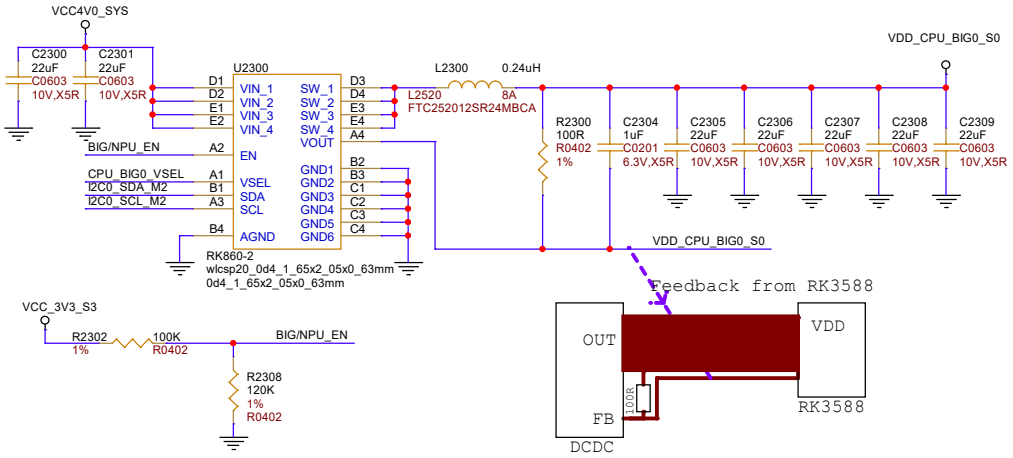
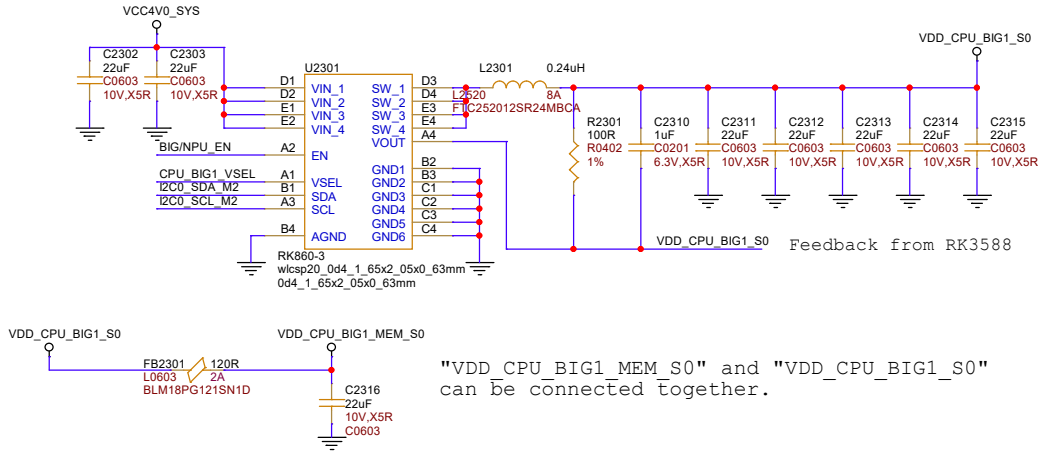
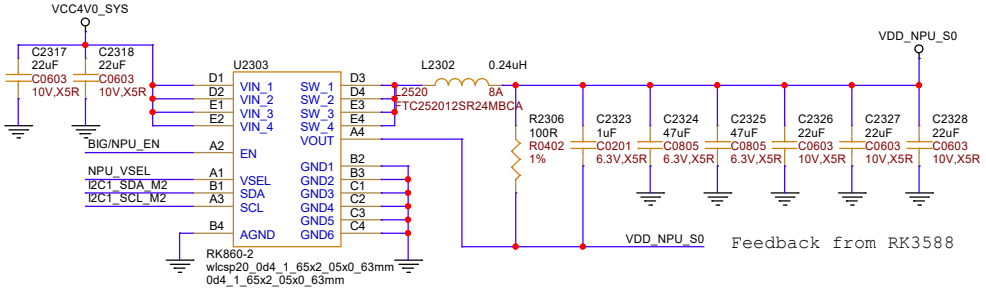
VDD_CPU_BIG0



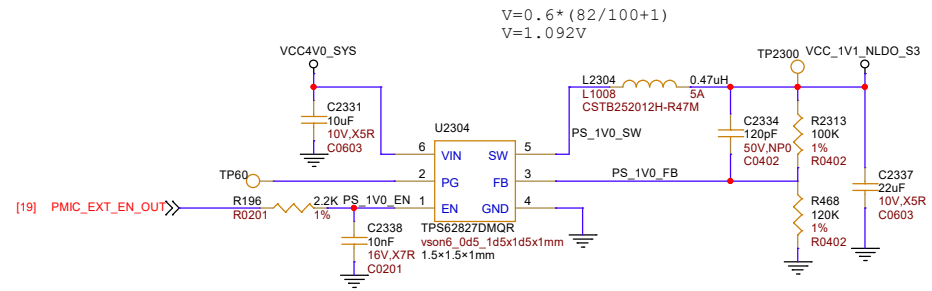
VDD_CPU_BIG1

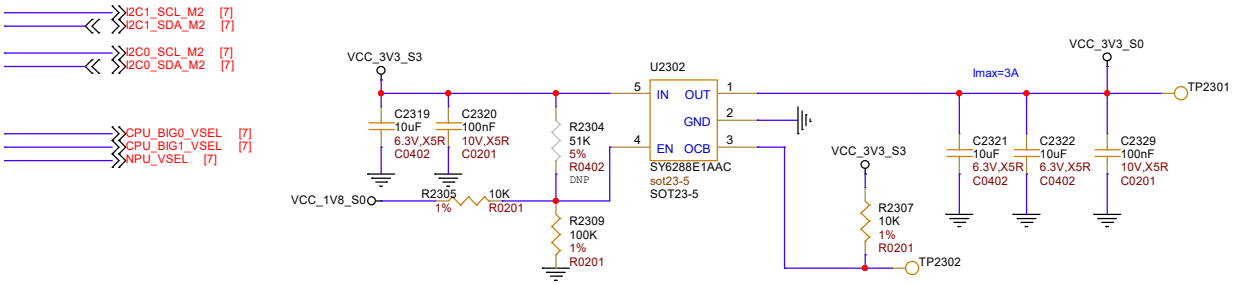


VDD_NPU



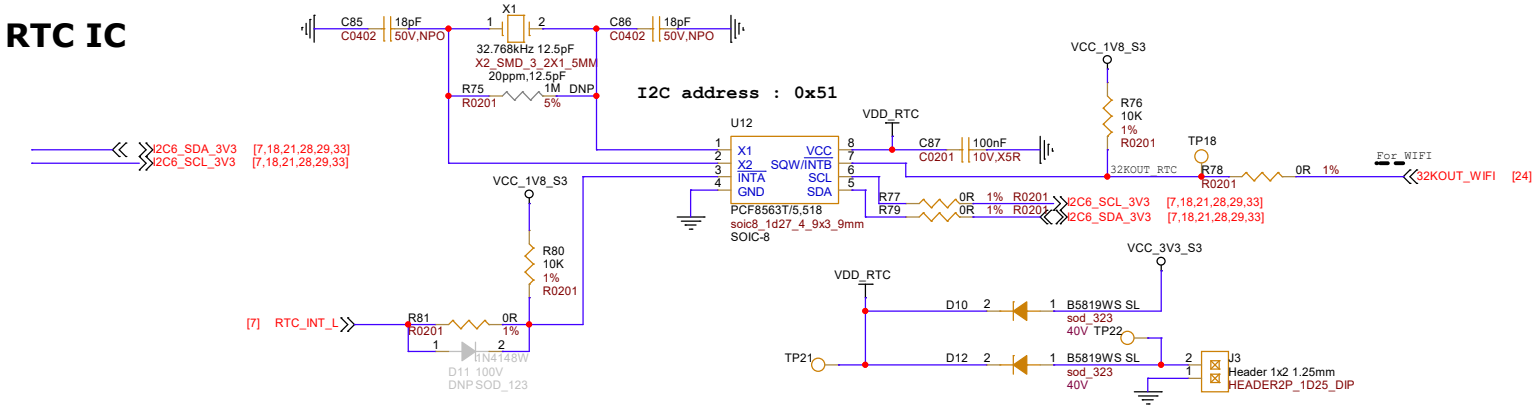
VCC_1V1_NLDO_S3



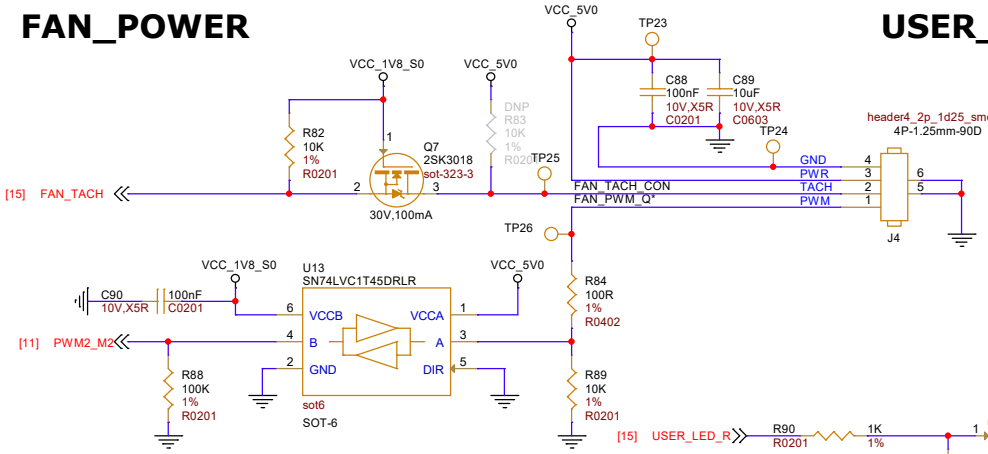


seeed studio	https://www.seeedstudio.com	
	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 20.Power_Ext Discrete	Rev: V1.0
Date: Tuesday, January 20, 2026		Sheet: 20 of 37

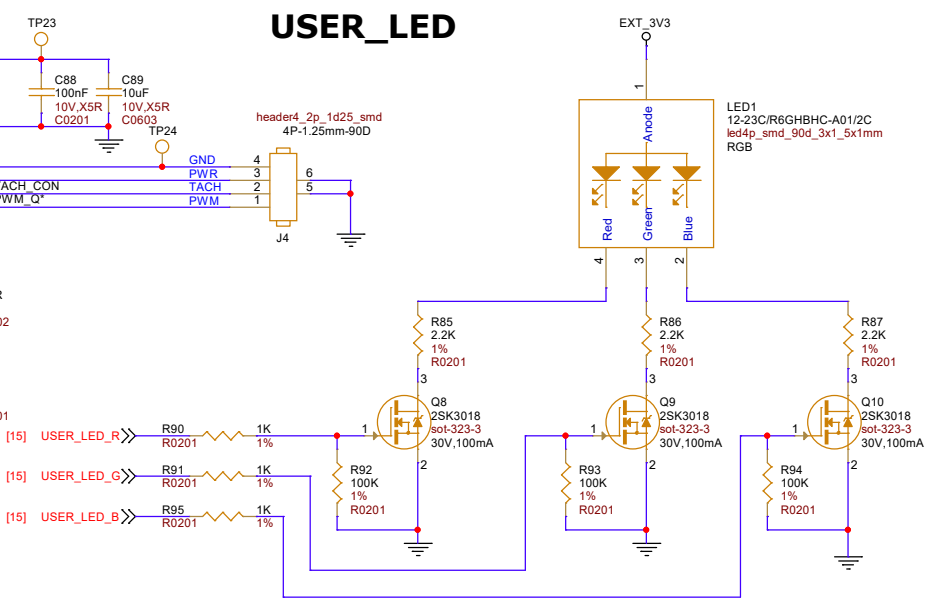
RTC IC

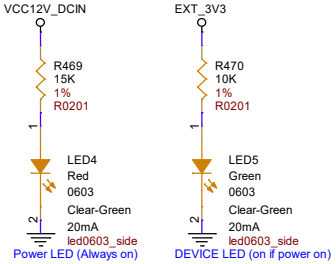


FAN_POWER



USER_LED





seeed studio	https://www.seeedstudio.com	
	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 21.RTC/FAN/LED	Rev: V1.0
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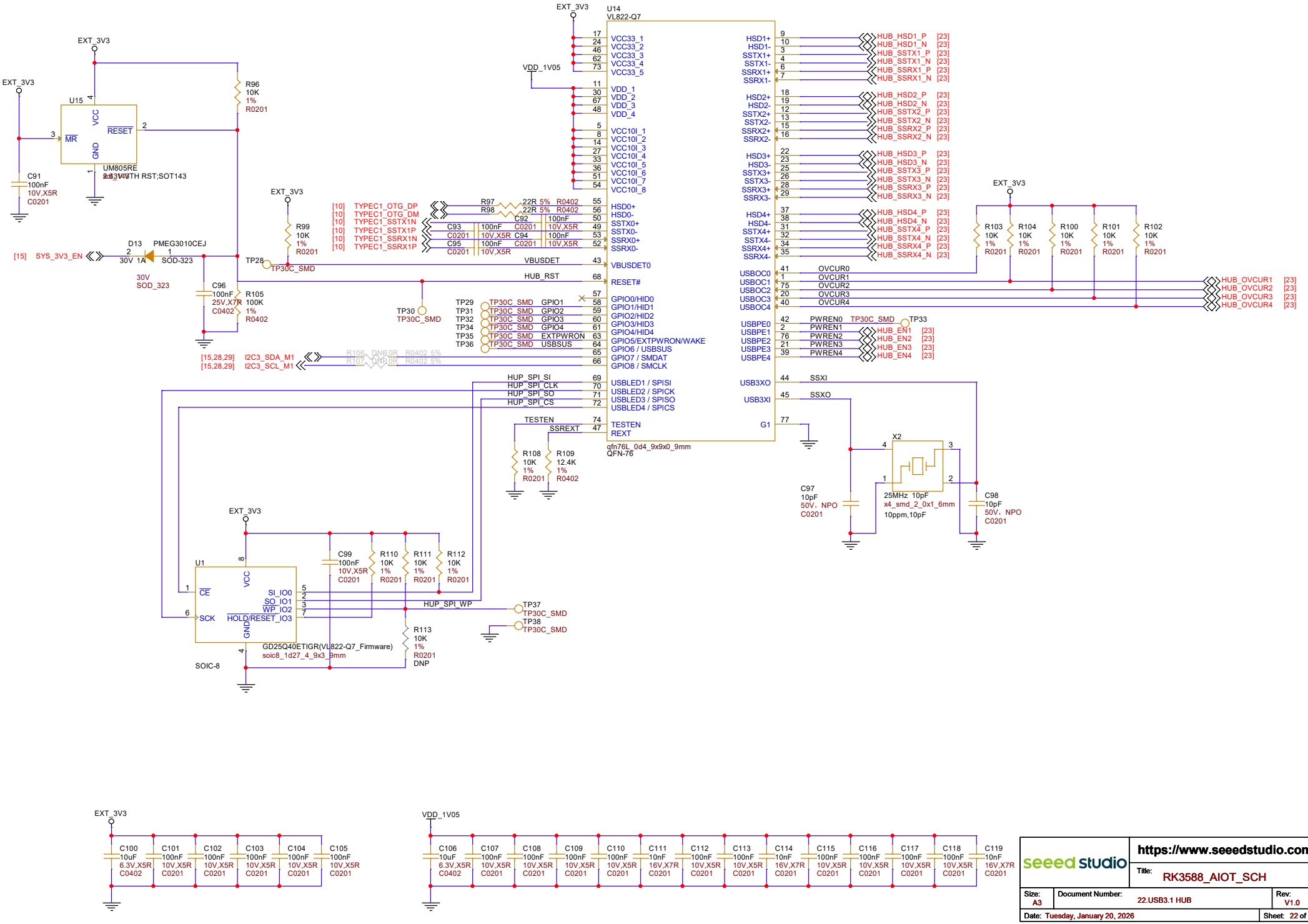
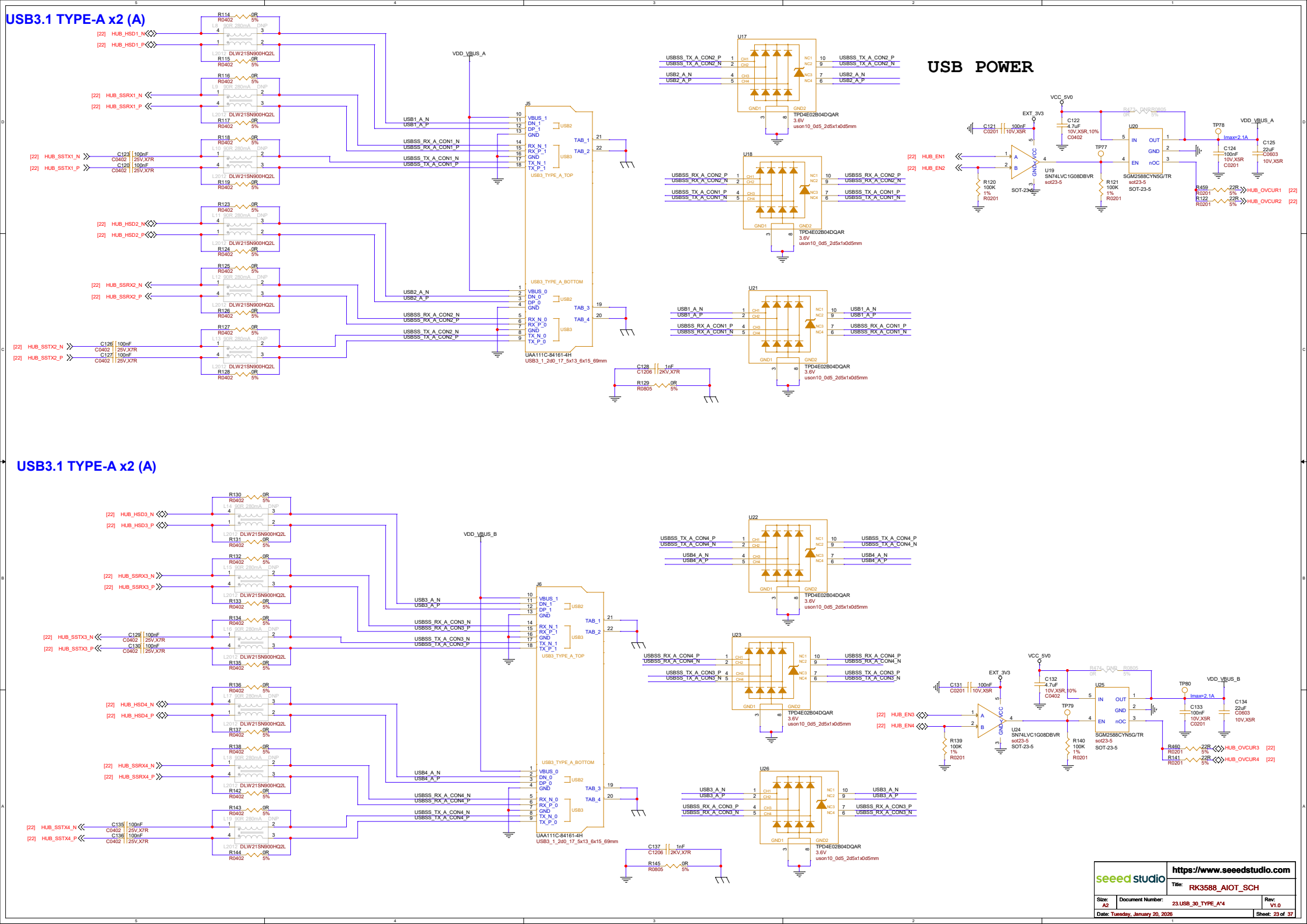

EXT_3V3
U14
VL822-Q7
VDD_1V05
VCC33_1
VCC33_2
VCC33_3
VCC33_4
VCC33_5
VDD_1
VDD_2
VDD_3
VDD_4
VCC10I_1
VCC10I_2
VCC10I_3
VCC10I_4
VCC10I_5
VCC10I_6
VCC10I_7
VCC10I_8
HSD0+
HSD0-
SSTX0+
SSTX0-
SSRX0+
SSRX0-
VBUSDET0
RESET#
GPIO0/HID0
GPIO1/HID1
GPIO2/HID2
GPIO3/HID3
GPIO4/HID4
GPIO5/EXTPWRON/WAKE
GPIO6 / USBSUS
GPIO7 / SMDAT
GPIO8 / SMCLK
USBLED1 / SPISI
USBLED2 / SPICK
USBLED3 / SPISO
USBLED4 / SPICS
TESTEN
REXT
qfn76L_0d4_9x9x0_9mm
QFN-76
HSD1+
HSD1-
SSTX1+
SSTX1-
SSRX1+
SSRX1-
HSD2+
HSD2-
SSTX2+
SSTX2-
SSRX2+
SSRX2-
HSD3+
HSD3-
SSTX3+
SSTX3-
SSRX3+
SSRX3-
HSD4+
HSD4-
SSTX4+
SSTX4-
SSRX4+
SSRX4-
USBOC0
USBOC1
USBOC2
USBOC3
USBOC4
OVCUR0
OVCUR1
OVCUR2
OVCUR3
OVCUR4
USBPE0
USBPE1
USBPE2
USBPE3
USBPE4
PWREN0
PWREN1
PWREN2
PWREN3
PWREN4
USB3XO
USB3XI
G1
SSXI
SSXO
HUB_HSD1_P [23]
HUB_HSD1_N [23]
HUB_SSTX1_P [23]
HUB_SSTX1_N [23]
HUB_SSRX1_P [23]
HUB_SSRX1_N [23]
HUB_HSD2_P [23]
HUB_HSD2_N [23]
HUB_SSTX2_P [23]
HUB_SSTX2_N [23]
HUB_SSRX2_P [23]
HUB_SSRX2_N [23]
HUB_HSD3_P [23]
HUB_HSD3_N [23]
HUB_SSTX3_P [23]
HUB_SSTX3_N [23]
HUB_SSRX3_P [23]
HUB_SSRX3_N [23]
HUB_HSD4_P [23]
HUB_HSD4_N [23]
HUB_SSTX4_P [23]
HUB_SSTX4_N [23]
HUB_SSRX4_P [23]
HUB_SSRX4_N [23]
HUB_OVCUR1 [23]
HUB_OVCUR2 [23]
HUB_OVCUR3 [23]
HUB_OVCUR4 [23]
HUB_EN1 [23]
HUB_EN2 [23]
HUB_EN3 [23]
HUB_EN4 [23]
R103 10K 1% R0201
R104 10K 1% R0201
R100 10K 1% R0201
R101 10K 1% R0201
R102 10K 1% R0201
X2
25MHz 10pF
x4_smd_2_0x1_6mm
10ppm,10pF
C97 10pF 50V, NPO C0201
C98 10pF 50V, NPO C0201
U15
UM805RE
SOT143
VCC
RESET
MR
GND
R96 10K 1% R0201
C91 100nF 10V,X5R C0201
D13 PMEG3010CEJ
30V 1A
SOD-323
[15] SYS_3V3_EN
C96 100nF 25V,X7R C0402
R105 100K 1% R0402
R99 10K 1% R0201
TP28 TP30C_SMD
[10] TYPEC1_OTG_DP
[10] TYPEC1_OTG_DM
[10] TYPEC1_SSTX1N
[10] TYPEC1_SSTX1P
[10] TYPEC1_SSRX1N
[10] TYPEC1_SSRX1P
R97 22R 5% R0402
R98 22R 5% R0402
C92 100nF
C93 100nF C0201 10V,X5R
C94 100nF C0201 10V,X5R
C95 100nF C0201 10V,X5R
VBUSDET
HUB_RST
TP29 TP30C_SMD GPIO1
TP31 TP30C_SMD GPIO2
TP32 TP30C_SMD GPIO3
TP34 TP30C_SMD GPIO4
TP35 TP30C_SMD EXTPWRON
TP36 TP30C_SMD USBSUS
TP30 TP30C_SMD
TP33 TP30C_SMD
[15,28,29] I2C3_SDA_M1
[15,28,29] I2C3_SCL_M1
R106 DNP 0R R0402 5%
R107 DNP 0R R0402 5%
HUP_SPI_SI
HUP_SPI_CLK
HUP_SPI_SO
HUP_SPI_CS
HUP_SPI_WP
TESTEN
SSREXT
R108 10K 1% R0201
R109 12.4K 1% R0402
U1
GD25Q40ETIGR(VL822-Q7_Firmware)
soic8_1d27_4_9x3_9mm
SOIC-8
CE
SCK
SI_IO0
SO_IO1
WP_IO2
HOLD/RESET_IO3
C99 100nF 10V,X5R C0201
R110 10K 1% R0201
R111 10K 1% R0201
R112 10K 1% R0201
R113 10K 1% R0201 DNP
TP37 TP30C_SMD
TP38 TP30C_SMD
C100 10uF 6.3V,X5R C0402
C101 100nF 10V,X5R C0201
C102 100nF 10V,X5R C0201
C103 100nF 10V,X5R C0201
C104 100nF 10V,X5R C0201
C105 100nF 10V,X5R C0201
C106 10uF 6.3V,X5R C0402
C107 100nF 10V,X5R C0201
C108 100nF 10V,X5R C0201
C109 100nF 10V,X5R C0201
C110 100nF 10V,X5R C0201
C111 10nF 16V,X7R C0201
C112 100nF 10V,X5R C0201
C113 100nF 10V,X5R C0201
C114 10nF 16V,X7R C0201
C115 100nF 10V,X5R C0201
C116 100nF 10V,X5R C0201
C117 100nF 10V,X5R C0201
C118 100nF 10V,X5R C0201
C119 10nF 16V,X7R C0201
seeed studio
https://www.seeedstudio.com
Title: RK3588_AIOT_SCH
Size: A3
Document Number: 22.USB3.1 HUB
Rev: V1.0
Date: Tuesday, January 20, 2026
Sheet: 22 of 37


USB3.1 TYPE-A x2 (A)
USB POWER
USB3.1 TYPE-A x2 (A)
seeed studio
https://www.seeedstudio.com
Title: RK3588_AIOT_SCH
Size: A2
Document Number: 23.USB_30_TYPE_A*4
Rev: V1.0
Date: Tuesday, January 20, 2026
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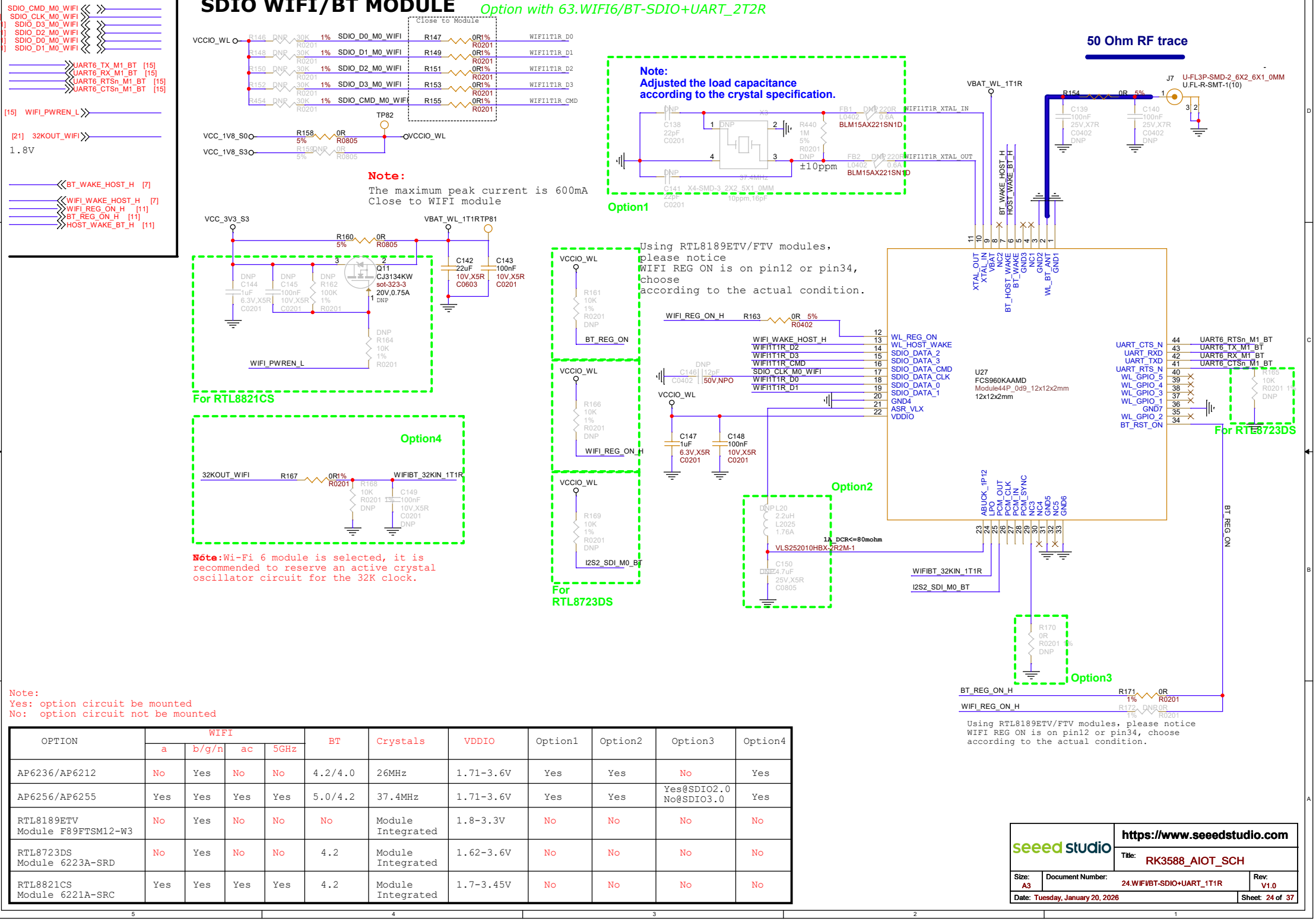
SDIO WIFI/BT MODULE

Option with 63.WIFI6/BT-SDIO+UART_2T2R



Note:
Yes: option circuit be mounted
No: option circuit not be mounted

OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

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	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 24.WIFI/BT-SDIO+UART_1T1R	Rev: V1.0
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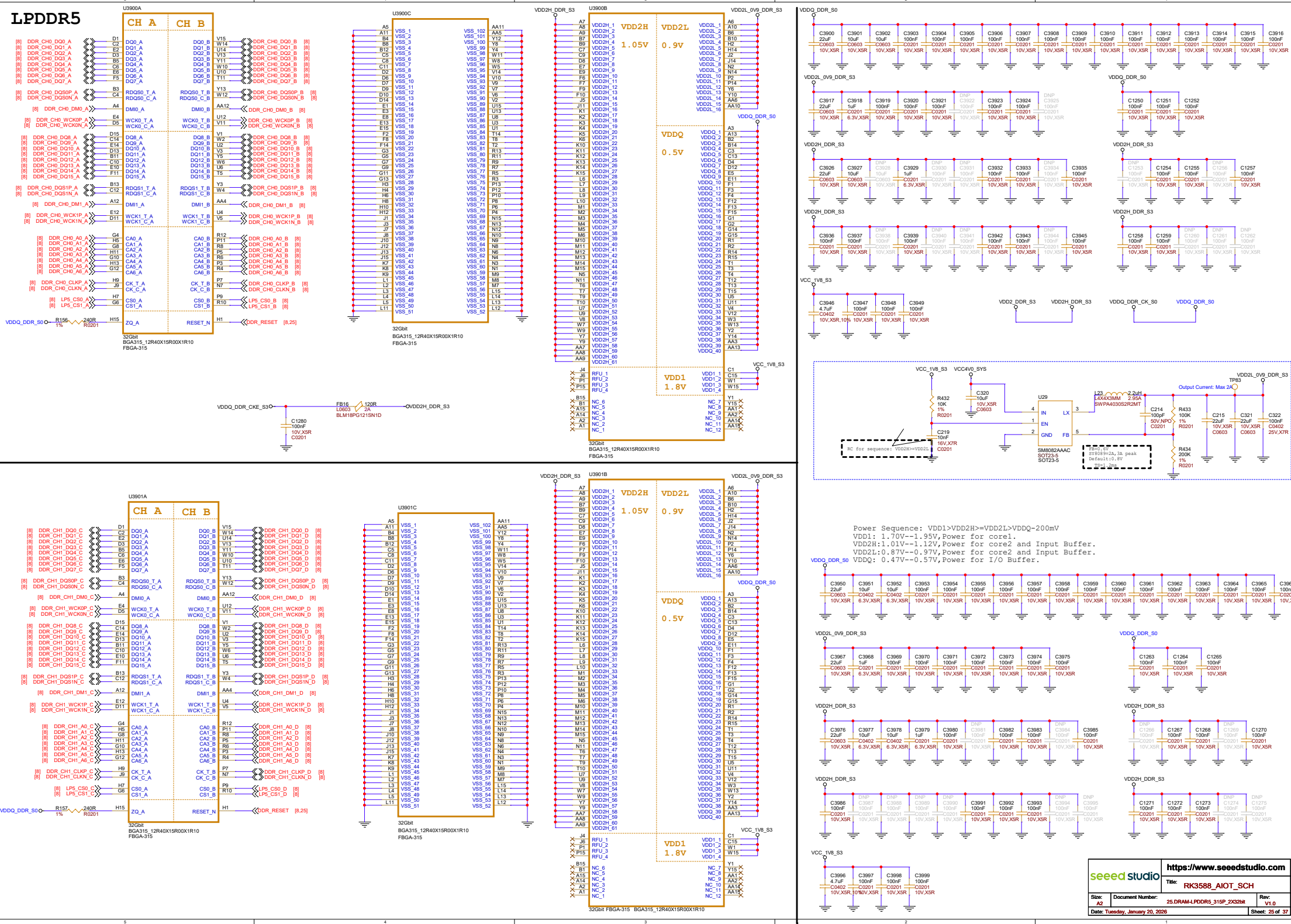
LPDDR5


U3900A
CH A
CH B
32Gbit
BGA315_12R40X15R00X1R10
FBGA-315
U3900C
32Gbit
BGA315_12R40X15R00X1R10
FBGA-315
U3900B
VDD2H
1.05V
VDD2L
0.9V
VDDQ
0.5V
VDD1
1.8V
32Gbit
BGA315_12R40X15R00X1R10
FBGA-315
VDDQ_DDR_S0
VDD2L_0V9_DDR_S3
VDD2H_DDR_S3
VCC_1V8_S3
VDDQ_DDR_CKE_S3
FB16
120R
2A
BLM18PG121SN1D
C1280
100nF
10V,X5R
C0201
U3901A
CH A
CH B
32Gbit
BGA315_12R40X15R00X1R10
FBGA-315
U3901C
32Gbit
BGA315_12R40X15R00X1R10
FBGA-315
U3901B
VDD2H
1.05V
VDD2L
0.9V
VDDQ
0.5V
VDD1
1.8V
32Gbit FBGA-315 BGA315_12R40X15R00X1R10
VCC_1V8_S3
VCC4V0_SYS
U29
SM8082AAAC
SOT23-5
SOT23-5
L23
2.2uH
L4X4X3MM
2.95A
SWPA4030S2R2MT
Output Current: Max 2A
VDD2L_0V9_DDR_S3
TP83
RC for sequence: VDD2H>=VDD2L
FB=0.6V
SY8089=2A,3A peak
Default:0.85V
FB=1.2MΩ
Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.
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https://www.seeedstudio.com
Title:
RK3588_AIOT_SCH
Size:
A2
Document Number:
25.DRAM-LPDDR5_315P_2X32bit
Rev:
V1.0
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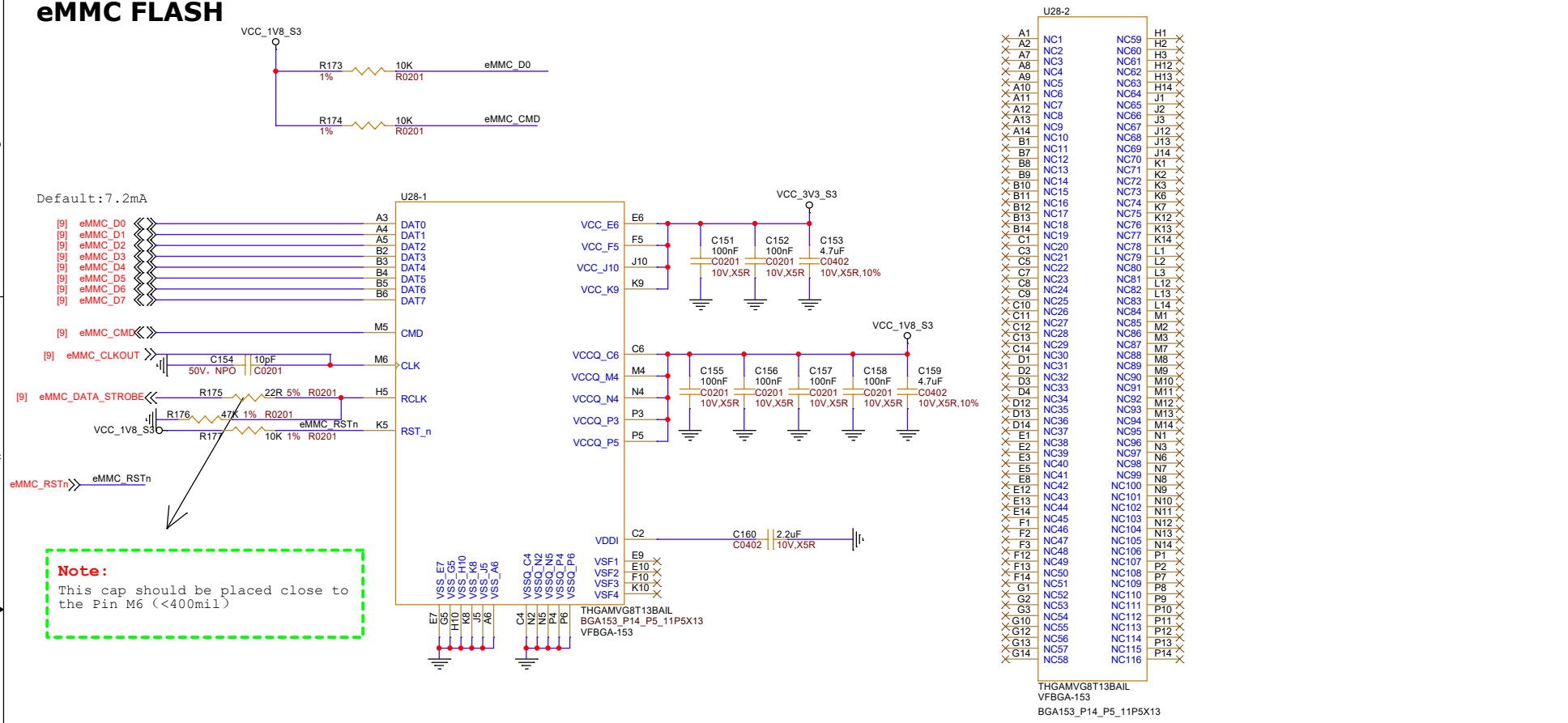
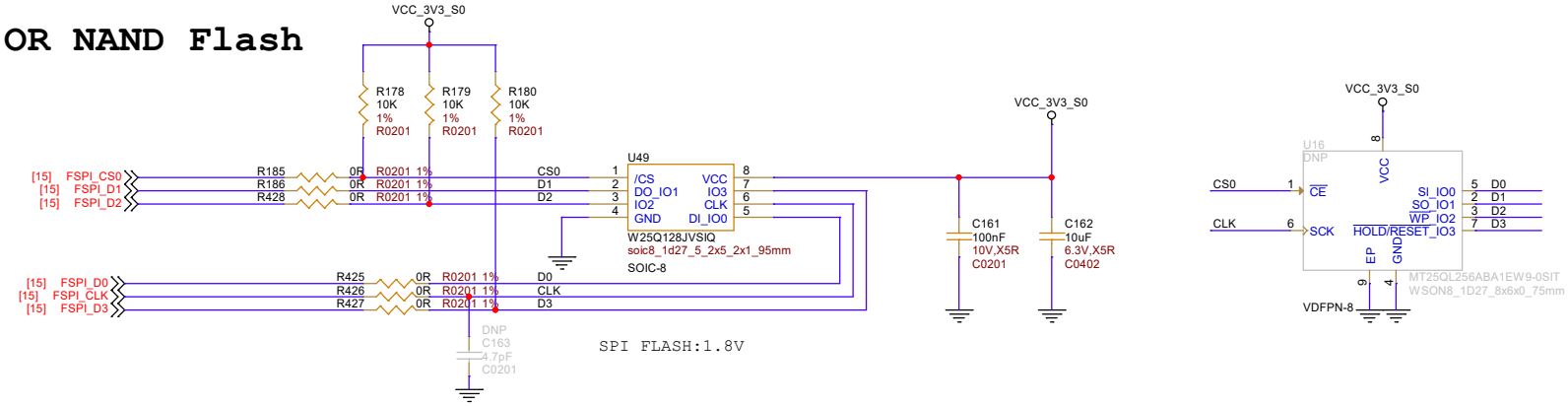
eMMC FLASH



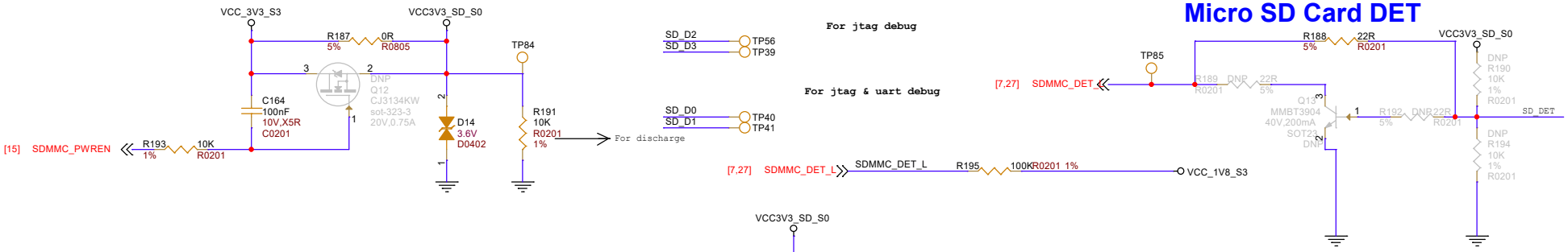
SPI NOR OR NAND Flash

SPI FLASH

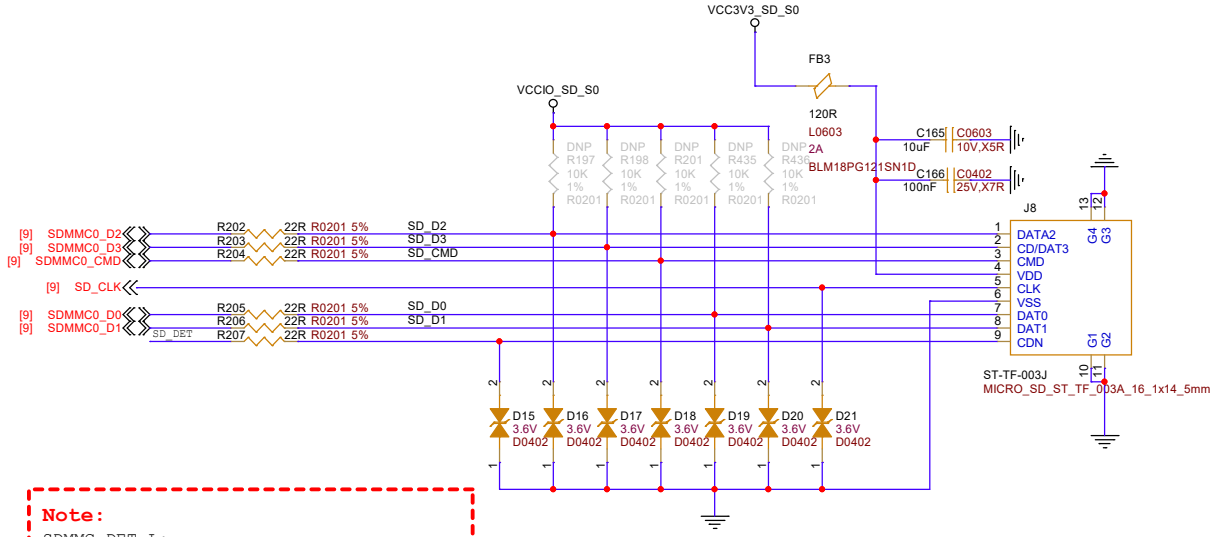


seeed studio	https://www.seeedstudio.com	
	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 26.Flash-eMMC Flash/SPI Flash	Rev: V1.0
Date: Tuesday, January 20, 2026		Sheet: 26 of 37

TF CARD



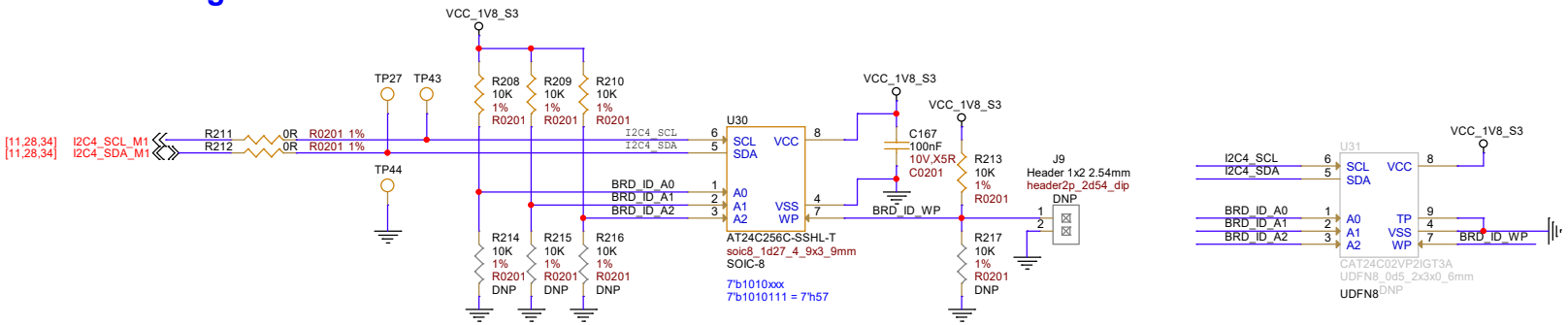
Micro SD Card Holder



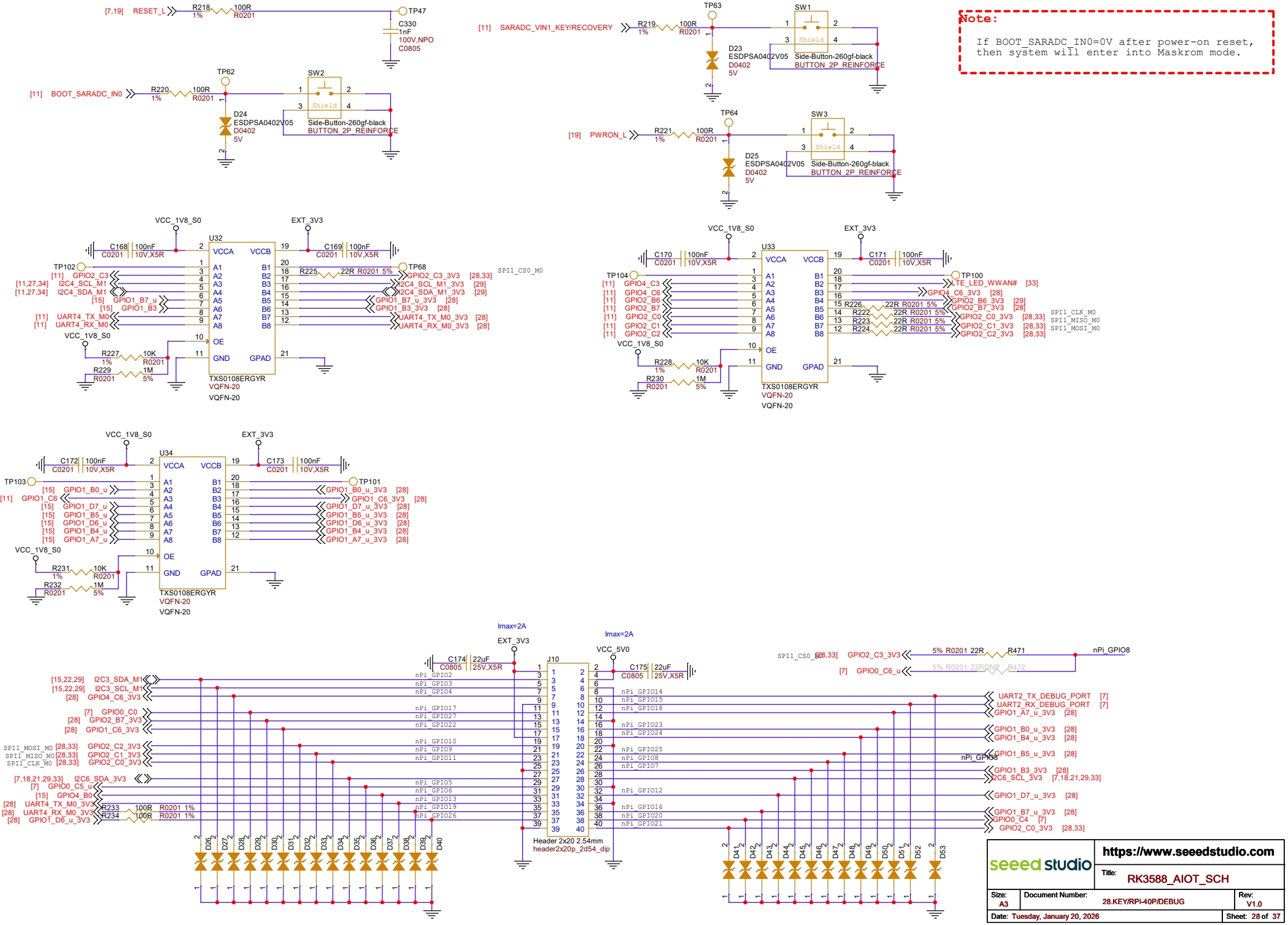
Note:

SDMMC_DET_L:
SDCARD PLUG: Must be pull-down to GND
SDCARD UNPLUG:Must be pull-up to 1.8V.

Carrier Board Config



seeed studio	https://www.seeedstudio.com	
	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 27.Flash-TF Card/EEPROM	Rev: V1.0
Date: Tuesday, January 20, 2026		Sheet: 27 of 37


[7,19] RESET_L
R218 1% 100R R0201
TP47
C330 1nF 100V,NPO C0805
[11] BOOT_SARADC_IN0
R220 1% 100R R0201
TP62
SW2
D24 ESDPSA0402V05 D0402 5V
Side-Button-260gf-black BUTTON_2P_REINFORCE
[11] SARADC_VIN1_KEY/RECOVERY
R219 1% 100R R0201
TP63
SW1
D23 ESDPSA0402V05 D0402 5V
Side-Button-260gf-black BUTTON_2P_REINFORCE
[19] PWRON_L
R221 1% 100R R0201
TP64
SW3
D25 ESDPSA0402V05 D0402 5V
Side-Button-260gf-black BUTTON_2P_REINFORCE
Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.
VCC_1V8_S0
EXT_3V3
U32
C168 100nF 10V,X5R C0201
C169 100nF 10V,X5R C0201
TP102
[11] GPIO2_C3
[11,27,34] I2C4_SCL_M1
[11,27,34] I2C4_SDA_M1
[15] GPIO1_B7_u
[15] GPIO1_B3
[11] UART4_TX_M0
[11] UART4_RX_M0
R225 22R R0201 5%
TP68
GPIO2_C3_3V3 [28,33]
I2C4_SCL_M1_3V3 [29]
I2C4_SDA_M1_3V3 [29]
GPIO1_B7_u_3V3 [28]
GPIO1_B3_3V3 [28]
UART4_TX_M0_3V3 [28]
UART4_RX_M0_3V3 [28]
SPI1_CS0_M0
R227 1% 10K R0201
R229 R0201 1M 5%
TXS0108ERGYR
VQFN-20
VCC_1V8_S0
EXT_3V3
U33
C170 C0201 100nF 10V,X5R
C171 C0201 100nF 10V,X5R
TP104
[11] GPIO4_C3
[11] GPIO4_C6
[11] GPIO2_B6
[11] GPIO2_B7
[11] GPIO2_C0
[11] GPIO2_C1
[11] GPIO2_C2
TP100
LTE_LED_WWAN# [33]
GPIO4_C6_3V3 [28]
GPIO2_B6_3V3 [29]
GPIO2_B7_3V3 [28]
GPIO2_C0_3V3 [28,33]
GPIO2_C1_3V3 [28,33]
GPIO2_C2_3V3 [28,33]
R226 22R R0201 5%
R222 22R R0201 5%
R223 22R R0201 5%
R224 22R R0201 5%
SPI1_CLK_M0
SPI1_MISO_M0
SPI1_MOSI_M0
R228 1% 10K R0201
R230 R0201 1M 5%
TXS0108ERGYR
VQFN-20
VCC_1V8_S0
EXT_3V3
U34
C172 C0201 100nF 10V,X5R
C173 C0201 100nF 10V,X5R
TP103
[15] GPIO1_B0_u
[11] GPIO1_C6
[15] GPIO1_D7_u
[15] GPIO1_B5_u
[15] GPIO1_D6_u
[15] GPIO1_B4_u
[15] GPIO1_A7_u
TP101
GPIO1_B0_u_3V3 [28]
GPIO1_C6_3V3 [28]
GPIO1_D7_u_3V3 [28]
GPIO1_B5_u_3V3 [28]
GPIO1_D6_u_3V3 [28]
GPIO1_B4_u_3V3 [28]
GPIO1_A7_u_3V3 [28]
R231 1% 10K R0201
R232 R0201 1M 5%
TXS0108ERGYR
VQFN-20
Imax=2A
EXT_3V3
C174 C0805 22uF 25V,X5R
J10
Header 2x20 2.54mm
header2x20p_2d54_dip
Imax=2A
VCC_5V0
C175 C0805 22uF 25V,X5R
[15,22,29] I2C3_SDA_M1
[15,22,29] I2C3_SCL_M1
[28] GPIO4_C6_3V3
[7] GPIO0_C0
[28] GPIO2_B7_3V3
[28] GPIO1_C6_3V3
SPI1_MOSI_M0 [28,33] GPIO2_C2_3V3
SPI1_MISO_M0 [28,33] GPIO2_C1_3V3
SPI1_CLK_M0 [28,33] GPIO2_C0_3V3
[7,18,21,29,33] I2C6_SDA_3V3
[7] GPIO0_C5_u
[15] GPIO4_B0
[28] UART4_TX_M0_3V3
[28] UART4_RX_M0_3V3
[28] GPIO1_D6_u_3V3
R233 100R R0201 1%
R234 100R R0201 1%
nPi_GPIO2
nPi_GPIO3
nPi_GPIO4
nPi_GPIO17
nPi_GPIO27
nPi_GPIO22
nPi_GPIO10
nPi_GPIO9
nPi_GPIO11
nPi_GPIO5
nPi_GPIO6
nPi_GPIO13
nPi_GPIO19
nPi_GPIO26
nPi_GPIO14
nPi_GPIO15
nPi_GPIO18
nPi_GPIO23
nPi_GPIO24
nPi_GPIO25
nPi_GPIO8
nPi_GPIO7
nPi_GPIO12
nPi_GPIO16
nPi_GPIO20
nPi_GPIO21
D26 D27 D28 D29 D30 D31 D32 D33 D34 D35 D36 D37 D38 D39 D40
D41 D42 D43 D44 D45 D46 D47 D48 D49 D50 D51 D52 D53
SPI1_CS0_M0 [28,33] GPIO2_C3_3V3
[7] GPIO0_C6_u
5% R0201 22R R471
5% R0201 22RDNP R472
nPi_GPIO8
UART2_TX_DEBUG_PORT [7]
UART2_RX_DEBUG_PORT [7]
GPIO1_A7_u_3V3 [28]
GPIO1_B0_u_3V3 [28]
GPIO1_B4_u_3V3 [28]
GPIO1_B5_u_3V3 [28]
GPIO1_B3_3V3 [28]
I2C6_SCL_3V3 [7,18,21,29,33]
GPIO1_D7_u_3V3 [28]
GPIO1_B7_u_3V3 [28]
GPIO0_C4 [7]
GPIO2_C0_3V3 [28,33]
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Title: RK3588_AIOT_SCH
Size: A3
Document Number: 28.KEY/RPI-40P/DEBUG
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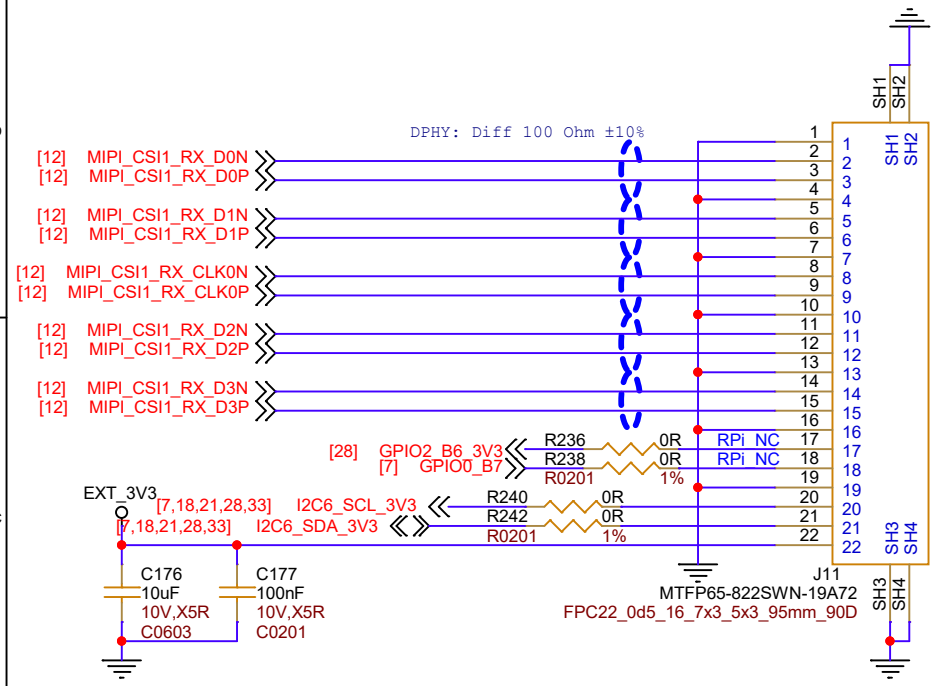
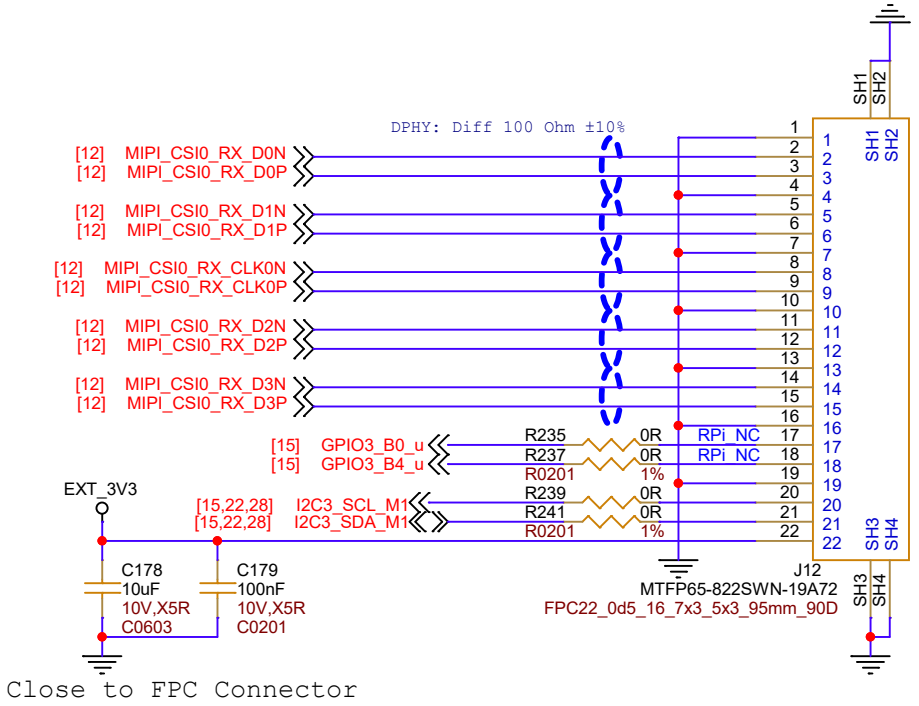
CAM0: VI-CAM MIPI DPHY CSI0 RX

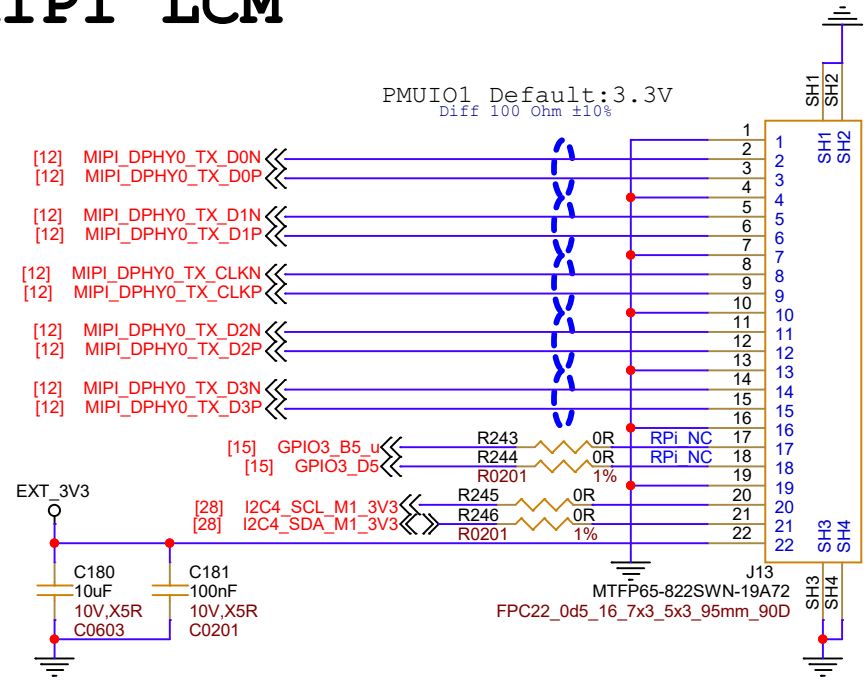


CAM1: VI-CAM MIPI DPHY CSI1/2 RX



Close to FPC Connector

MIPI LCM



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	Title: RK3588_AIOT_SCH	
Size: A4	Document Number: 29.MIPI_CSI*2/MIPI_DSI*1	Rev: V1.0
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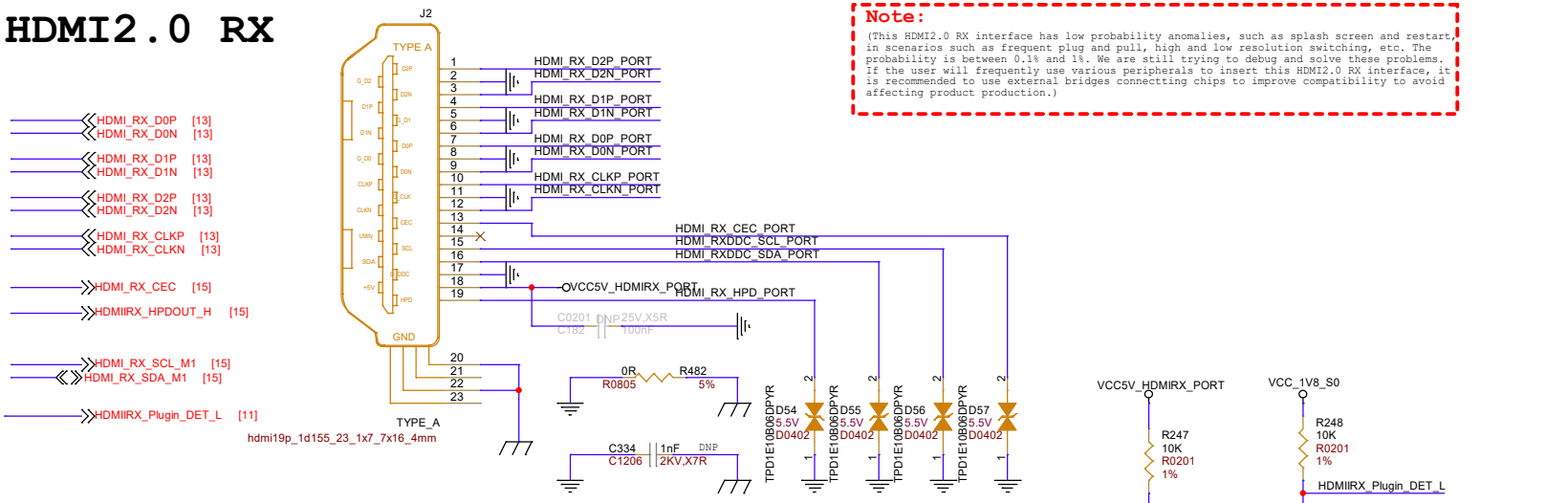
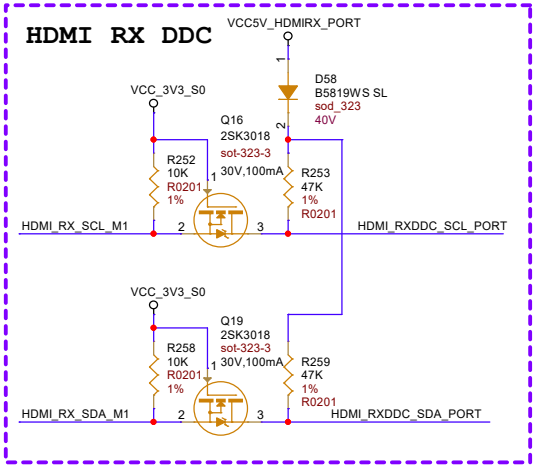
HDMI2.0 RX

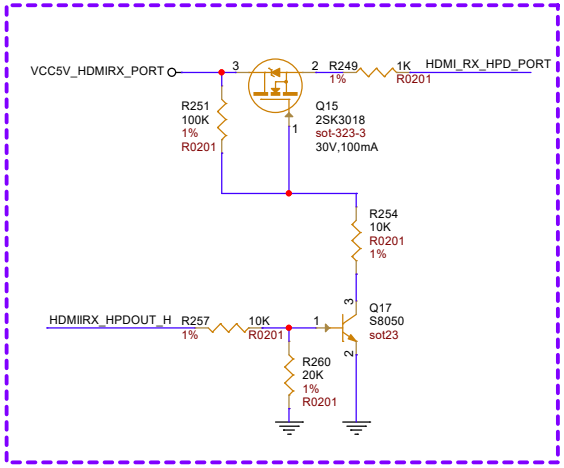
Note:

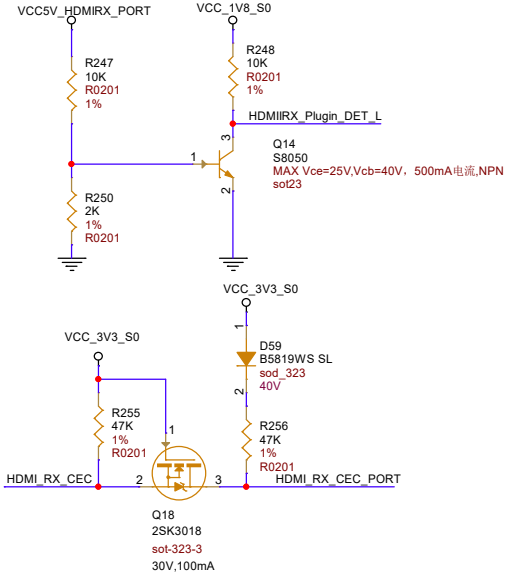
(This HDMI2.0 RX interface has low probability anomalies, such as splash screen and restart, in scenarios such as frequent plug and pull, high and low resolution switching, etc. The probability is between 0.1% and 1%. We are still trying to debug and solve these problems. If the user will frequently use various peripherals to insert this HDMI2.0 RX interface, it is recommended to use external bridges connectting chips to improve compatibility to avoid affecting product production.)



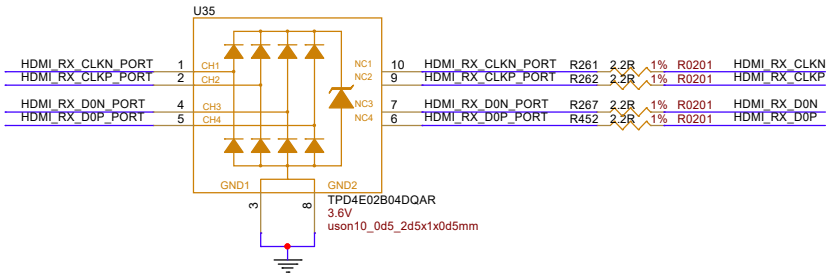
HDMI RX DDC

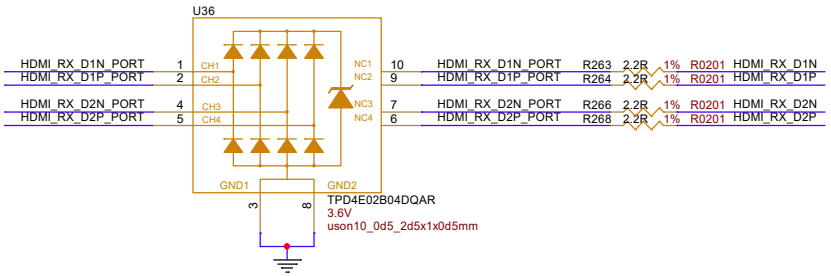






HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V





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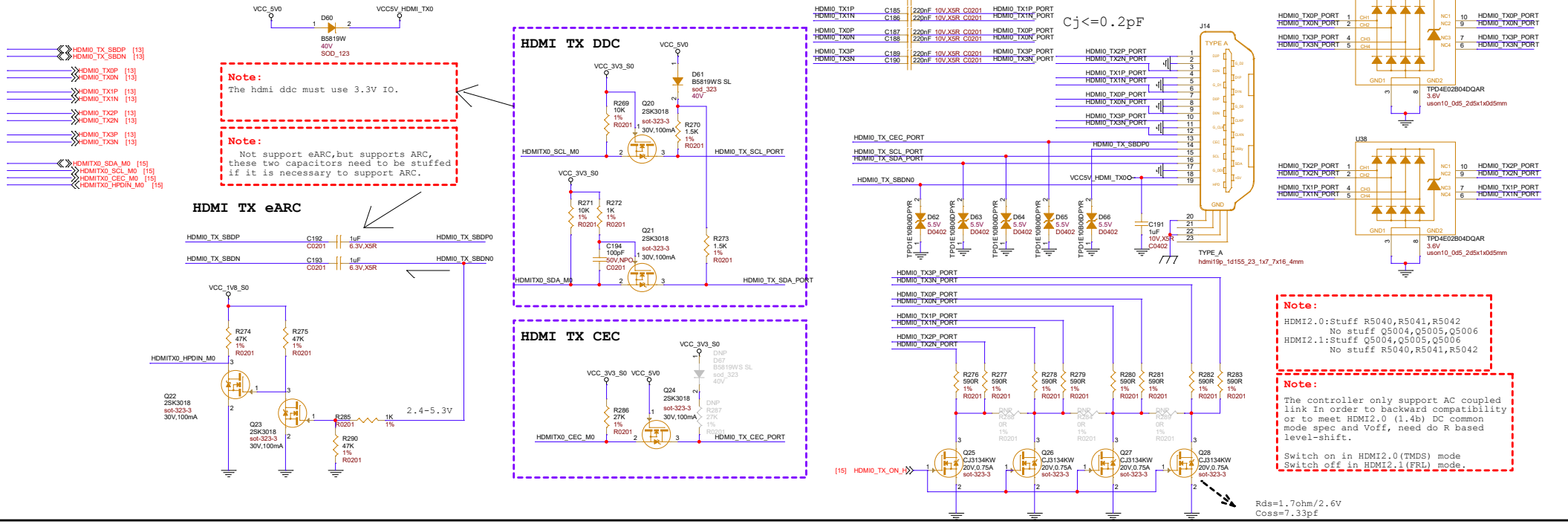
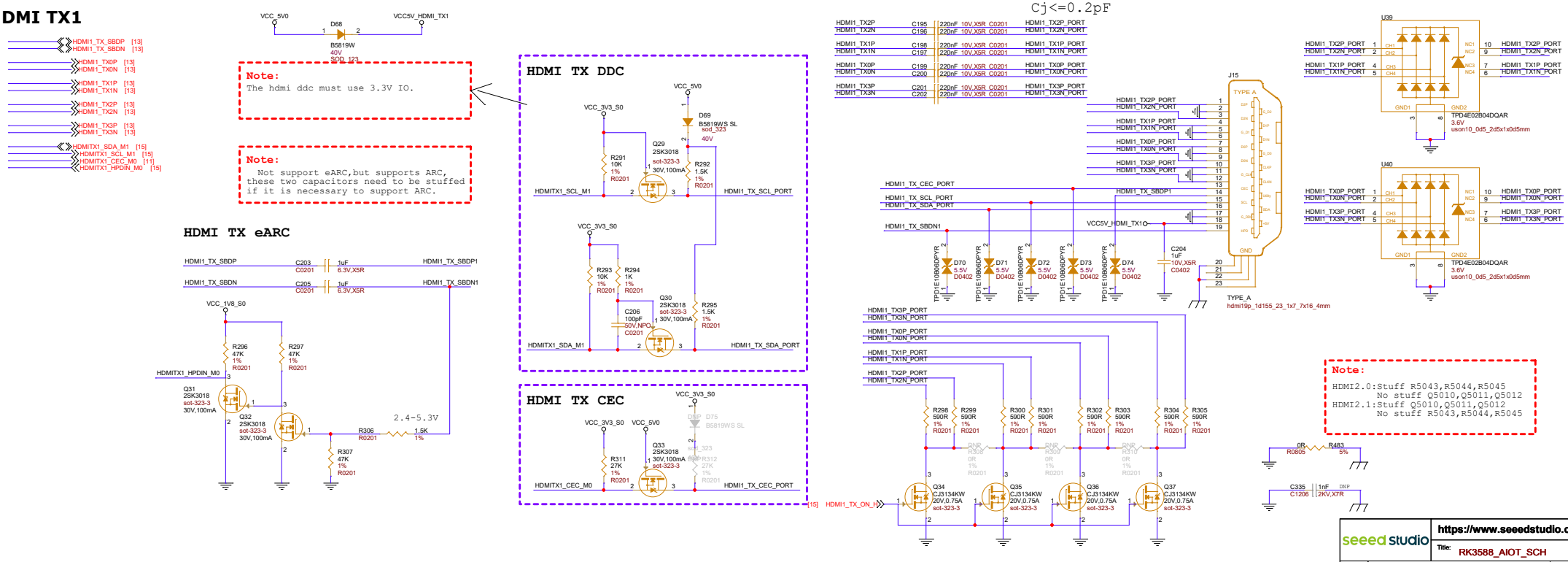
HDMI TX0



HDMI TX1



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CODEC

I2S0_MCLK [11]
I2S0_SCLK [11]
I2S0_LRCK [11]
I2S0_SDO0 [11]
I2S0_SDI0 [11]

SARADC_VIN3_HP_HOOK [11]
HP_DET_L [11]

VCC_1V8_S0 — FB4 120R 2A L0603 BLM18PG121SN1D — VCCA1V8_CODEC

VCCA_3V3_S0 — FB5 120R 2A L0603 BLM18PG121SN1D — VCCA3V3_CODEC

C212 4.7uF 10V,X5R,10% C0402
C213 100nF 10V,X5R C0201

The chip can adopt 1.8V power supply
to reduce power consumption

VCCA1V8_CODEC
C207 100nF 25V,X7R C0402

U41 ES8311 qfn20_0d4_3X3X0_75mm

4	DVDD	DACVREF	14 — C209 1uF 10V,X5R C0402
3	PVDD	ADCVREF	15 — C208 1uF 10V,X5R C0402
5	DGND	VMID	16 — C210 1uF 10V,X5R C0402
2	MCLK	AGND	10
6	CLK/DMIC_SCL	PGND	21
8	LRCK	AVDD	11
7	ASDOUT	MIC1P/DMIC_SDA	18 — LIN2_ES8388 — C211 1uF 10V,X5R — MIC_INP_PHONE
9	DSDIN	MIC1N	17 — RIN2_ES8388 — C323 1uF 10V,X5R — HP_GND
1	CCLK	OUTN	13 — HPOUT_L
19	CDATA	OUTP	12 — HPOUT_R
20	CE		

GNDA

I2S0_MCLK — R313 0R 1% R0201
I2S0_SCLK — R314 0R 1% R0201
I2S0_LRCK — R315 0R 1% R0201
I2S0_SDI0 — R316 0R 1% R0201
I2S0_SDO0 — R317 0R 1% R0201

[11] I2C7_SCL_M0_CODEC — R318 22R 5% R0201 — I2C_SCL_ES8388
[11] I2C7_SDA_M0_CODEC — R319 22R 5% R0201 — I2C_SDA_ES8388

DNP C217 100pF 50V,NPO C0201
DNP C218 100pF 50V,NPO C0201

R320 10K 1% R0201

VCCA3V3_CODEC
C216 100nF 25V,X7R C0402
C324 4.7uF 10V,X5R,10% C0402

R321 0R 5% R0805

Headphone Jack(4-pole with DET & MIC)

CTIA(L,R,G,M)

HPOUT_R — C325 47uF 6.3V,X5R C0805
HPOUT_L — C220 47uF 6.3V,X5R C0805

Q38 CJ3134KW sot-323-3 20V,0.75A
Q39 CJ3134KW sot-323-3 20V,0.75A

HPOUT_R_C
HPOUT_L_C

R324 470R 5% R0402
R325 470R 5% R0402

[15] PHONE_CTL — R328 100K 1% R0201 — R327 100K 1% R0201

DNP C224 100nF 10V,X5R C0201
DNP C225 100nF 10V,X5R C0201

MIC_INP_PHONE
VCCA3V3_CODEC

R322 2.2K 1% R0201
R323 100R 1% R0201

DNP C221 100pF 50V,NPO C0201
R326 100K 1% R0201
C222 1uF 10V,X5R C0402

HP_GND
SARADC_VIN3_HP_HOOK

R329 0R 5% R0402

DNP C223 100nF 10V,X5R C0201
R330 100K 1% R0201

VCC_3V3_S0

DNP R331 100K 1% R0201

HP_DET_L
Pull-up to
IO power rail.
short @ Plug IN

R332 1K 1% R0201

C226 100nF 10V,X5R C0201

Note:
If there is no external pull-up resistor,
SOC internal pull-up needs to be configured

D76 3.6V D0402 — TPD1E1B04DPYR
D77 3.6V D0402
D78 3.6V D0402
D79 3.6V D0402

J17 ST-PJ-35A078-A
AUDIO_6P_PJ35A078_12_9X8_25X4_35MM

MIC_INP_PHONE
HPOUT_L_C
HPOUT_R_C
HP_GND

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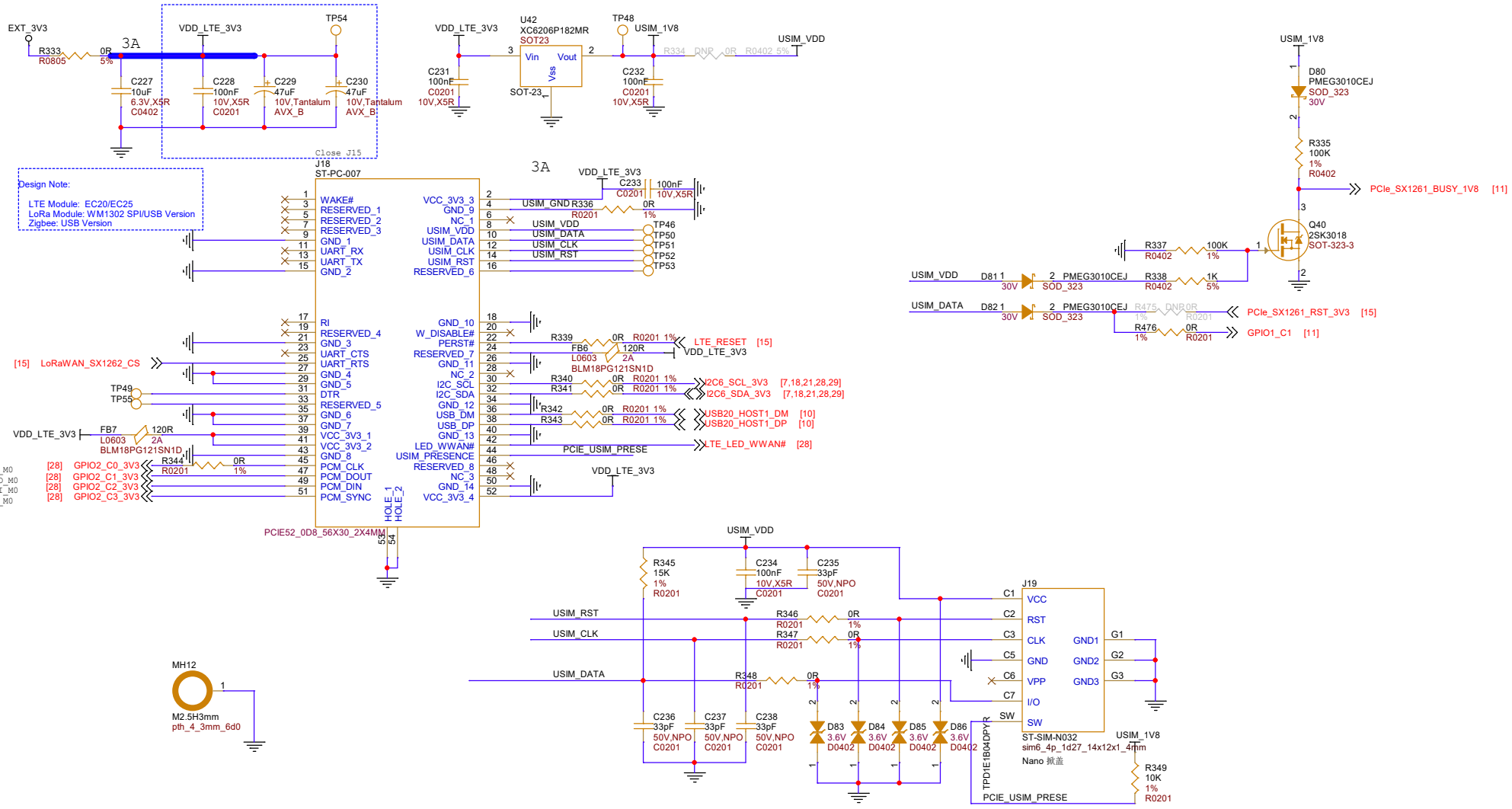

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	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 33.Mini-PCIE (4G/LORA)	Rev: V1.0
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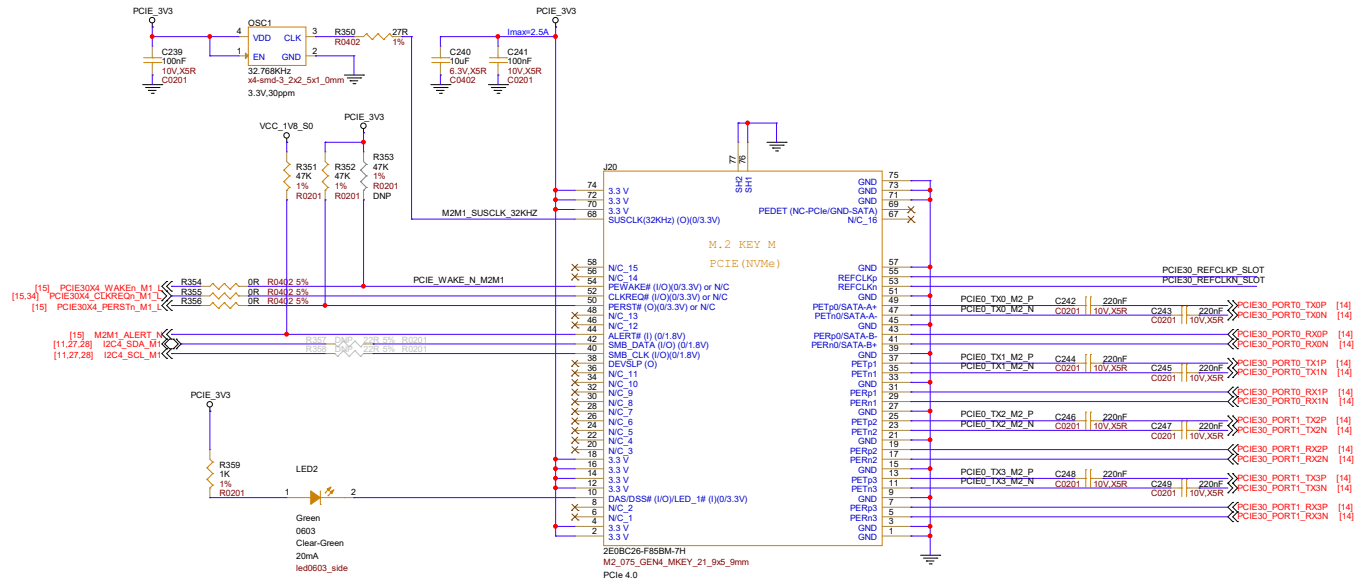
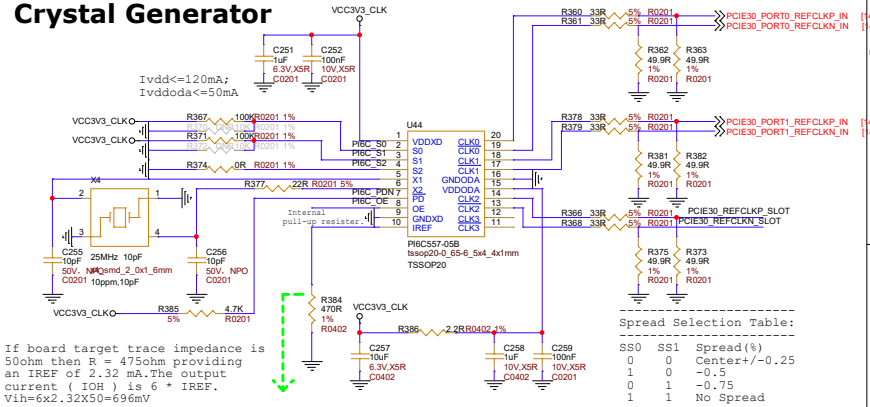
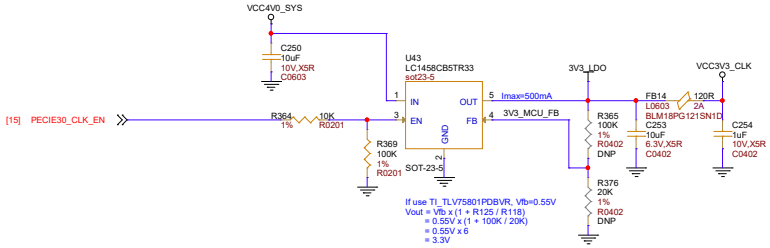
M.2 KEY-M (NVME PCIE30*4)

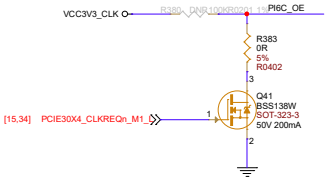


Crystal Generator

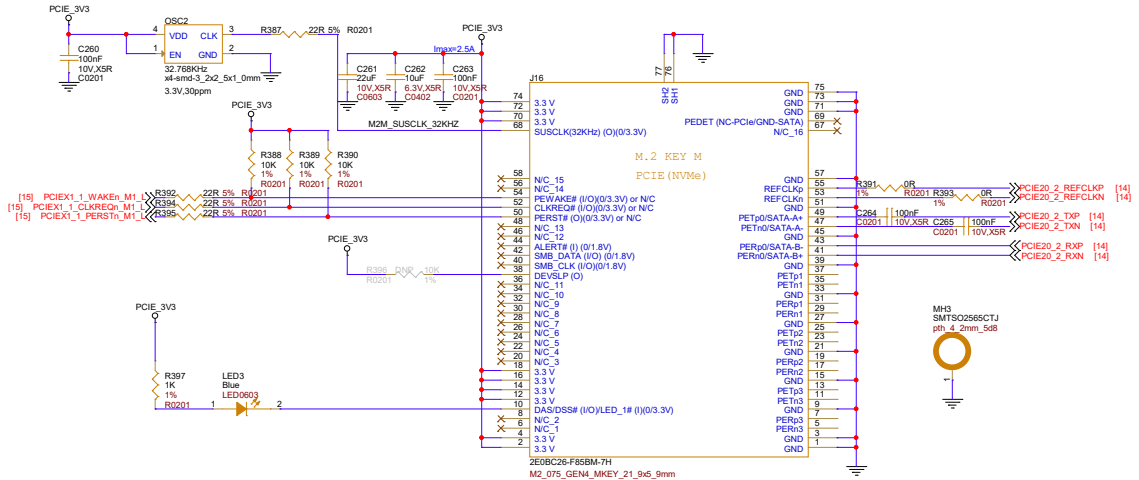


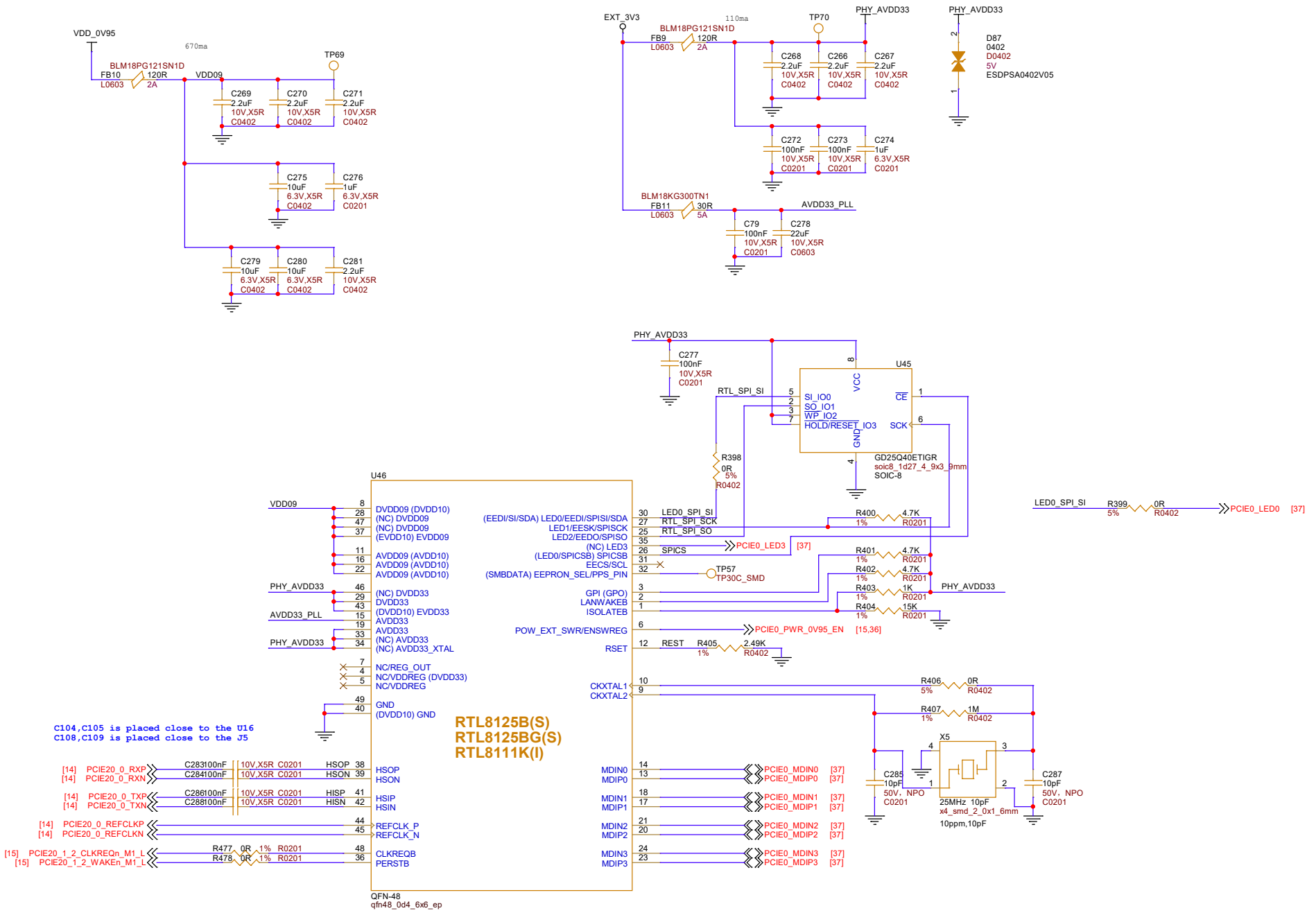
4V to 3.3V





M.2 KEY-M (NVME PCIE20)





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	Title: RK3588_AIOT_SCH	
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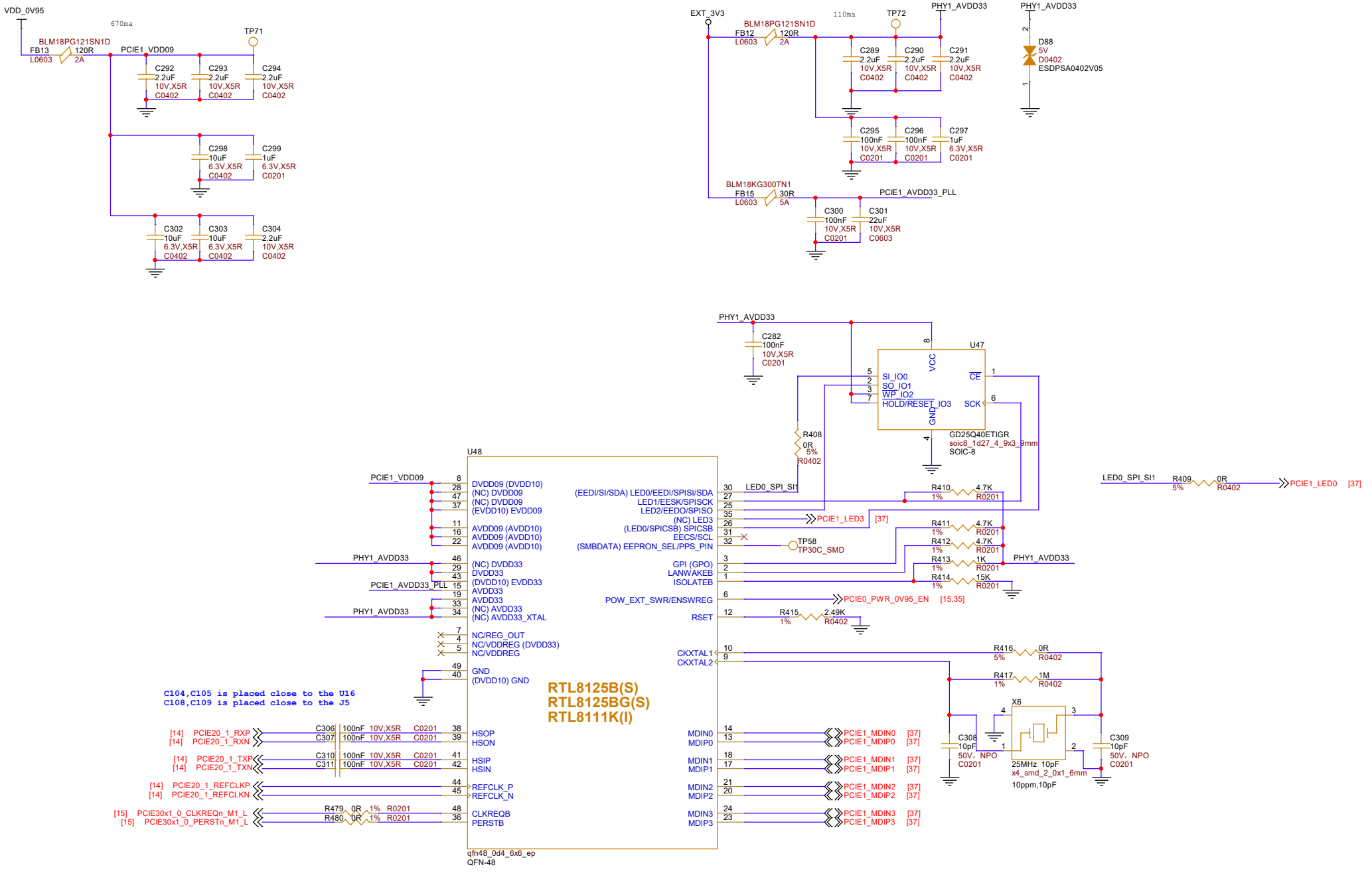

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Title:	RK3588_AIOT_SCH
Size: A3	Document Number: 36.Ethernet_Controller(PCIE1)
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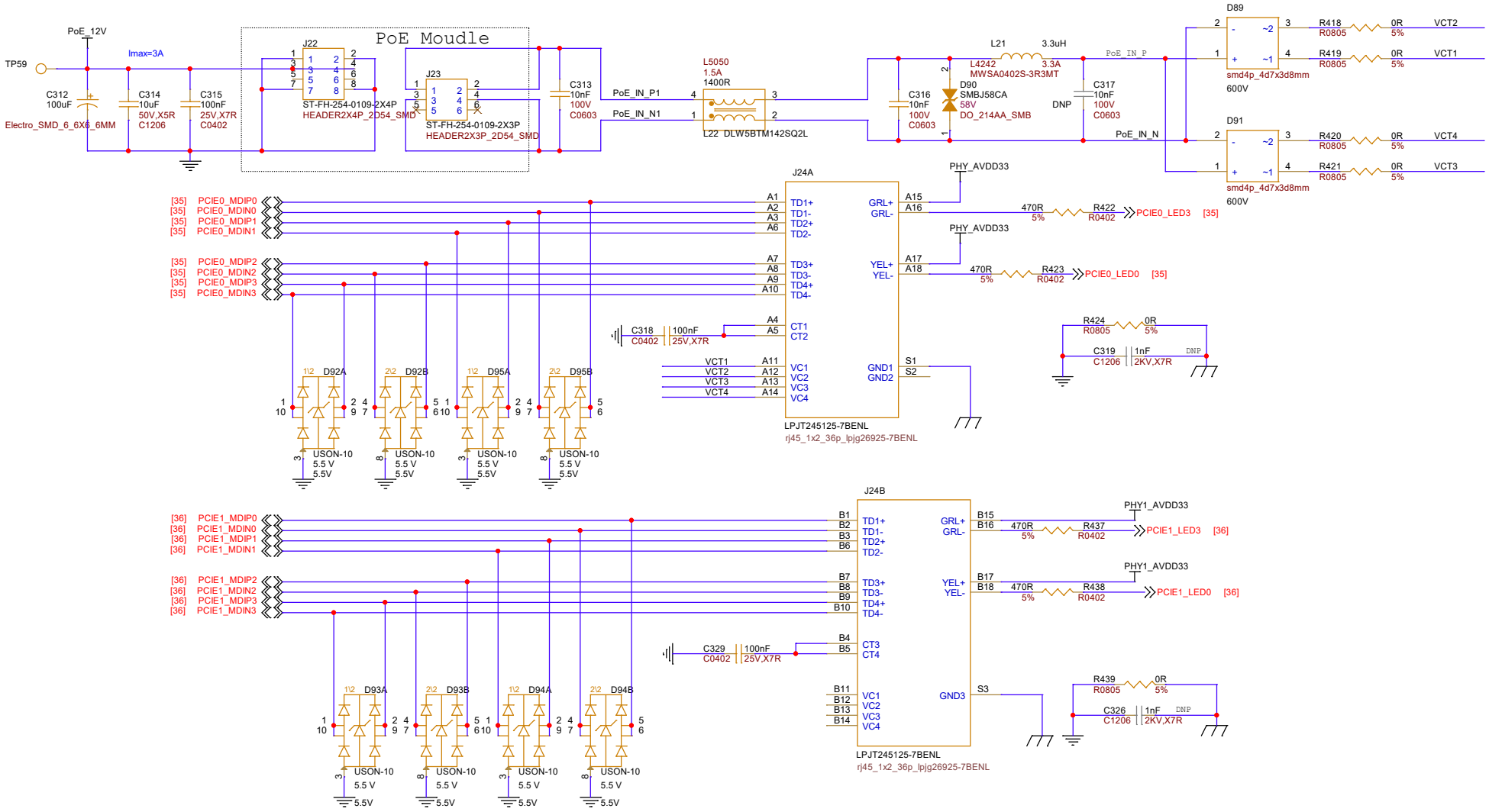
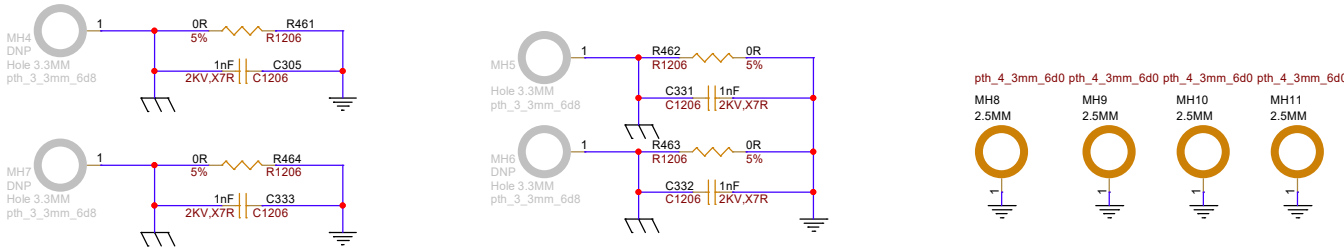
RJ45*2



Mount Hole



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	Title: RK3588_AIOT_SCH	
Size: A3	Document Number: 37.RJ45*2&HOLE	Rev: V1.0
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